LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-E040109-00-K *Advanced LIGO UK* March 2004

Electrostatic drive amplifier for controls prototype tests

D.I. Robertson, R. Pallester, K.A. Strain

Distribution of this document:
Inform aligo_sus, LASTI

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

Institute for Gravitional Research
University of Glasgow
Phone +44 141 330 5884
Fax +44 141 330 6833
E-mail k.strain@physics.gla.ac.uk

Department of
University of Birmingham
E-mail:

Engineering Department
CCLRC Rutherford Appleton Laboratory
Chilton, Didcot, Oxon OX12 0NA
Phone +44 (0) 1235 44 5297
Fax +44 (0) 1235 445843

Particle Physics and Astronomy Research Council (PPARC)

http://www.ligo.caltech.edu/

1 Introduction and scope

1.1 Purpose

This document documents the high voltage amplifiers for the controls prototype tests of quad suspensions for Advanced LIGO

1.2 Contents

- Design philosophy
- Operation
- Connection and circuit diagrams

2 References

G010086-00.

Apex PA94 data sheet available on:
http://eportal.apexmicrotech.com/mainsite/products/pages/op_amps/pa94.asp?guid=

3 Design

Two identical amplifiers have been supplied, each designed to drive one 4 quadrant electrostatic drive panel based loosely on the design used in GEO 600. The aim was to provide maximum flexibility. The amplifiers have 5 identical channels, one for the bias voltage, and one for the signal for each quadrant. The channels are DC coupled, but designed with the option of using AC bias and signals if required.

There are two functional stages in each channel: a differential receiver accepts a low voltage signal, and is followed by a high voltage gain stage. The high voltage stage is designed to allow supply voltages up to +/- 450 V (symmetrical supplies) and yet provide extremely low noise. It is hoped that this gives sufficient flexibility to cover the required range of force (not known at the time of design). The overall gain on each channel is 40 (80 on channel 0).

After initial tests it was found to be satisfactory to rely on external convection cooling, so some air space is required around the unit.

The HV OP-AMPs are APEX part PA94. The APEX data sheet should be consulted for further details. A number of spares are held at Glasgow in case of short-term supply difficulties. Key parameters of this device are:

- rail to rail supply voltage 900V maximum, 100V minimum.
- power bandwidth >>16 kHz
- input noise $11\text{nV}/\sqrt{\text{Hz}}$ at 10 Hz (typical).

4 Operation

Power supply requirements is for both low voltage (+/- 20V), and high voltage, symmetrical supplies. The HV supply must be energized symmetrically as the HV OPAMP performance can be permanently degraded by operation with only one supply. The minimum useful voltage is 50V and the maximum permissible is 450V (+/-). It is recommended that supplies above

300V should be used with caution as tests at Glasgow were carried out with +/- 300V, the highest available.

Current consumption from the HV rails (no load) is 120mA (36W per rail at 300V).

Current consumption from the LV rails (no load) is ~1A from +20V and ~50mA from –20V. The +20V line takes this high current because it also powers the internal cooling fans. The LV power is regulated to +/- 15V for the sensitive circuitry.

The units accept 5 inputs, differentially, on sub-D connectors as specified below. The maximum input voltage is +/- 12V with respect to case ground. The input devices are LT1125s, there is no additional input protection and so caution should be used to check input signal levels before connection.

Outputs are provided on SHV connectors, one per channel, the maximum output is about 20V less than the appropriate supply rail. Caution should be used in dealing with high voltages, and warning labels compliant with local regulations should be attached. The outputs are single ended.

If DC bias is used there are no special considerations with respect to power dissipation. Sufficiently high voltage and high frequency AC bias will, however, cause problems. The units were tested driving 300Vpp at 16kHz into a 1nF capacitive load (to represent reasonable lengths of cable). It is recommended that AC bias at 8192 or 16384 Hz be considered. The output current limits at ~100mA, equivalent to a 480Vpp signal at 16kHz driving a 2nF load.

5 Diagrams

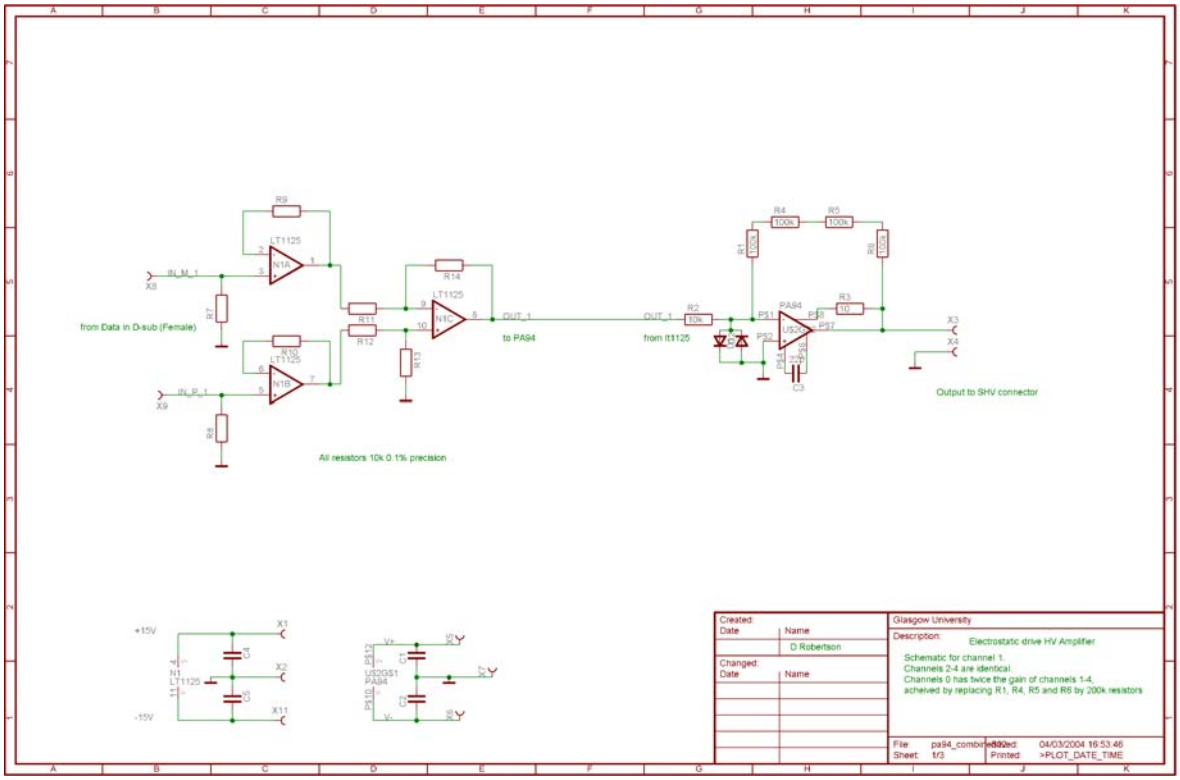

Figure 1 Schematic for one channel of the ESD drive. All the channels are identical except channel 0 which has twice the gain in the final HV amplifier.

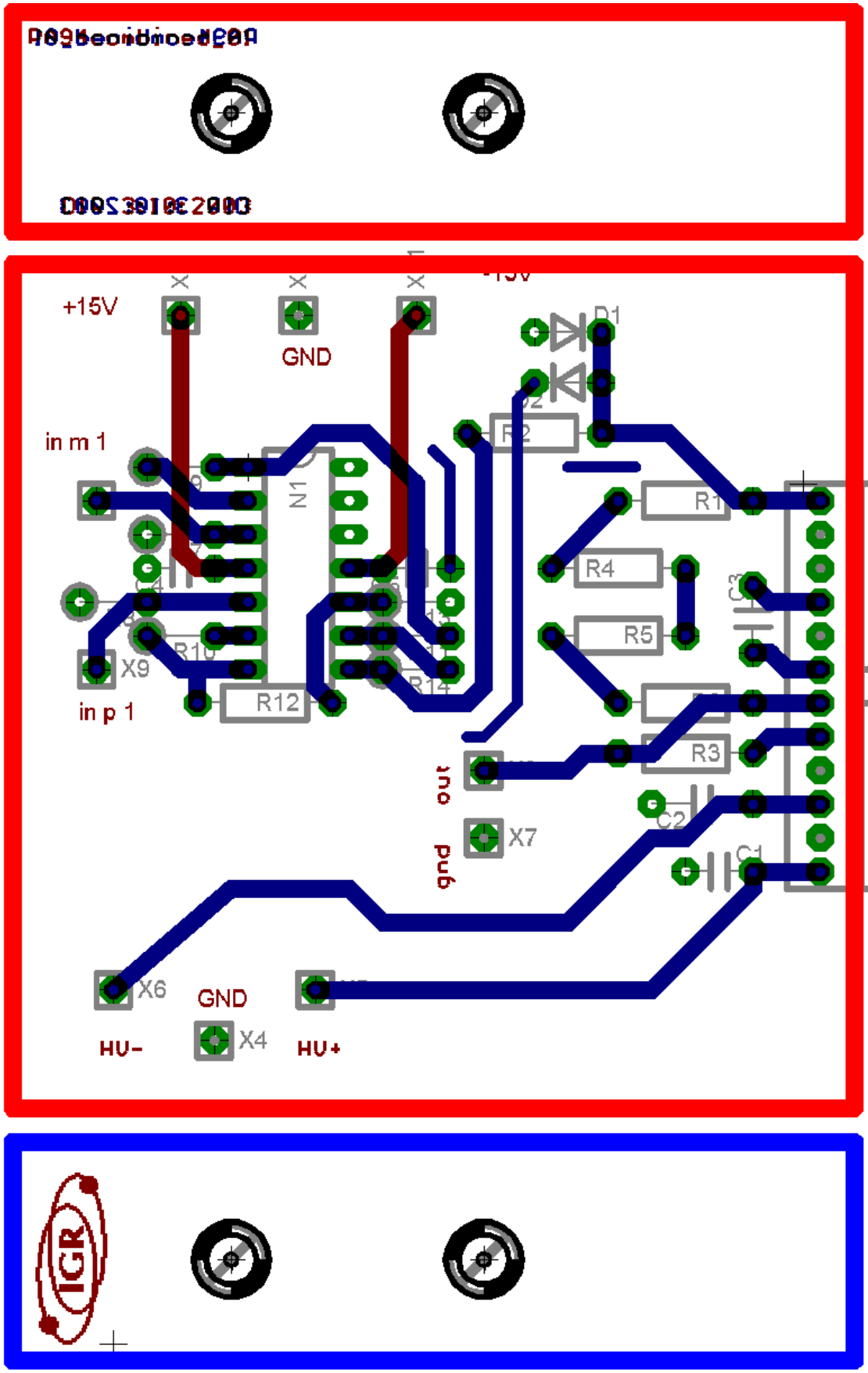

Figure 2 Board layout for one of the amplifiers. Red lines are on the component side and blue on the underside.

5.1 Connector information

Low Voltage in (D-sub male on box)

Pins 1 and 2	+20V
Pins 7 and 8	-20V
Pins 11,12,13	Common

Data in (D-sub female on box)

Pin 1	m1
Pin 2	m2
Pin 3	m3
Pin 4	m4
Pin 5	gnd
Pin 6	gnd
Pin 7	m0
Pin 8	n/c
Pin 9	p1
Pin 10	p2
Pin 11	p3
Pin 12	p4
Pin 13	gnd
Pin 14	p0
Pin 15	n/c

HV in (9 pin round socket)

Pin1	+ve HT
Pin3	-ve HT
Pin9	common

Outputs (SHV)

B0

B1

B2

B3

B4