LIGO Laboratory / LIGO Scientific Collaboration

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OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

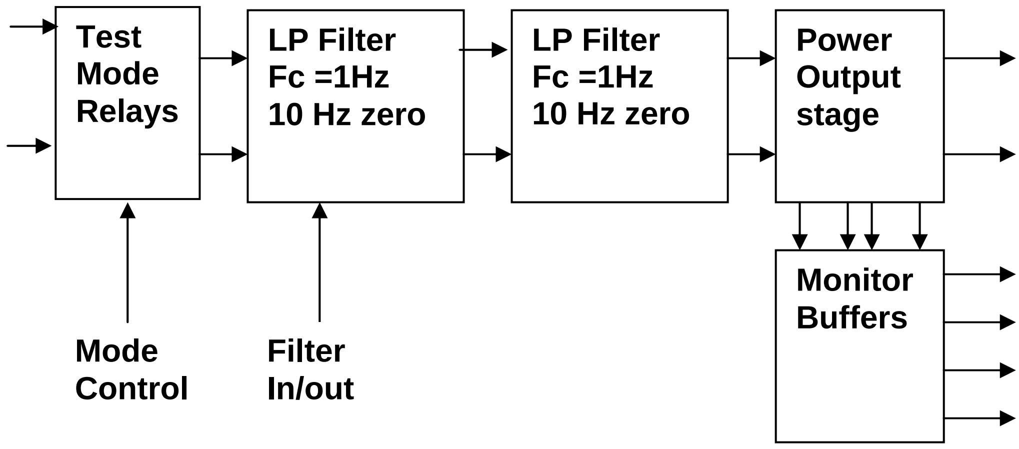
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_10……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

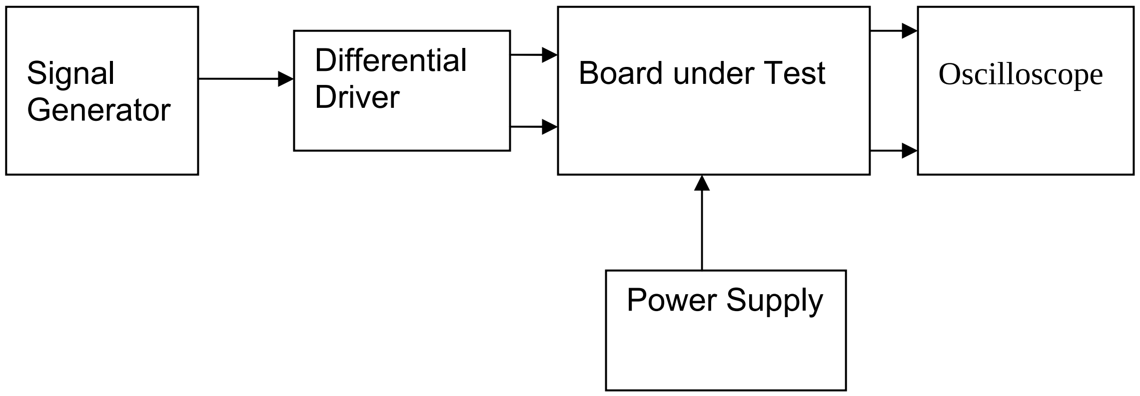
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.05	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.17	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3.3v to 3.7v	√
Ch2	3.3	3.3v to 3.7v	√
Ch3	3.3	3.3v to 3.7v	√
Ch4	3.3	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.49	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

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9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	**Ch1 stable ?**	**Ch2 o/p**	**Ch2 stable ?**	**Ch3 o/p**	**Ch3 stable ?**	**Ch4 o/p**	**Ch4 stable ?**
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.4	√	-17.4	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.5	√	-2.5	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.5	√	2.5	√	2.5	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Output @ 10Hz	Maximum o/p	@ Frequency
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

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13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.14	√
Ch2	**1.12v**	1.14	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.14	√

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OMC COIL DRIVER BOARD
TEST PLAN

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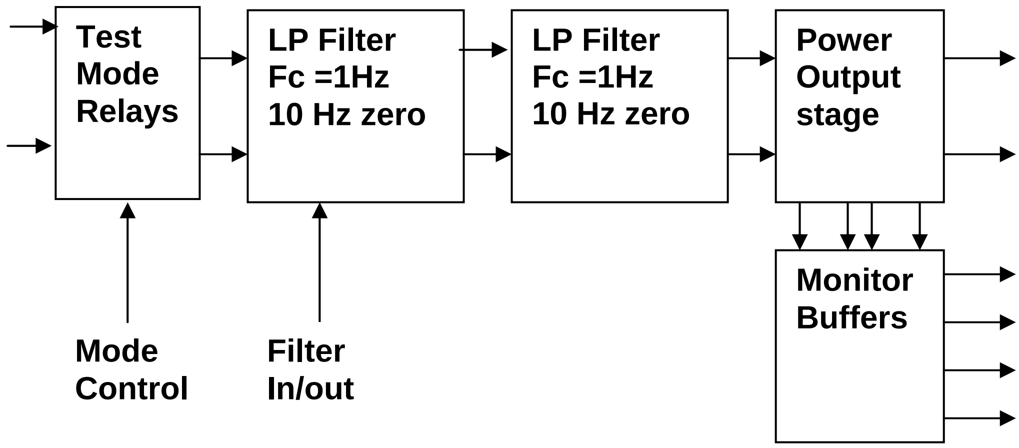

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

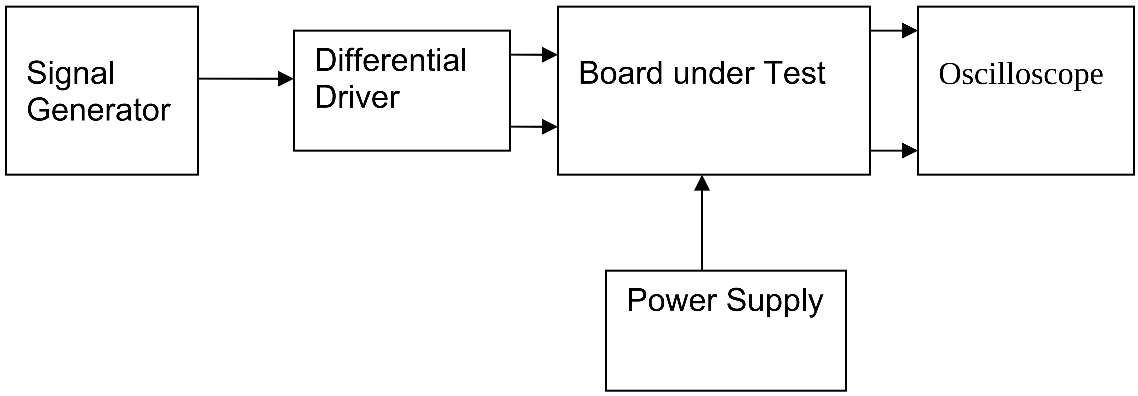
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

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J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

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3 Pin Power Connector

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If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.99	1mV	√
+15v TP4	14.96	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	250mA
-16.5v	350mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

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Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..OMC_2……………………Serial No ………………………………
Test Engineer…..Xen………………………
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

Unit……………….OMC_2……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10..…………………

8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_2……………………Serial No ………………………………
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Date……………..27/10/10…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit………………OMC_2……………………Serial No ………………………………
Test Engineer…..Xen………………….……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	**Ch1 stable ?**	**Ch2 o/p**	**Ch2 stable ?**	**Ch3 o/p**	**Ch3 stable ?**	**Ch4 o/p**	**Ch4 stable ?**
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.3	√	-17.4	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.4	√	-2.4	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.4	√	2.4	√	2.4	√
5v	12.3	√	12.3	√	12.4	√	12.4	√
7v	17.0	√	17.0	√	17.2	√	17.2	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	**OUTPUT CHANNEL**	**Maximum Output**	**@ Frequency**
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.14	√

LIGO Laboratory / LIGO Scientific Collaboration

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OMC Coil Driver Board Test Plan

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

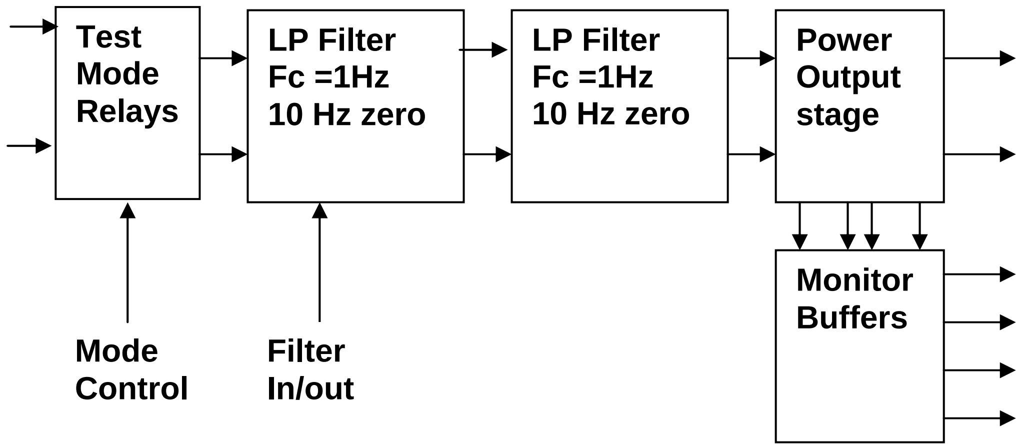
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_3……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..27/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……………..OMC_3……………………Serial No ………………………………
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

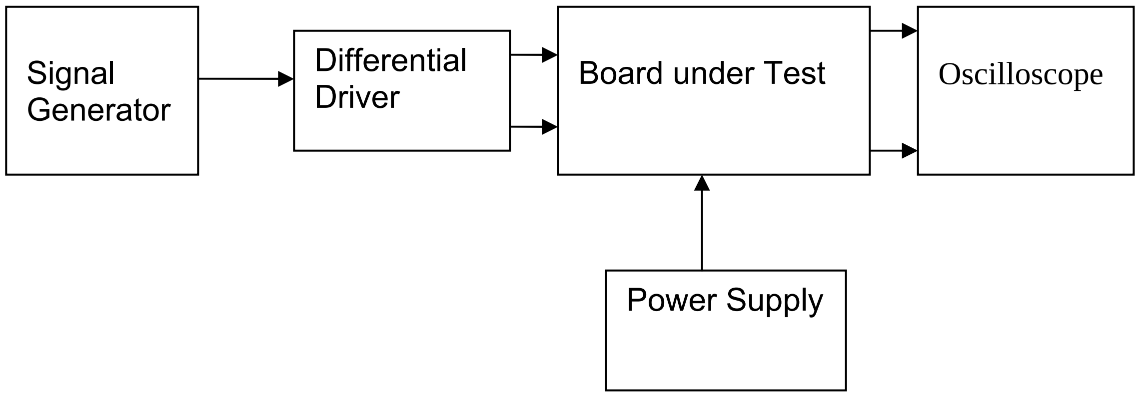
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………….OMC_3……………………Serial No ………………………………
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.11	1mV	√
+15v TP4	14.94	1mV	√
-15v TP6	-15.07	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_3……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..27/10/10…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

Unit……………..OMC_3……………………Serial No ……………………………..
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8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.46	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit………………OMC_3……………………Serial No ………………………………
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9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit………………OMC_3……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.3	√	-17.3	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.4	√	-12.5	√
-1v	-2.5	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.5	√	2.4	√	2.4	√
5v	12.1	√	12.5	√	12.3	√	12.0	√
7v	17.0	√	17.2	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer……………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	**OUTPUT CHANNEL**	**Maximum Output**	**@ Frequency**
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……………….OMC_3……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..27/10/10.…………………

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	**Ch2**	**Ch3**	**Ch4**
Not Clipping?	√	√	√	√

	Theoretical o/p	**Measured**	**OK+/- 0.1v?**
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.13	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T1000567-v1 Advanced LIGO UK 29 September 2010

OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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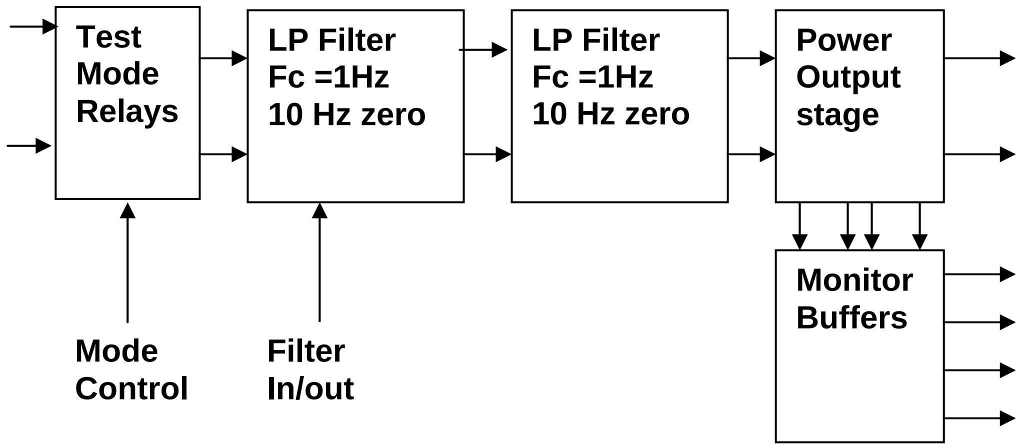
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_4……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..27/10/10…………………

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

Unit………………OMC_4……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10.…………………

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..27/10/10…………………

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

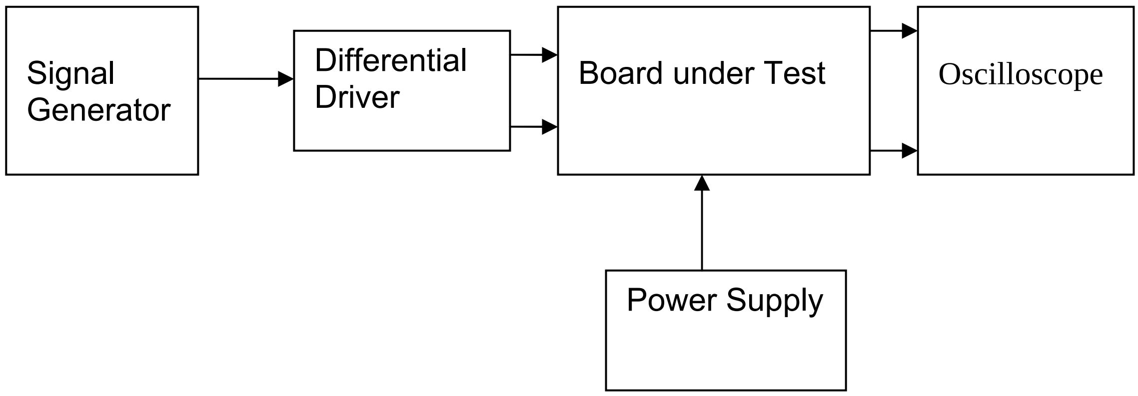
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit………………OMC_4……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..27/10/10.…………………

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	11.98	1mV	√
+15v TP4	14.93	1mV	√
-15v TP6	-15.03	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10.…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………OMC_4……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..27/10/10…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.35	3.3v to 3.7v	√
Ch2	3.35	3.3v to 3.7v	√
Ch3	3.35	3.3v to 3.7v	√
Ch4	3.35	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.67	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.67	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..27/10/10…………………

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.50	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..27/10/10…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10…………………

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.4	√	-17.4	√	-17.3	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.4	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.4	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.5	√	2.5	√	2.5	√
5v	12.2	√	12.3	√	12.2	√	12.1	√
7v	17.0	√	12.2	√	17.0	√	12.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit…………………………………..Serial No ……………………………..
Test Engineer……………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	**OUTPUT CHANNEL**	**Maximum Output**	**@ Frequency**
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……………….OMC_4……………………Serial No ………………………………
Test Engineer…..Xen…………………..……
Date……………..27/10/10.…………………

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.13	√

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LIGO-T1000567-v1 Advanced LIGO UK 29 September 2010

OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

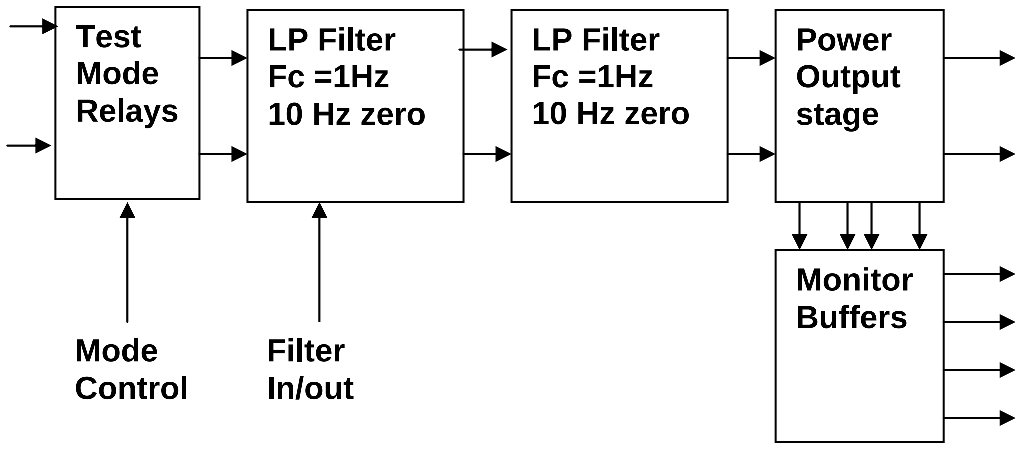
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_5……………………Serial No ………………………………
Test Engineer…..Xen…………………..……
Date……………..28/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit………………OMC_5……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..28/10/10..…………………

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

Unit………………OMC_5……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..27/10/10.…………………

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit……………….OMC_5…………………….Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..27/10/10…………………

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

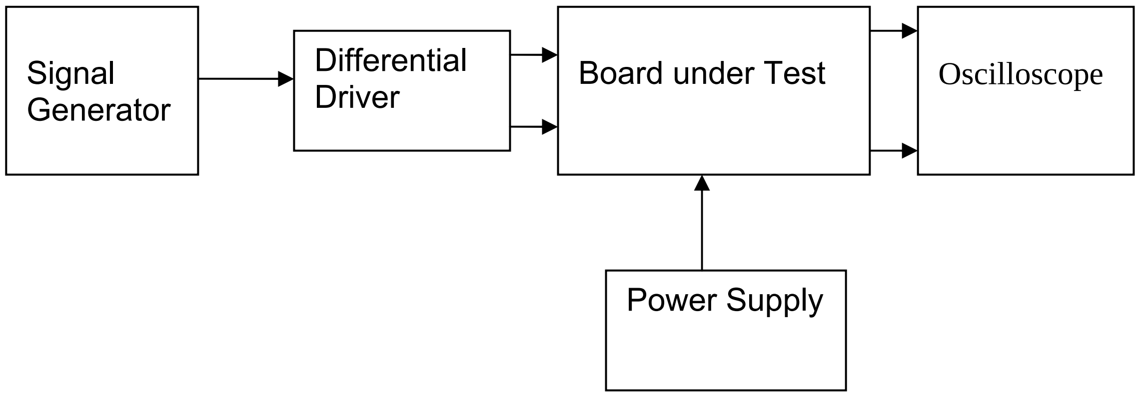
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………….OMC_5……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..27/10/10.…………………

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.04	1mV	√
+15v TP4	14.86	1mV	√
-15v TP6	-15.05	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit………………OMC_5……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..27/10/10.…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_5……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..28/10/10…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

Unit………………OMC_5……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..28/10/10…………………

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.50	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.49	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………..OMC_5……………………Serial No ………………………………
Test Engineer…..Xen…………………..……
Date……………..28/10/10…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………….OMC_5……………………Serial No ………………………………
Test Engineer…..Xen………………………
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.3	√	-17.3	√	-17.5	√
-5v	-12.5	√	-12.4	√	-12.5	√	-12.5	√
-1v	-2.4	√	-2.4	√	-2.4	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.4	√	2.5	√
5v	12.0	√	12.0	√	12.0	√	12.3	√
7v	17.0	√	17.0	√	17.0	√	17.1	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………..OMC_5……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..28/10/10…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Output @ 10Hz	Maximum o/p	@ Frequency
Channel 1	Channel 2	-138.4dB	-115.3dB	238Hz
Channel 2	Channel 1	-136.1dB	-108.8dB	234Hz
Channel 2	Channel 3	-132.6dB	-110.7dB	269Hz
Channel 3	Channel 2	-134.5dB	-108.5dB	468Hz
Channel 3	Channel 4	-134.0dB	-107.1dB	251Hz
Channel 4	Channel 3	-137.5dB	-106.4dB	251Hz

Unit……………...OMC_5……………………Serial No ………………………………
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13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.13	√

LIGO Laboratory / LIGO Scientific Collaboration

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OMC Coil Driver Board Test Plan

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

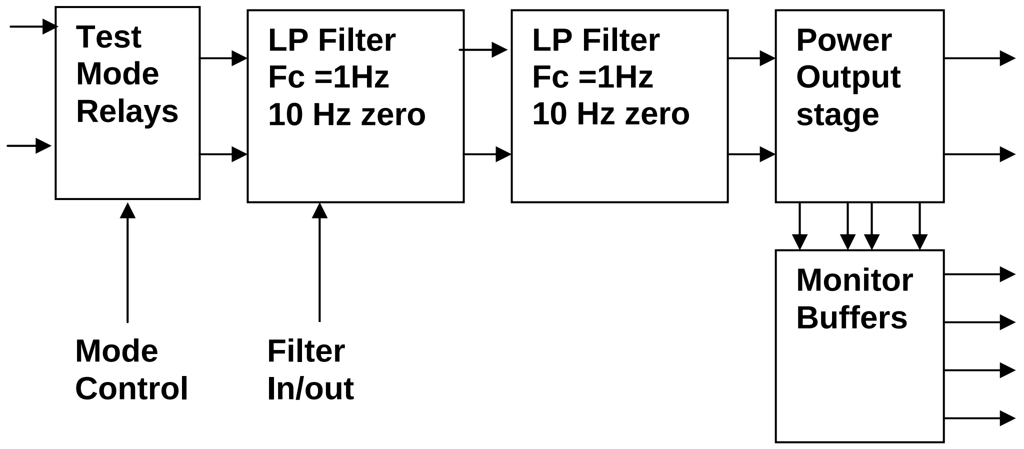
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_6……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..28/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit………………OMC_6……………………Serial No ………………………………
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit………………OMC_6……………………Serial No ………………………………
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

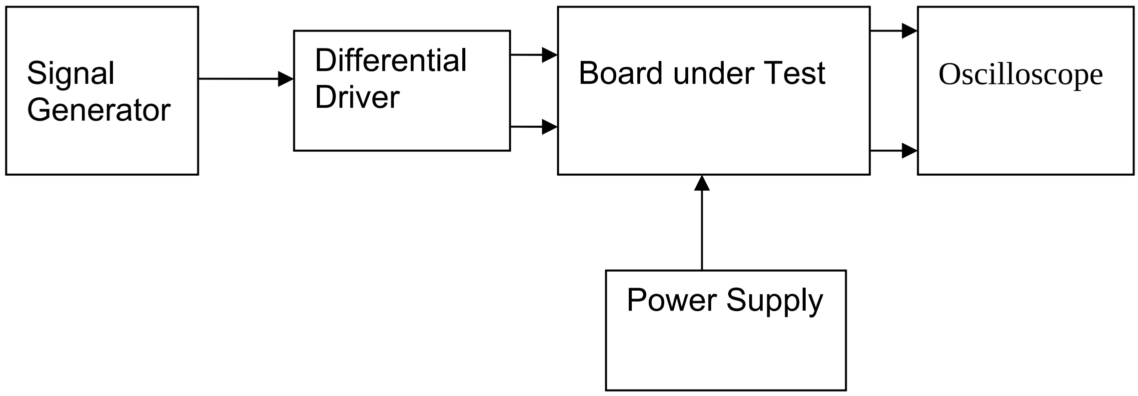
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit………………OMC_6……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.02	1mV	√
+15v TP4	14.91	1mV	√
-15v TP6	-15.02	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit………………OMC_6……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_6……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..28/10/10…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.67	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

Unit………………OMC_6……………………Serial No ………………………………
Test Engineer…..Xen………………………
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8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.49	0.4v to 0.5v	√
Ch2	0.50	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_6……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..28/10/10.…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………….OMC_6……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..28/10/10..…………………

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	**Ch1 stable ?**	**Ch2 o/p**	**Ch2 stable ?**	**Ch3 o/p**	**Ch3 stable ?**	**Ch4 o/p**	**Ch4 stable ?**
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.4	√	-17.4	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.4	√	-2.6	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.5	√	2.5	√	2.4	√
5v	12.3	√	12.3	√	12.2	√	12.2	√
7v	17.0	√	17.2	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Output @ 10Hz	Maximum o/p	@ Frequency
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit………………OMC_6……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..28/10/10.…………………

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.13	√

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LIGO-T1000567-v1 Advanced LIGO UK 29 September 2010

OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

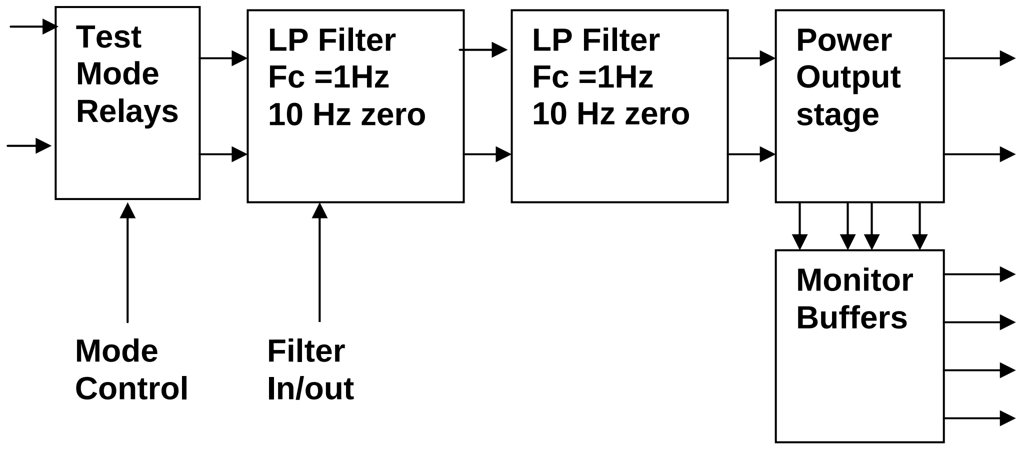
OMC COIL DRIVER BOARD
TEST PLAN

Unit……………….OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit………………OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10.…………………

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	**Manufacturer**	**Model**	**Serial Number**
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

Unit……………….OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit………………OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

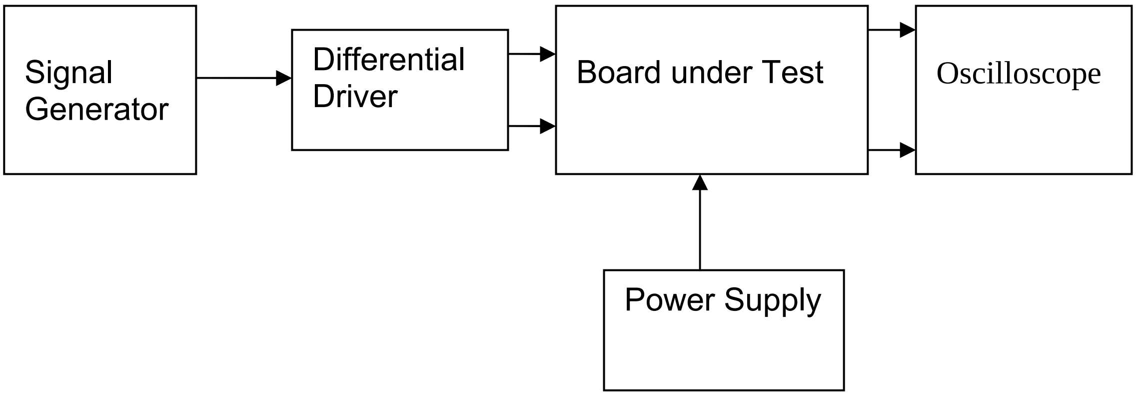
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit………………OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.03	1mV	√
+15v TP4	15.02	1mV	√
-15v TP6	-15.08	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit………………OMC_7……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..28/10/10…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_7……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..29/10/10.…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.3	3.3v to 3.7v	√
Ch4	3.3	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.48 to 0.75v	√
Ch2	0.47	0.48 to 0.75v	√
Ch3	0.47	0.48 to 0.75v	√
Ch4	0.48	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

Unit………………OMC_7……………………Serial No ………………………………
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8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.25	3v to 3.4v	√
Ch2	3.25	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.49	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_7…………………….Serial No ………………………………
Test Engineer…..Xen……………………..….
Date……………..29/10/10…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………..OMC_7……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..29/10/10…………………

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.5	√	-17.4	√	-17.4	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.4	√	-2.5	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.4	√	2.4	√	2.5	√	2.5	√
5v	12.0	√	12.0	√	12.5	√	12.5	√
7v	17.0	√	17.0	√	17.4	√	17.4	√
10v	24.5	√	24.4	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer……………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

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Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	**OUTPUT CHANNEL**	**Output @ 10Hz**	**Maximum o/p**	**@ Frequency**
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……………….OMC_7……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..29/10/10.…………………

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	**Ch2**	**Ch3**	**Ch4**
Not Clipping?	√	√	√	√

	Theoretical o/p	**Measured**	**OK+/- 0.1v?**
Ch1	**1.12v**	1.14	√
Ch2	**1.12v**	1.13	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.14	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T1000567-v1 Advanced LIGO UK 29 September 2010

OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

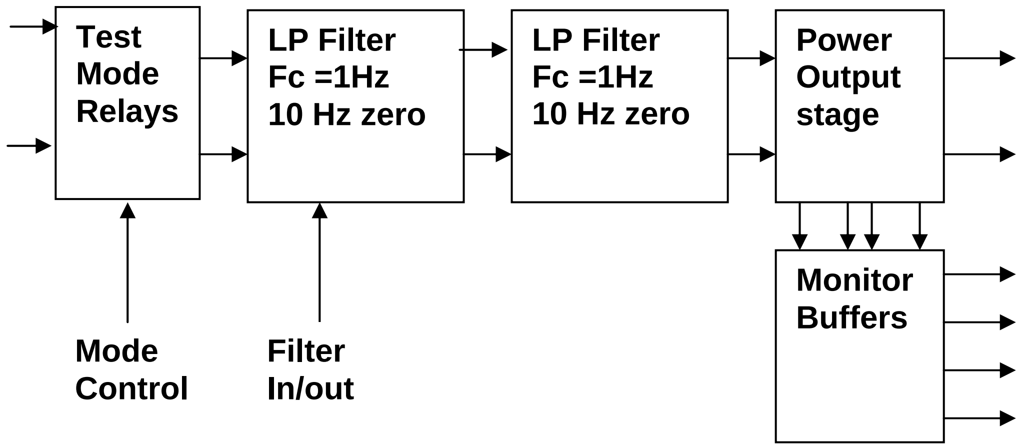
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_8……………………Serial No ………………………………
Test Engineer…..Xen…………………..……
Date……………..29/10/10…………………

Contents

1. Description

Block diagram



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The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen………………….……
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2. Test equipment

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V/I calibrator	Time Electronics	1044	
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Unit………………OMC_8……………………Serial No ………………………………
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Workmanship

Inspect the general workmanship standard and comment: √

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C200 has been soldered across R5 and R23 on all channels.

Links:

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Unit………………OMC_8……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10.…………………

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

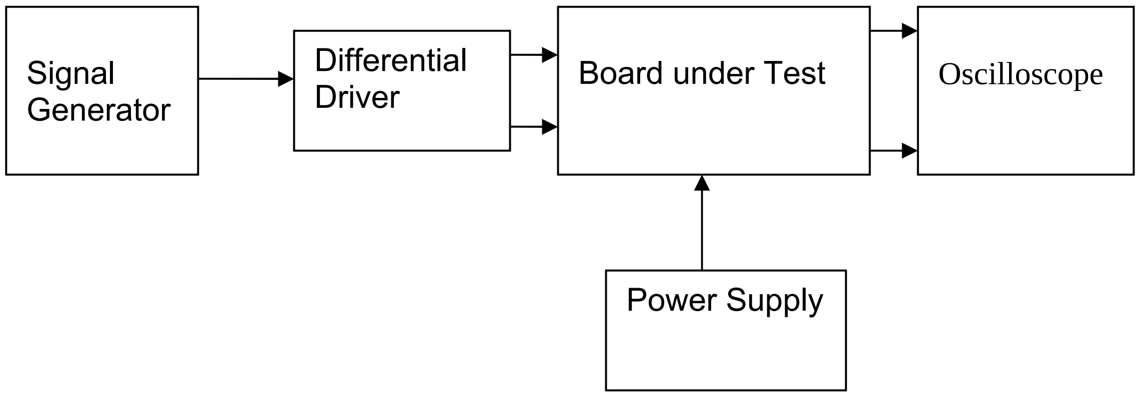
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen…………………….……
Date……………..29/10/10.…………………

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.05	1mV	√
+15v TP4	14.92	1mV	√
-15v TP6	-15.01	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10.…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen………………….……
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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen……………………..…
Date……………..29/10/10.…………………

8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.50	0.4v to 0.5v	√
Ch3	0.49	0.4v to 0.5v	√
Ch4	0.50	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_8……………………Serial No ………………………………
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9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………….OMC_8……………………Serial No ………………………………
Test Engineer…..Xen………………………
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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.5	√	-17.5	√	-17.5	√	-17.5	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.5	√	-2.5	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.5	√	2.5	√	2.5	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.5	√	17.5	√	17.5	√	17.5	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer……………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Output @ 10Hz	Maximum o/p	@ Frequency
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit……………….OMC_8……………………Serial No ………………………………
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13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.13	√
Ch2	**1.12v**	1.14	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.14	√

LIGO Laboratory / LIGO Scientific Collaboration

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OMC Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

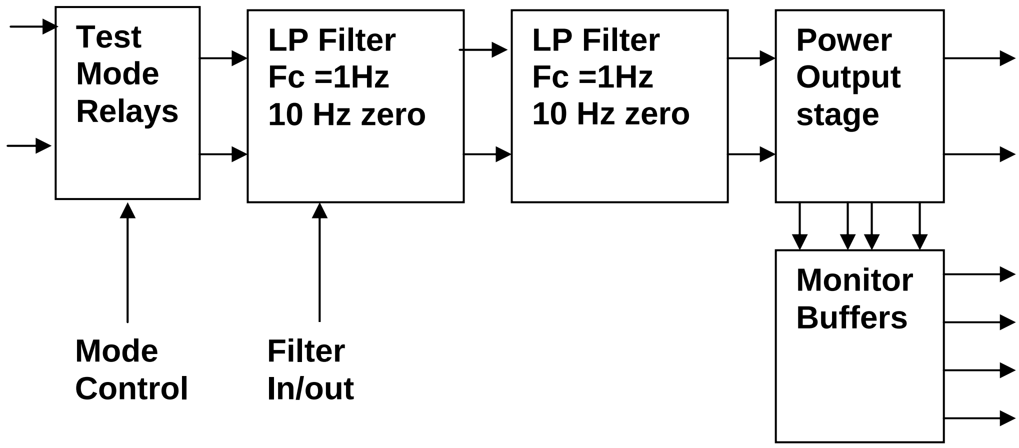
OMC COIL DRIVER BOARD
TEST PLAN

Unit………………OMC_9……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10…………………

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……………..OMC_9……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit………………OMC_9……………………Serial No ………………………………
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

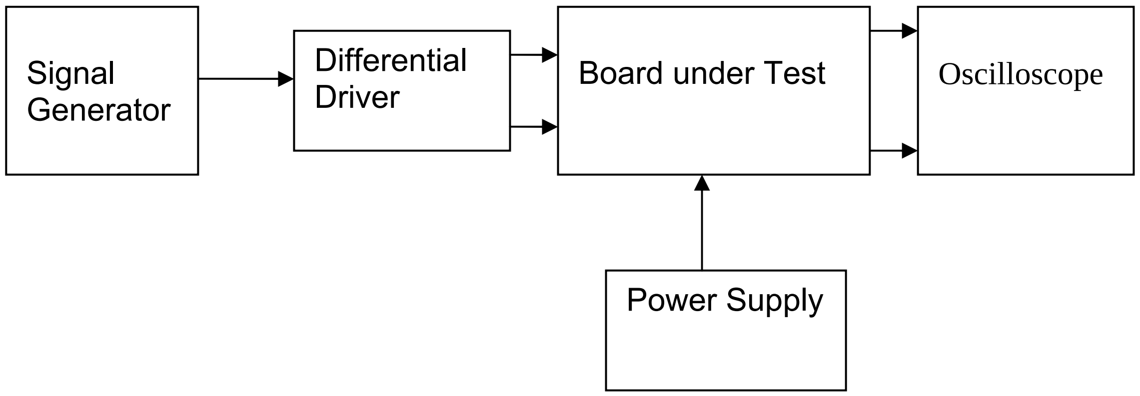
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit………………OMC_9……………………Serial No ………………………………
Test Engineer…..Xen……………………..……
Date……………..29/10/10.…………………

6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.06	1mV	√
+15v TP4	14.95	1mV	√
-15v TP6	-14.95	5mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	250mA

If the supplies are correct, proceed to the next test.

Unit………………OMC_9……………………Serial No ………………………………
Test Engineer…..Xen………………….……
Date……………..29/10/10.…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….OMC_9……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..29/10/10…………………

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3.3v to 3.7v	√
Ch2	3.3	3.3v to 3.7v	√
Ch3	3.3	3.3v to 3.7v	√
Ch4	3.3	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

Unit………………OMC_9……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..29/10/10.…………………

8.3 Fixed filter in: Remove W4, insert W5
Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.85	4.7v to 5v	√
Ch2	4.85	4.7v to 5v	√
Ch3	4.85	4.7v to 5v	√
Ch4	4.85	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.3	3v to 3.4v	√
Ch2	3.3	3v to 3.4v	√
Ch3	3.3	3v to 3.4v	√
Ch4	3.3	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 KHz

	Output	Specification	Pass/Fail
Ch1	0.16	0.14v to 0.16v	√
Ch2	0.16	0.14v to 0.16v	√
Ch3	0.16	0.14v to 0.16v	√
Ch4	0.16	0.14v to 0.16v	√

Unit……………….OMC_9……………………Serial No ………………………………
Test Engineer…..Xen………………………
Date……………..29/10/10…………………

9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.08	√
2	0.08V	Pin 7 to Pin 8	0.08	√
3	0.08V	Pin 11 to Pin 12	0.08	√
4	0.08V	Pin 15 to Pin 16	0.08	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	**Ch1 stable ?**	**Ch2 o/p**	**Ch2 stable ?**	**Ch3 o/p**	**Ch3 stable ?**	**Ch4 o/p**	**Ch4 stable ?**
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.4	√	-17.4	√	-17.4	√	-17.4	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.5	√	-2.5	√	-2.5	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.5	√	2.5	√	2.5	√
5v	12.2	√	12.2	√	12.2	√	12.2	√
7v	17.0	√	17.0	√	17.0	√	17.0	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Output @ 10Hz	Maximum o/p	@ Frequency
Channel 1	Channel 2			
Channel 2	Channel 1			
Channel 2	Channel 3			
Channel 3	Channel 2			
Channel 3	Channel 4			
Channel 4	Channel 3			

Unit.................OMC_9......................Serial No ....
Test Engineer.....Xen...........................
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13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.14	√
Ch2	**1.12v**	1.14	√
Ch3	**1.12v**	1.13	√
Ch4	**1.12v**	1.14	√

LIGO Laboratory / LIGO Scientific Collaboration

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OMC Coil Driver Board Test Plan

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

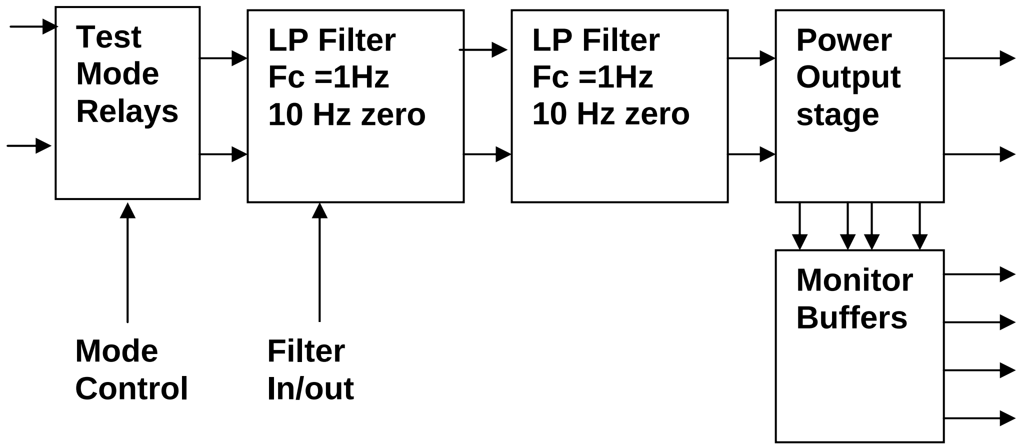
OMC COIL DRIVER BOARD
TEST PLAN

Unit……………….OMC_1……………………Serial No ………………………………
Test Engineer…..Xen………….……
Date……………..27/10/10……..……

Contents

1. Description

Block diagram



2. Description

Each OMC Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Unit……………...OMC_1……………………Serial No ………………………………
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	
Function Generator	Hitachi	VG-4429	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: √

C21 and C26 have been replaced by a 10nF polypropylene capacitor on all channels.

C200 has been soldered across R5 and R23 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

Unit………………OMC_1……………………Serial No ………………………………
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

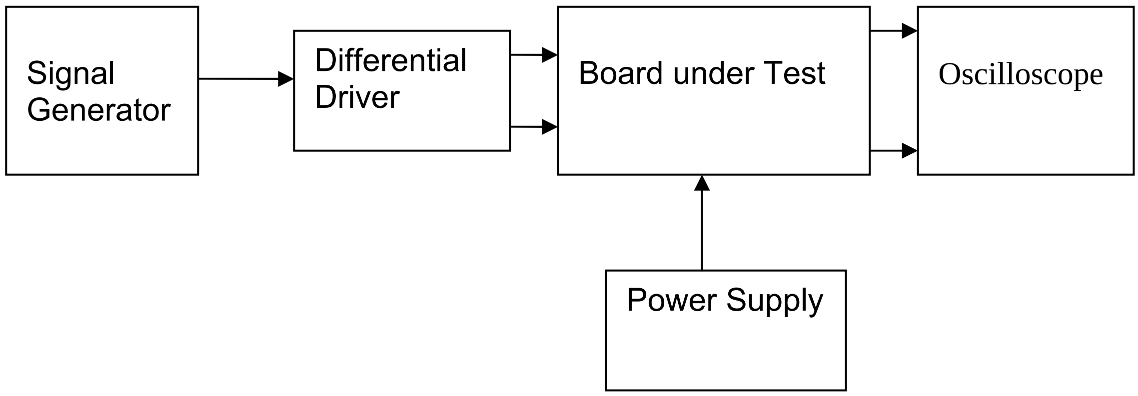
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit………………OMC_1……………………Serial No ………………………………
Test Engineer…..Xen………………
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6. Power

Check the polarity of the wiring:
3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.
Record regulator outputs:

Regulator	Output voltage	Output noise	Nominal +/- 0.5v?
+12v TP5	12.01	1mV	√
+15v TP4	14.96	2mV	√
-15v TP6	-15.03	10mV	√

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	350mA
-16.5v	450mA

If the supplies are correct, proceed to the next test.

Unit………………OMC_1……………………Serial No ………………………………
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Test Switches

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13 at 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.9	5.0	5.0	4.7v to 5v	√
Ch2	4.9	5.0	5.0	4.7v to 5v	√
Ch3	4.9	5.0	5.0	4.7v to 5v	√
Ch4	4.9	5.0	5.0	4.7v to 5v	√

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7 to 5v	√
Ch2	4.9	4.7 to 5v	√
Ch3	4.9	4.7 to 5v	√
Ch4	4.9	4.7 to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.4	3.3v to 3.7v	√
Ch2	3.4	3.3v to 3.7v	√
Ch3	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3v to 3.7v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.68	0.48 to 0.75v	√
Ch2	0.68	0.48 to 0.75v	√
Ch3	0.68	0.48 to 0.75v	√
Ch4	0.68	0.48 to 0.75v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.48	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.48	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.47	0.4v to 0.5v	√
Ch3	0.47	0.4v to 0.5v	√
Ch4	0.47	0.4v to 0.5v	√

Unit……………….OMC_1……………………Serial No ………………………………
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8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

	Output	Specification	Pass/Fail
Ch1	4.9	4.7v to 5v	√
Ch2	4.9	4.7v to 5v	√
Ch3	4.9	4.7v to 5v	√
Ch4	4.9	4.7v to 5v	√

1Hz

	Output	Specification	Pass/Fail
Ch1	3.2	3v to 3.4v	√
Ch2	3.2	3v to 3.4v	√
Ch3	3.2	3v to 3.4v	√
Ch4	3.2	3v to 3.4v	√

10Hz

	Output	Specification	Pass/Fail
Ch1	0.47	0.4v to 0.5v	√
Ch2	0.48	0.4v to 0.5v	√
Ch3	0.50	0.4v to 0.5v	√
Ch4	0.48	0.4v to 0.5v	√

100Hz

	Output	Specification	Pass/Fail
Ch1	0.16	0.15v to 0.16v	√
Ch2	0.16	0.15v to 0.16v	√
Ch3	0.16	0.15v to 0.16v	√
Ch4	0.16	0.15v to 0.16v	√

1 kHz

	Output	Specification	Pass/Fail
Ch1	0.15	0.14v to 0.16v	√
Ch2	0.15	0.14v to 0.16v	√
Ch3	0.15	0.14v to 0.16v	√
Ch4	0.15	0.14v to 0.16v	√

Unit………………OMC_1……………………Serial No ………………………………
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9. Monitor Outputs

Remove links W4 and W5.
Connect a 39 ohm dummy load to each channel.
Apply a 1V r.m.s input at 10Hz measured between TP10 and TP14, and record the differential output from each monitor pair on P1 for each channel. Compare them with the voltage outputs (TP9 to TP13).

Voltage monitors

Ch.	Nominal	Output between TP9 & TP13	Monitor Pins on P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.22V	1.22	Pin 1 to Pin 2	1.22	√
2	1.22V	1.22	Pin 5 to Pin 6	1.22	√
3	1.22V	1.22	Pin 9 to Pin 10	1.22	√
4	1.22V	1.22	Pin 13 to Pin 14	1.22	√

Current monitors

Ch.	Nominal	Monitor Pins	Monitor O/P	Pass/Fail: Equal? (+/- 0.1v)
1	0.08V	Pin 3 to Pin 4	0.079	√
2	0.08V	Pin 7 to Pin 8	0.079	√
3	0.08V	Pin 11 to Pin 12	0.079	√
4	0.08V	Pin 15 to Pin 16	0.079	√

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………..OMC_1……………………Serial No ………………………………
Test Engineer…..Xen………….……
Date……………..26/10/10……..……

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-24.5	√	-24.5	√	-24.5	√	-24.5	√
-7v	-17.5	√	-17.5	√	-17.5	√	-17.5	√
-5v	-12.5	√	-12.5	√	-12.5	√	-12.5	√
-1v	-2.5	√	-2.5	√	-2.4	√	-2.3	√
0v	0	√	0	√	0	√	0	√
1v	2.5	√	2.4	√	2.5	√	2.3	√
5v	12.5	√	12.0	√	12.5	√	12.3	√
7v	17.3	√	17.0	√	17.5	√	17.2	√
10v	24.5	√	24.5	√	24.5	√	24.5	√

Unit……………………………………Serial No ………………………………
Test Engineer……………………….……
Date…………………..…………………

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

Unit……………….OMC_1……………………Serial No ………………………………
Test Engineer…..Xen………….……
Date……………..26/10/10……..……

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.
Connect a 39 Ohm load resistor to the output of each channel. Switch out the filters. Apply a 10v peak sinusoidal signal at 10 Hz to the input. Check that the signal on TP10 is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

	Ch1	Ch2	Ch3	Ch4
Not Clipping?	√	√	√	√

	Theoretical o/p	Measured	OK+/- 0.1v?
Ch1	**1.12v**	1.1	√
Ch2	**1.12v**	1.1	√
Ch3	**1.12v**	1.1	√
Ch4	**1.12v**	1.1	√