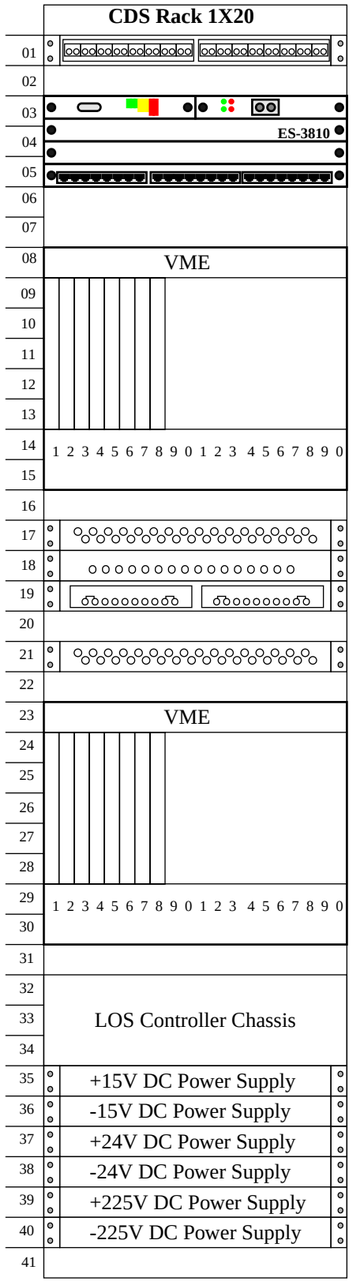

Rack Mount Components w/Locations

Loc	Description	Vendor	Model	Designator
01	Fiber Optic Patch Panel			FPP-1
03	Ethernet Switch w/ATM Uplink	Fore	ES-3810	ES-1
08	VME Crate	Knurr		VME-1
17	DAQS Interconnect Chassis (BNC)	LIGO		DAQIC-1
18	Accelerometer Signal Conditioner	Endevco		ACCSC-1
19	DAQS Interconnect Chassis (LEMO)	LIGO		DAQIC-2
21	GDS Interconnect Chassis (BNC)	LIGO		GDSIC-1
23	VME Crate	Knurr		VME-2
32	LOS Controller Chassis	LIGO		LOSC-1
35	+15VDC Power Supply	Sorenson		PS-1
36	-15VDC Power Supply	Sorenson		PS-2
37	+24VDC Power Supply	Sorenson		PS-3
38	-24VDC Power Supply	Sorenson		PS-4
39	+225VDC Power Supply	Sorenson		PS-5
40	-225VDC Power Supply	Sorenson		PS-6

Notes:
1) See referenced drawings for Timing, CDS Network and DAQS Network connections.
2) Suspension controls are detailed in a separate drawing (See TBD drawing)

VME-1 Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	MIPS Processor	Heurikon	4700	CPU-1
2	Reflected Memory	VMIC	5588DMA	RM-1
3	GPS Clock Master	Brandywine		GPS-1
4	Timing Clock Driver	LIGO		GPSCD-1
5	ADC	ICS	110B1	ADC1
6	Timing Clock Driver	LIGO		GPSCD-2
7	DAC	ICS	115	DAC1
8	Timing Clock Fanout	LIGO		GPSCF-1
9				
10				
11	68040 Processor	Motorola	MVME262	CPU-2
12				
13				
14				
15				

VME-2 Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	68040 Processor	Motorola	MVME262	CPU-1
2	ADC	VMIC	3113A	ADC1
3	DAC	VMIC	4116	DAC1
4	Relay Output Module	Xycom	220	RO1
5				

Reference Drawings

DWG Number	Description
D990083-C	Livingston Timing System Cable Diagram
D990084-C	Livingston DAQS Network Connections
D990085-C	Livingston Control and Monitoring Network

Revision History

REV	Date	Description
A	02/01/00	Initial Release

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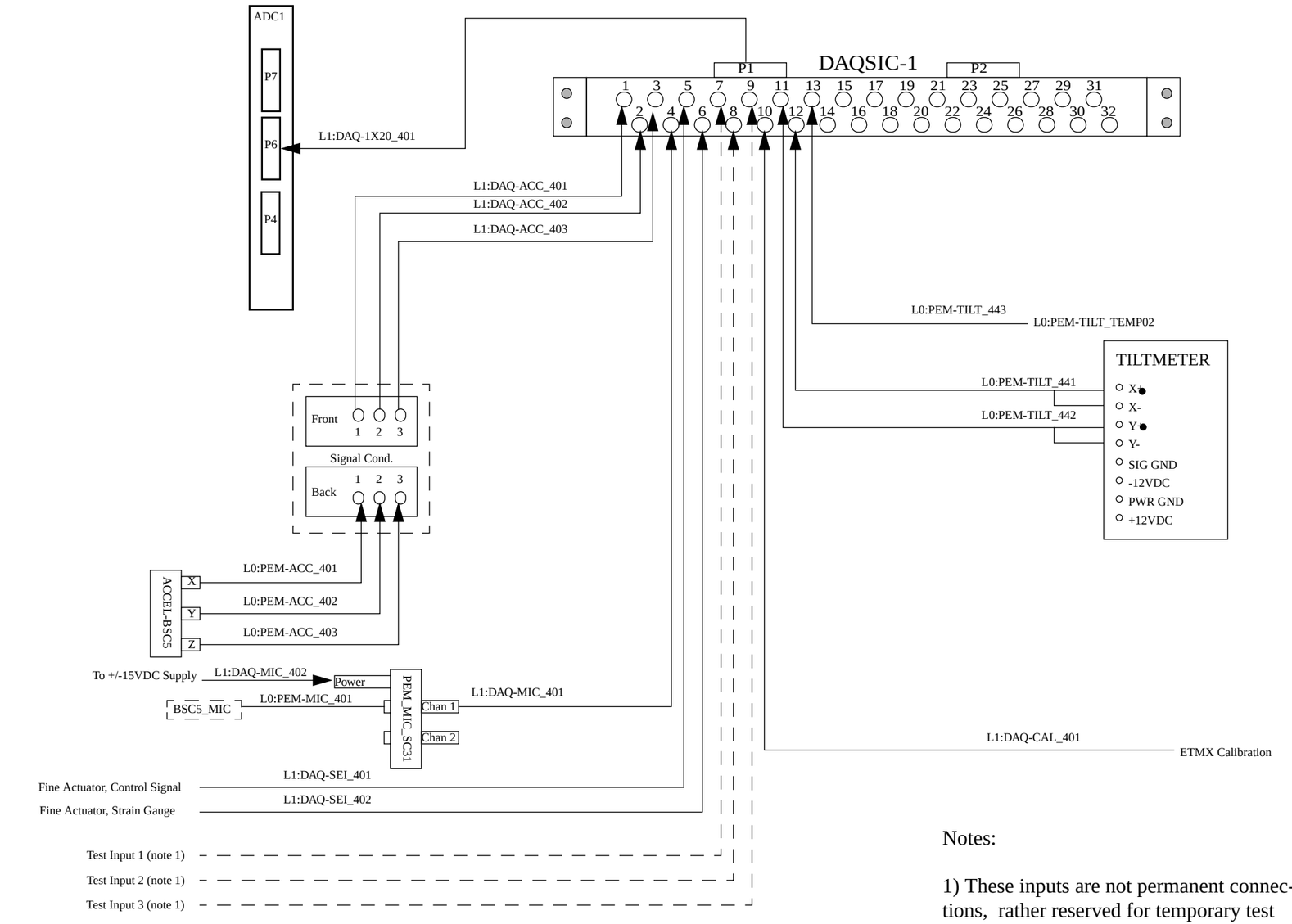
Livingston Rack Layout - 1X20
Chassis Layouts

Drawn By: R. Bork
Date: 1/31/00
Dwg. No. D990183-A-C
Sheet 1 of 3

Chan	Name	Rate
00	L0:PEM-BSC5_ACCX	2048
01	L0:PEM-BSC5_ACCY	2048
02	L0:PEM-BSC5_ACCZ	2048
03	L0:PEM-BSC5_MIC	2048
04	L1:SEI-BSC5_FINE1	256
05	L1:SEI-BSC5_FINE2	256
06	L0:GDS-EX_TO1	16384
07	L0:GDS-EX_TO2	2048
08	L0:GDS-EX_TO3	2048
09	L1:LSC-ETMX_CAL	16384
10	L0:PEM-EX_TILTX	256
11	L0:PEM-EX_TILTY	256
12	L0:PEM-EX_TEMP2	16
13		
14		
15		
16	L1:-SUS-BSC5_SENSOR_SIDE	256
17	L0:PEM-EX_SEISZ	256
18	L1:SUS-BSC5_COIL_UL	2048
19	L1:SUS-BSC5_COIL_LL	2048
20	L1:-SUS-BSC5_COIL_UR	2048
21	L1:-SUS-BSC5_COIL_LR	2048
22	L1:-SUS-BSC5_COIL_SIDE	2048
23	L1:-SUS-BSC5_COIL_SUM	16384
24	L1:SUS-BSC5_SENSOR_UL	256
25	L1:SUS-BSC5_SENSOR_LL	256
26	L1:-SUS-BSC5_SENSOR_UR	256
27	L1:-SUS-BSC5_SENSOR_LR	256
28	L0:PEM-EX_SEISX	256
29	L0:PEM-EX_SEISY	256
30	L1:GDS-EX_RAMP1	16384
31	L1:GDS-EX_TRIG1	16384



Notes:

1) These inputs are not permanent connections, rather reserved for temporary test inputs.
2) See following sheet for connection of channels 16-31.

Reference Drawings

DWG Number	Description

Revision History

REV	Date	Description

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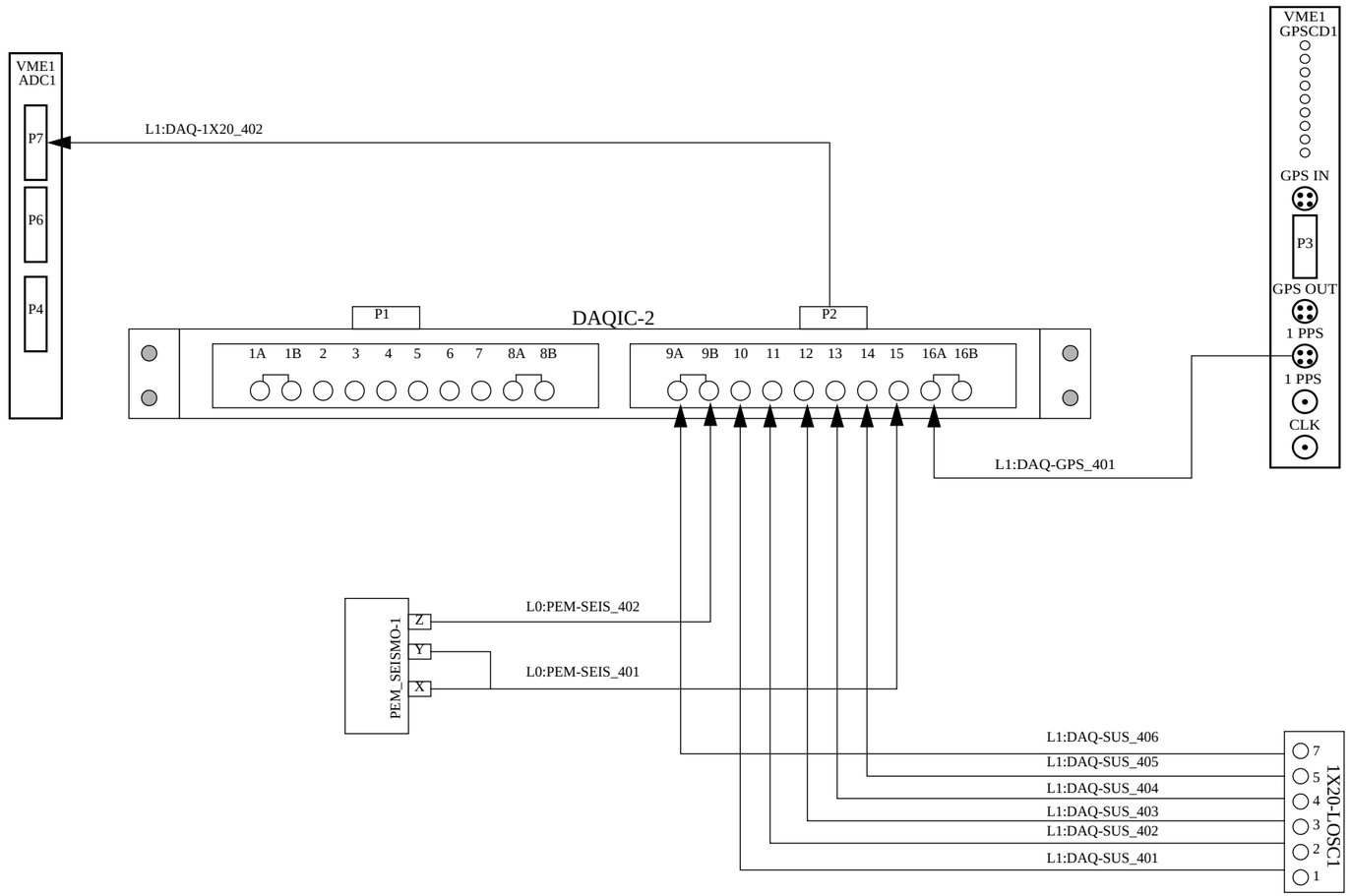
Livingston CDS Rack Layout - 1X20 DAQIC-1 Connections

Drawn By: R. Bork

Dwg. No. D990183-A-C

Date: 1/31/00

Sheet 2 of 3



Reference Drawings	
DWG Number	Description

Revision History		
REV	Date	Description

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Livingston CDS Rack Layout - 1X20
DAQS Interconnect Chassis
(1X20_DAQIC-2)

Drawn By: R. Bork	Dwg. No. D990183-A-C
Date: 1/31/00	Sheet 3 of 3