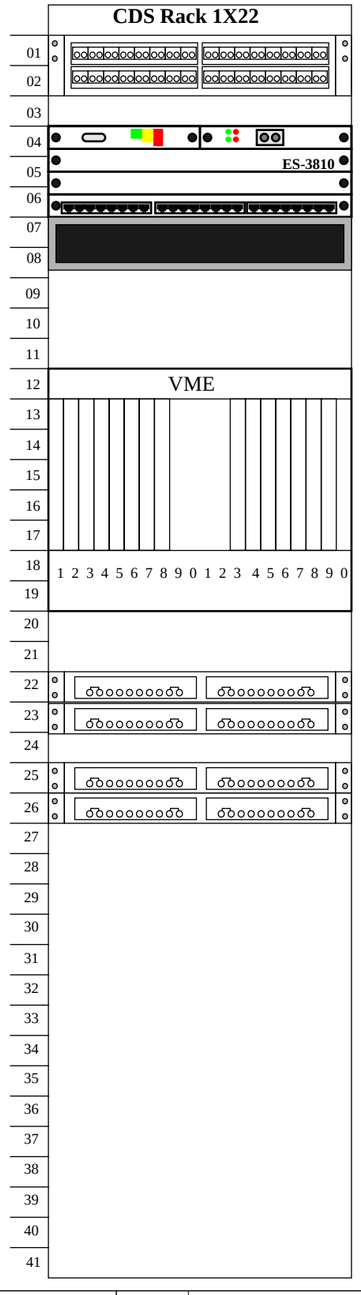

Rack Mount Components w/Locations

Loc	Description	Vendor	Model	Designator
01	Multi-Mode Fiber Optic Patch Panel	Anexder		FPP-1
06	Ethernet Switch w/ATM Uplink	Fore	ES-3810	ES-1
07	Cable routing panduit	Panduit		CRP-1
12	VME Crate	Knurr		VME-1
22	DAQS Interconnect Chassis	LIGO		DAQSIC-1
23	DAQS Interconnect Chassis	LIGO		DAQSIC-2
25	DAQS Interconnect Chassis	LIGO		DAQSIC-3
26	DAQS Interconnect Chassis	LIGO		DAQSIC-4

VME Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	MIPS Processor	Heurikon	4700	uP-1
2	MIPS Processor	Heurikon	4700	uP-2
3	Reflected Memory	VMIC	5588DMA	RM-1
4				
5	GPS Clock Master Receiver	Brandywing		GPS-1
6	GPS Clock Fanout	LIGO		GPSCF-1
7	GPS Clock Driver	LIGO		GPSCD-1
8	ADC	ICS	110B1	ADC-1
9	ADC	ICS	110B1	ADC-2
10	ADC	ICS	110B1	ADC-3
11	ADC	ICS	110B1	ADC-4
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FINISHED SURFACE RMS
BREAK CORNERS ON OUT.
REMOVE ALL BURRS

DO NOT SCALE THIS DRAWING

USED ON:

NEXT ASS'Y:

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION
REFERENCE DRAWINGS			

REV	DESCRIPTION	SHEETS EFFECTED	DATE
ISSUE DESCRIPTION			

CURRENT REVISION APPROVAL

		GROUP	SIGNATURE	DATE
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CHECKED				
		DCC		

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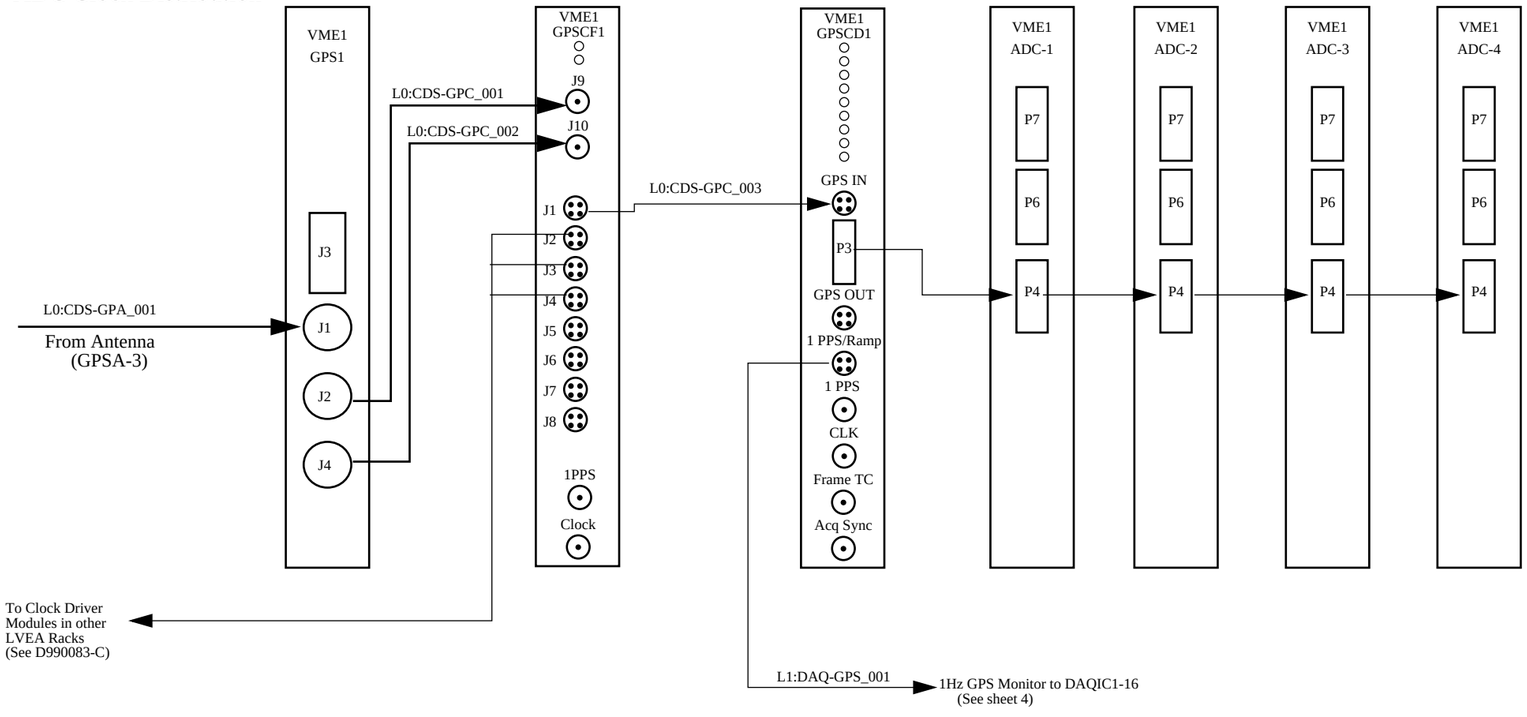
Livingston CDS Rack Layout - 1X22 Chassis Layouts

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 1 of 7	STD	VER. 01

6 5 4 3 2 1

ADC Clock Distribution



	D990083-C	Livingston Timing System Cable Diagram			UNLESS OTHERWISE SPECIFIED					CURRENT REVISION APPROVAL			
					DIMENSIONS ARE IN INCHES					DRAWN R. Bork	GROUP	SIGNATURE	DATE 4/6/99
					TOLERANCES: FRACTIONAL ± ANGULAR MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS IN OUT: REMOVE ALL BURRS					CHECKED			
					DO NOT SCALE THIS DRAWING	REV	DESCRIPTION	SHEETS EFFECTED	DATE				
	DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION	USED ON:						DCC		
	REFERENCE DRAWINGS				NEXT ASS'Y:	ISSUE DESCRIPTION							

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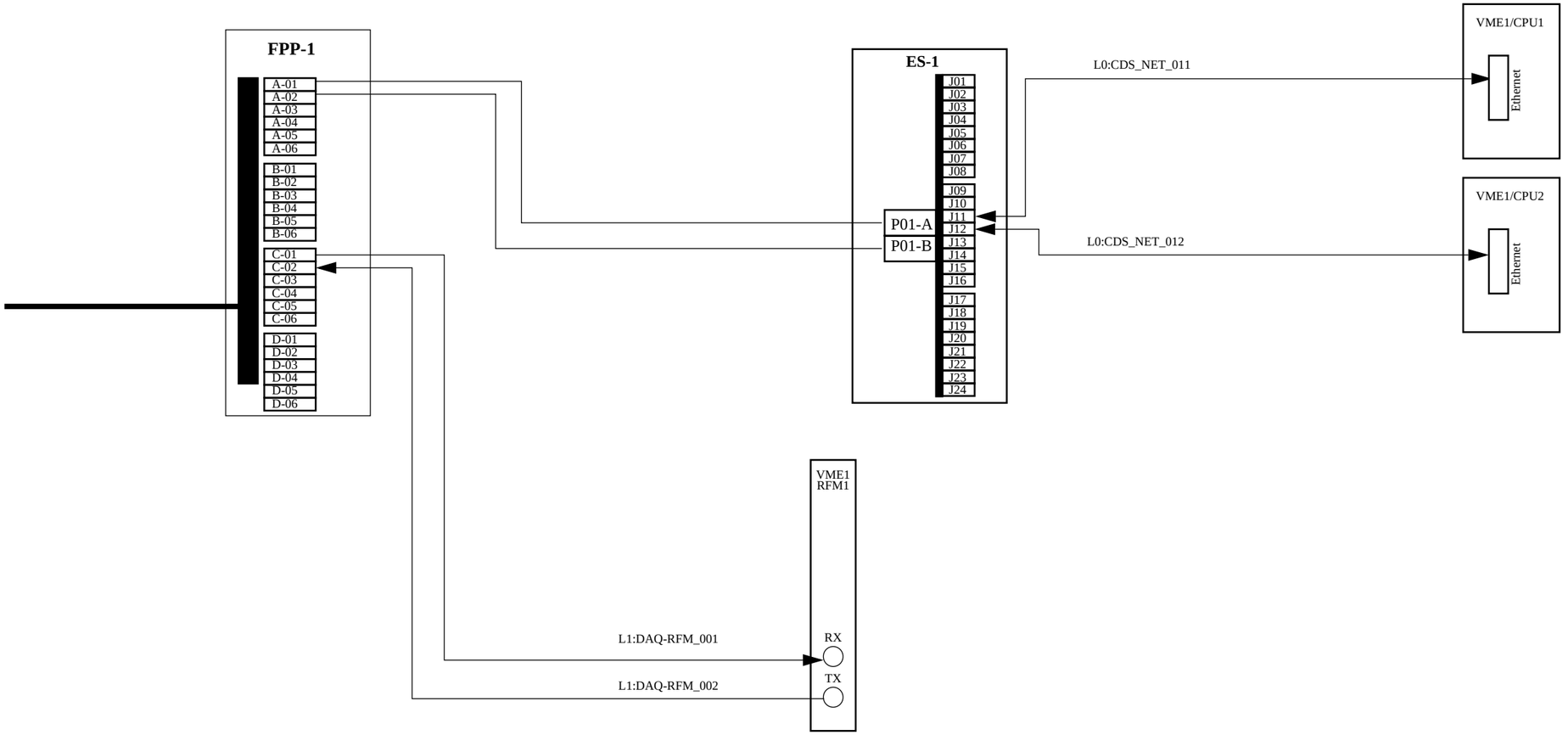
Livingston CDS Rack Layout - 1X22
Timing System Connections

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 2 of 7	STD	VER. D1

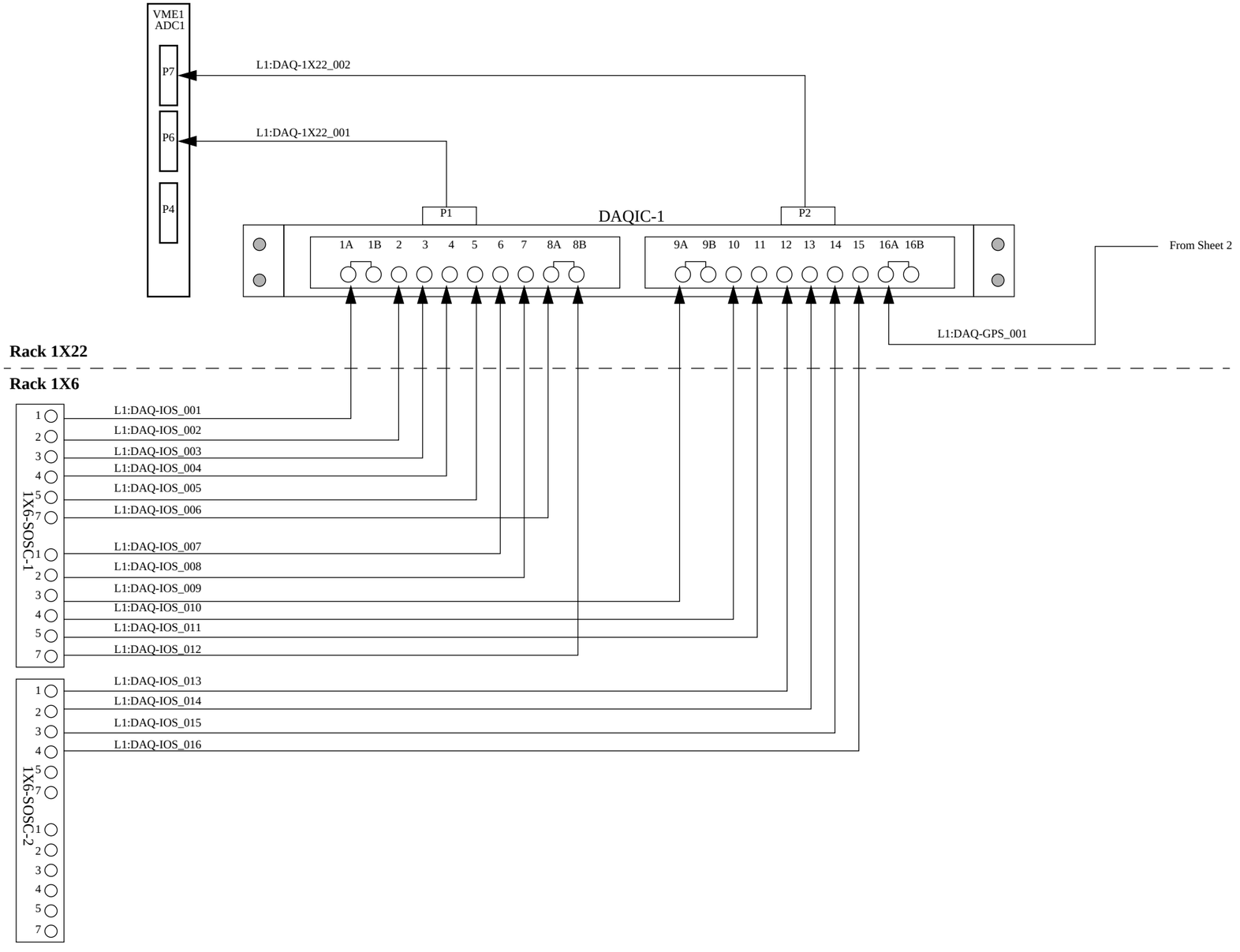
6 5 4 3 2 1



D990085-C	Livingston CDS Network			UNLESS OTHERWISE SPECIFIED					CURRENT REVISION APPROVAL				LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY
D990084-C	Livingston DAQ Network			DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS ON OUT: REMOVE ALL BURRS					DRAWN R. Bork	GROUP	SIGNATURE	DATE 4/6/99	Livingston CDS Rack Layout - 1X22 CDS & DAQS Networking Connections
									CHECKED				
				DO NOT SCALE THIS DRAWING									SCALE / SIZE B / DWG. NO. D990162-00-C / REV.
DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION	USED ON:	REV	DESCRIPTION	SHEETS EFFECTED	DATE		DCC			CAD FILE / SCALE / SHEET 3 of 7 / STD / VER. D1
REFERENCE DRAWINGS				NEXT ASS'Y:	ISSUE DESCRIPTION								

6 5 4 3 2 1

Chan	Name	Rate
00	L1:SUS-MC1_COIL_UL	2048
01	L1:SUS-MC1_COIL_LL	2048
02	L1:-SUS-MC1_COIL_UR	2048
03	L1:-SUS-MC1_COIL_LR	2048
04	L1:-SUS-MC1_COIL_SIDE	2048
05	L1:-SUS-MC1_COIL_SUM	16384
06	L1:-SUS-MC1_SENSOR_UL	256
07	L1:-SUS-MC1_SENSOR_LL	256
08	L1:-SUS-MC1_SENSOR_UR	256
09	L1:-SUS-MC1_SENSOR_LR	256
10	L1:SUS-MC2_COIL_UL	2048
11	L1:SUS-MC2_COIL_LL	2048
12	L1:-SUS-MC2_COIL_UR	2048
13	L1:-SUS-MC2_COIL_LR	2048
14	L1:SUS-MC1_SENSOR_SIDE	256
15	L1:SUS-MC2_SENSOR_SIDE	256
16	L1:-SUS-MC2_COIL_SIDE	2048
17	L1:-SUS-MC2_COIL_SUM	16384
18	L1:-SUS-MC2_SENSOR_UL	256
19	L1:-SUS-MC2_SENSOR_LL	256
20	L1:-SUS-MC2_SENSOR_UR	256
21	L1:-SUS-MC2_SENSOR_LR	256
22	L1:SUS-MC3_COIL_UL	2048
23	L1:SUS-MC3_COIL_LL	2048
24	L1:-SUS-MC3_COIL_UR	2048
25	L1:-SUS-MC3_COIL_LR	2048
26	L1:-SUS-MC3_COIL_SIDE	2048
27	L1:-SUS-MC3_COIL_SUM	16384
28	L1:-SUS-MC3_SENSOR_UL	256
29	L1:-SUS-MC3_SENSOR_LL	256
30	L1:GDS-GPS_RAMP1	16384
31	L1:GDS--GPS_TRIG1	16384
	TOTAL (BTYES/SEC)	**231424**



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FINISHED SURFACE RMS
BREAK CORNERS IN OUT:
REMOVE ALL BURRS

DO NOT SCALE THIS DRAWING

USED ON:

NEXT ASS'Y:

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION
REFERENCE DRAWINGS			

REV	DESCRIPTION	SHEETS EFFECTED	DATE
ISSUE DESCRIPTION			

CURRENT REVISION APPROVAL

		GROUP	SIGNATURE	DATE
DRAWN	R. Bork			4/6/99
CHECKED				
		DCC		

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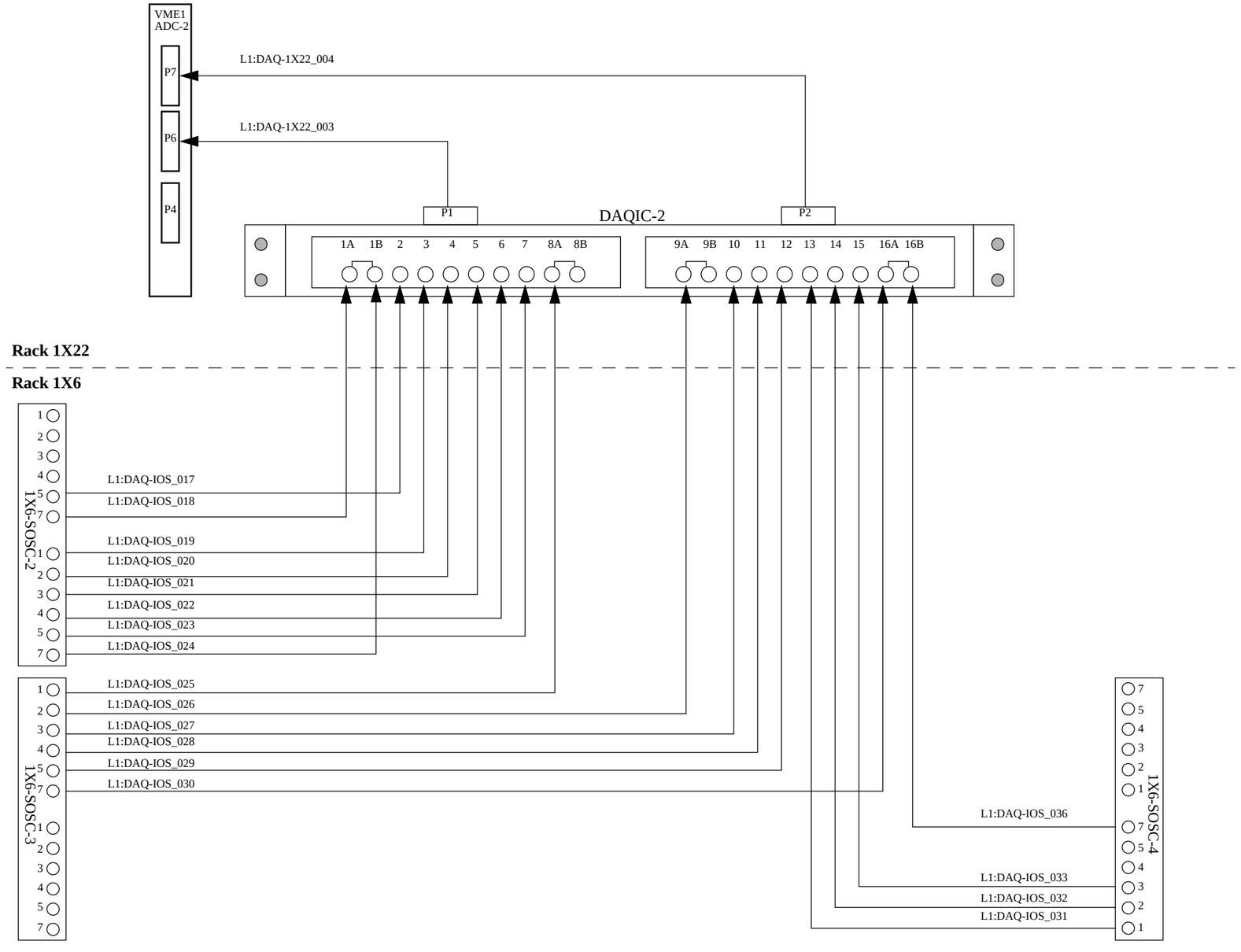
Livingston CDS Rack Layout - 1X22
DAQS Interconnect Chassis
(1X22_DAQIC-1)

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 4 of 7	STD	VER. D1

6 5 4 3 2 1

Chan	Name	Rate
00	L1:SUS-MC3_SENSOR_SIDE	256
01	L1:SUS-SM1_SENSOR_SIDE	256
02	L1:-SUS-MC3_SENSOR_UR	256
03	L1:-SUS-MC3_SENSOR_LR	256
04	L1:SUS-SM1_COIL_UL	2048
05	L1:SUS-SM1_COIL_LL	2048
06	L1:-SUS-SM1_COIL_UR	2048
07	L1:-SUS-SM1_COIL_LR	2048
08	L1:-SUS-SM1_COIL_SIDE	2048
09	L1:-SUS-SM1_COIL_SUM	16384
10	L1:-SUS-SM1_SENSOR_UL	256
11	L1:-SUS-SM1_SENSOR_LL	256
12	L1:-SUS-SM1_SENSOR_UR	256
13	L1:-SUS-SM1_SENSOR_LR	256
14	L1:SUS-MMT1_COIL_UL	2048
15	L1:SUS-MMT1_COIL_LL	2048
16	L1:-SUS-MMT1_COIL_UR	2048
17	L1:-SUS-MMT1_COIL_LR	2048
18	L1:-SUS-MMT1_COIL_SIDE	2048
19	L1:-SUS-MMT1_COIL_SUM	16384
20	L1:-SUS-MMT1_SENSOR_UL	256
21	L1:-SUS-MMT1_SENSOR_LL	256
22	L1:-SUS-MMT1_SENSOR_UR	256
23	L1:-SUS-MMT1_SENSOR_LR	256
24	L1:SUS-MMT2_COIL_UL	2048
25	L1:SUS-MMT2_COIL_LL	2048
26	L1:-SUS-MMT2_COIL_UR	2048
27	L1:-SUS-MMT2_COIL_LR	2048
28	L1:-SUS-MMT2_COIL_SIDE	2048
29	L1:-SUS-MMT2_COIL_SUM	16384
30	L1:SUS-MMT1_SENSOR_SIDE	256
31	L1:SUS-MMT2_SENSOR_SIDE	256
	TOTAL (BTYES/SEC)	**166912**



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FINISHED SURFACE RMS
BREAK CORNERS ON OUT.
REMOVE ALL BURRS

DO NOT SCALE THIS DRAWING

USED ON:

NEXT ASS'Y:

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION

REFERENCE DRAWINGS

REV	DESCRIPTION	SHEETS EFFECTED	DATE

ISSUE DESCRIPTION

CURRENT REVISION APPROVAL

		GROUP	SIGNATURE	DATE
DRAWN	R. Bork			4/6/99
CHECKED				
		DCC		

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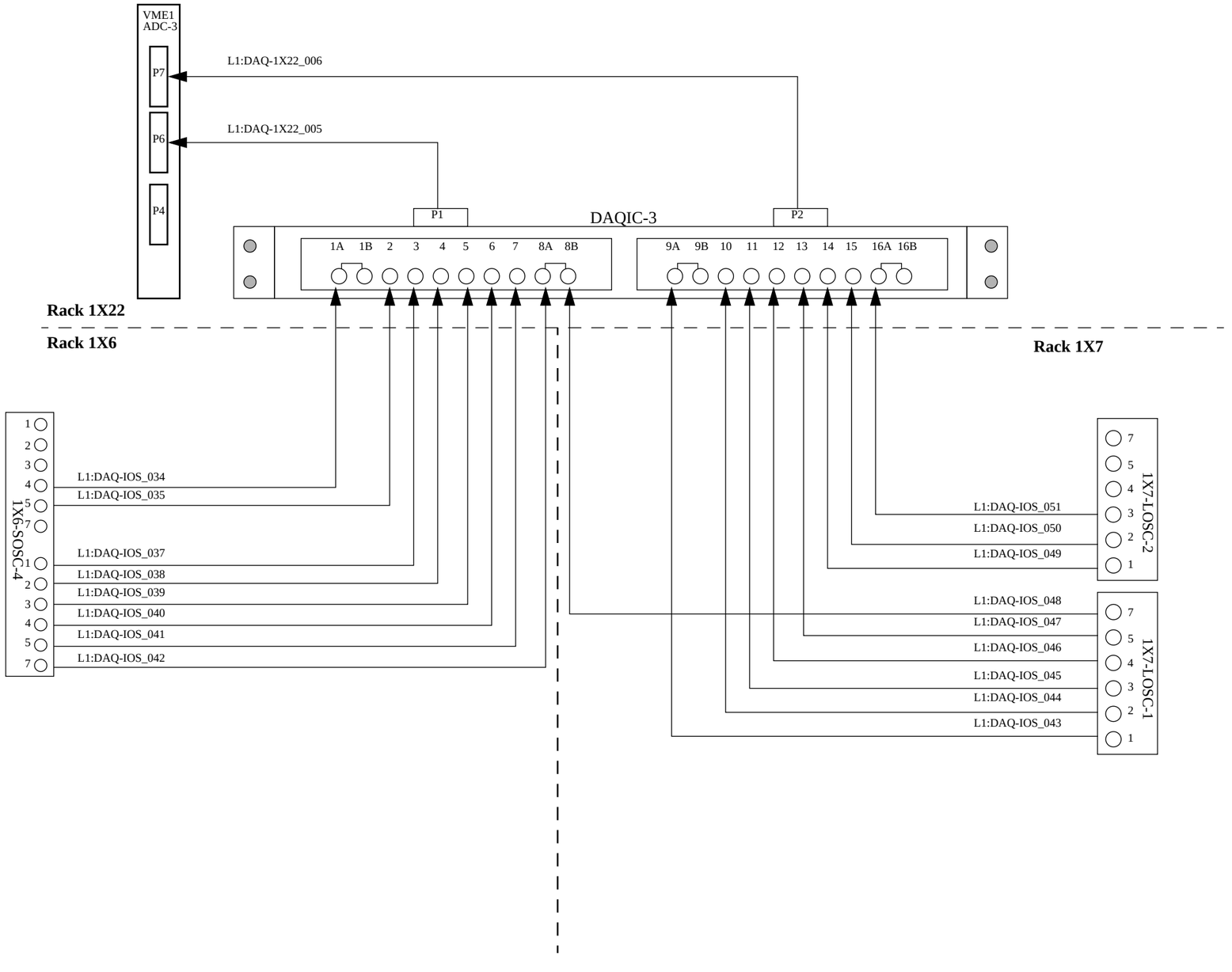
Livingston CDS Rack Layout - 1X22 DAQS Interconnect Chassis (1X22_DAQIC-2)

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 5 of 7	STD	VER. D1

6 5 4 3 2 1

Chan	Name	Rate
00	L1:-SUS-MMT2_SENSOR_UL	256
01	L1:-SUS-MMT2_SENSOR_LL	256
02	L1:-SUS-MMT2_SENSOR_UR	256
03	L1:-SUS-MMT2_SENSOR_LR	256
04	L1:SUS-MMT3_COIL_UL	2048
05	L1:SUS-MMT3_COIL_LL	2048
06	L1:-SUS-MMT3_COIL_UR	2048
07	L1:-SUS-MMT3_COIL_LR	2048
08	L1:-SUS-MMT3_COIL_SIDE	2048
09	L1:-SUS-MMT3_COIL_SUM	16384
10	L1:-SUS-MMT3_SENSOR_UL	256
11	L1:-SUS-MMT3_SENSOR_LL	256
12	L1:-SUS-MMT3_SENSOR_UR	256
13	L1:-SUS-MMT3_SENSOR_LR	256
14	L1:SUS-MMT3_SENSOR_SIDE	256
15	L1:-SUS-RCM_SENSOR_SIDE*	256
16	L1:SUS-RCM_COIL_UL	2048
17	L1:SUS-RCM_COIL_LL	2048
18	L1:-SUS-RCM_COIL_UR	2048
19	L1:-SUS-RCM_COIL_LR	2048
20	L1:-SUS-RCM_COIL_SIDE	2048
21	L1:-SUS-RCM_COIL_SUM	16384
22	L1:SUS-RCM_SENSOR_UL	256
23	L1:SUS-RCM_SENSOR_LL	256
24	L1:-SUS-RCM_SENSOR_UR	256
25	L1:-SUS-RCM_SENSOR_LR	256
26	L1:SUS-BSM_COIL_UL	2048
27	L1:SUS-BSM_COIL_LL	2048
28	L1:-SUS-BSM_COIL_UR	2048
29	L1:-SUS-BSM_COIL_LR	2048
30	L1:-SUS-BSM_COIL_SIDE	2048
31	L1:-SUS-BSM_COIL_SUM	16384
	TOTAL (BTYES/SEC)	**166912**



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR MACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FINISHED SURFACE RMS
BREAK CORNERS ON OUT:
REMOVE ALL BURRS

DO NOT SCALE THIS DRAWING

USED ON:

NEXT ASS'Y:

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION
REFERENCE DRAWINGS			

REV	DESCRIPTION	SHEETS EFFECTED	DATE
ISSUE DESCRIPTION			

CURRENT REVISION APPROVAL

		GROUP	SIGNATURE	DATE
DRAWN	R. Bork			4/6/99
CHECKED				
		DCC		

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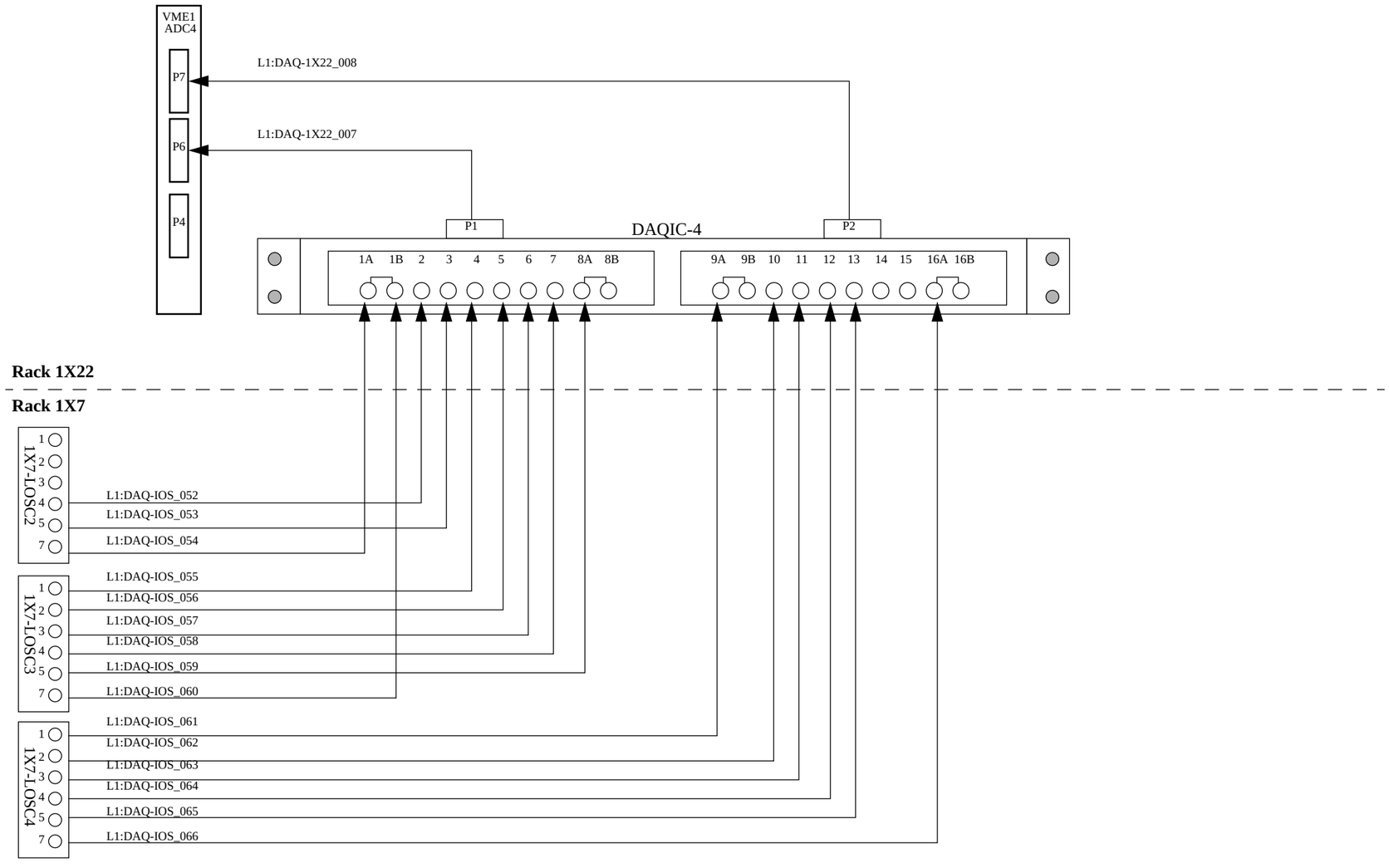
Livingston CDS Rack Layout - 1X22
DAQS Interconnect Chassis
(1X22_DAQIC-3)

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 6 of 7 STD		VER. D1

6 5 4 3 2 1

Chan	Name	Rate
00	L1:-SUS-BSM_SENSOR_SIDE*	256
01	L1:SUS-ITMX_SENSOR_SIDE	256
02	L1:SUS-BSM_SENSOR_UL	256
03	L1:SUS-BSM_SENSOR_LL	256
04	L1:-SUS-BSM_SENSOR_UR	256
05	L1:-SUS-BSM_SENSOR_LR	256
06	L1:SUS-ITMX_COIL_UL	2048
07	L1:SUS-ITMX_COIL_LL	2048
08	L1:-SUS-ITMX_COIL_UR	2048
09	L1:-SUS-ITMX_COIL_LR	2048
10	L1:-SUS-ITMX_COIL_SIDE	2048
11	L1:-SUS-ITMX_COIL_SUM	16384
12	L1:-SUS-ITMX_SENSOR_UL	256
13	L1:-SUS-ITMX_SENSOR_LL	256
14	L1:-SUS-ITMX_SENSOR_UR	256
15	L1:-SUS-ITMX_SENSOR_LR	256
16	L1:SUS-ITMY_COIL_UL	2048
17	L1:SUS-ITMY_COIL_LL	2048
18	L1:-SUS-ITMY_COIL_UR	2048
19	L1:-SUS-ITMY_COIL_LR	2048
20	L1:-SUS-ITMY_COIL_SIDE	2048
21	L1:-SUS-ITMY_COIL_SUM	16384
22	L1:-SUS-ITMY_SENSOR_UL	256
23	L1:-SUS-ITMY_SENSOR_LL	256
24	L1:-SUS-ITMY_SENSOR_UR	256
25	L1:-SUS-ITMY_SENSOR_LR	256
26		
27		
28		
29		
30	L1:SUS-ITMY_SENSOR_SIDE	256
31		
	TOTAL (BTYES/SEC)	**114176**



UNLESS OTHERVISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULARMACH ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FONISHED SURFACE RMS
BREAK CORNERS IN OUT.
REMOVE ALL BURRS

DO NOT SCALE THIS DRAWING

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NEXT ASS'Y:

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION
REFERENCE DRAWINGS			

REV	DESCRIPTION	SHEETS EFFECTED	DATE
ISSUE DESCRIPTION			

CURRENT REVISION APPROVAL

		GROUP	SIGNATURE	DATE
DRAWN	R. Bork			4/6/99
CHECKED				
		DCC		

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Livingston CDS Rack Layout - 1X22
DAQS Interconnect Chassis
(1X22_DAQIC-4)

SCALE	SIZE	DWG. NO.	REV.
	B	D990162-00-C	
CAD FILE SCALE	SHEET 7 of 7 STD		VER. D1

6 5 4 3 2 1