VME SLAVE INTERFACE

page 3 of 6
8036902K.SCH

DTACK*
IACK*
WRITE*
DS0*
SYSRESET*
AM0
AM1
AM3
AM4
AM5
A13
A14
A15
D00
D01
D02
D03
D04
D05
D06
D07

CLK ENABLE
1PPS_SYNC
BRESET
1PPS ENABLE
CLK_SYNC
AS
ERESET
SYNC_ERROR

MAIN TIMING

Page 2 of 6
8036901K.SCH

1_PPS
CLK ENABLE
1PPS_SYNC
BRESET
1PPS ENABLE
CLK_SYNC
AS
CLOCK
S_1PPS
CLK_HI
FTC
AS'

INDEPENDENT TIMING

Page 4 of 6
8036903K.SCH

1_PPS

DIAGNOSTICS

Page 5 of 6
8036904K.SCH

1_PPS
CLOCK
S_1PPS
CLK_HI
FTC
AS'
CLK ENABLE
1PPS ENABLE
CLK_SYNC
AS
ERESET
SYNC_ERROR

TIMING DIAGRAM

Page 6 of 6
8036905K.SCH

P1

D00	1A	1B		1C	
D01	2A	2B		2C	
D02	3A	3B		3C	
D03	4A	4B		4C	
D04	5A	5B	BG0IN*	5C	
D05	6A	6B	BG0OUT*	6C	
D06	7A	7B	BG1IN*	7C	
D07	8A	8B	BG1OUT*	8C	
GND	9A	9B	BG2IN*	9C	GND
	10A	10B	BG2OUT*	10C	
GND	11A	11B	BG3IN*	11C	
	12A	12B	BG3OUT*	12C	SYSRESET*
DS0*	13A	13B		13C	
WRITE*	14A	14B		14C	AM5
GND	15A	15B		15C	
DTACK*	16A	16B	AM0	16C	
GND	17A	17B	AM1	17C	
	18A	18B	AM2	18C	
GND	19A	19B	AM3	19C	
IACK*	20A	20B	GND	20C	
IACKIN*	21A	21B		21C	
IACKOUT*	22A	22B		22C	
	23A	23B	GND	23C	A15
AM4	24A	24B		24C	A14
	25A	25B		25C	A13
	26A	26B		26C	
	27A	27B		27C	
	28A	28B		28C	
	29A	29B		29C	
	30A	30B		30C	
-12V	31A	31B		31C	+12V
+5V	32A	32B	+5V	32C	+5V

DIN96

P2

	1A	1B		1C	
	2A	2B		2C	
	3A	3B		3C	
	4A	4B		4C	
	5A	5B		5C	
	6A	6B		6C	
	7A	7B		7C	
	8A	8B		8C	
	9A	9B		9C	
	10A	10B		10C	
	11A	11B		11C	
	12A	12B		12C	
	13A	13B		13C	
	14A	14B		14C	
	15A	15B		15C	
	16A	16B		16C	
	17A	17B		17C	
	18A	18B		18C	
	19A	19B		19C	
	20A	20B		20C	
	21A	21B		21C	
	22A	22B		22C	
	23A	23B		23C	
	24A	24B		24C	
	25A	25B		25C	
	26A	26B		26C	
	27A	27B		27C	
	28A	28B		28C	
	29A	29B		29C	
	30A	30B		30C	
	31A	31B		31C	
	32A	32B		32C	

DIN96

+12V — 30 mA — C3 10uF — GND

-12V — 160 mA — C1 10uF — GND

U1 LM320T-5 (GND, Vin, -5V)

TP1 VEE — VEE

C46 1uF; C13, C14, C15, C16 0.1uF

+5V — 580 mA — EMI1 P9832CT — C2 10uF — GND

C45 1uF; C6, C7, C8, C9, C10, C11, C12, C17, C18, C19, C20, C21, C22, C23 0.1uF

TP2 VCC — VCC

C31, C32, C33, C34, C35, C36, C37, C40 0.1uF

C24, C25, C26, C27, C28, C29, C30, C38, C39 0.1uF

TP3 GND, TP4 GND, TP5 GND, TP6 GND, TP7 GND

Date Last Modified:	*18-Oct-99*
Title	***GPS Clock Driver***
Size: B	DCC Number: D980369-11-C
PCB / SCH Revision:	C / 11
Engineer:	*D. Ouimette*
Date:	19-Oct-1999
Time:	08:42:21
Sheet	1 of 6
File:	S:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036900K.prj

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
LIGO

Clock Polarity

Clock polarity shown for jumper JP1 installed.

JP1 · R14 1.00K · U3A 74F04 · TP12 POL · U15B 74F86 · CLK_HI *to page 5*

U2F 74F04 · U15A 74F86

TP8 PEN · *from page 3* 1PPS ENABLE

TP9 CEN · *from page 3* CLK ENABLE

U17A DM74S140 · CLOCK_HI · TP13 CLK · R26 1K · P3 20PIN

U17B DM74S140 · CLOCK_LO

U18A DM74S140 · FS · TP15 AS · TP14 FS · JP3 Driver Function

U18B DM74S140 · AS

to page 4 & 5 1_PPS

to page 5 CLOCK

R3 475 · R4 475 · R5 475 · R6 475 · U21A MC10H124 · U21B MC10H124

JP4 Enable Select · R27 1K

J2 LEMO 4PIN · GPS OUT ECL

TP11 CS · *to page 3 & 5* CLK_SYNC

to page 5 FTC

50 ns Delay DL-1 DDU8F-5250 · *to page 3 & 5* AS

from page 3 BRESET

U16 74ALS867 · TC · U2C 74F04

C53 470pF · R11 100

1 PPS REFERENCE

MC10H115 · MC10H125 · U11B · U12B · R8 100 · R2 475

U7B 74F74 · TP10 PS · *to page 3* 1PPS_SYNC

U2E 74F04 · R10 100 · C51 100pF · U14A 74F32

Delay to ensure setup time to load counter via RESET

U8A 74F74

J1 LEMO 4PIN · GPS IN

U7A 74F74 · U5A 74F08

U2B 74F04 · R7 100 · C50 100pF · U2D 74F04 · U13A 74F00

25ns delay pulse to follow TC

U11A · U12A · R9 100 · R1 475

U2A 74F04

U5B 74F08

Shift Register

U22 74LS164 · JP2 Delay Select

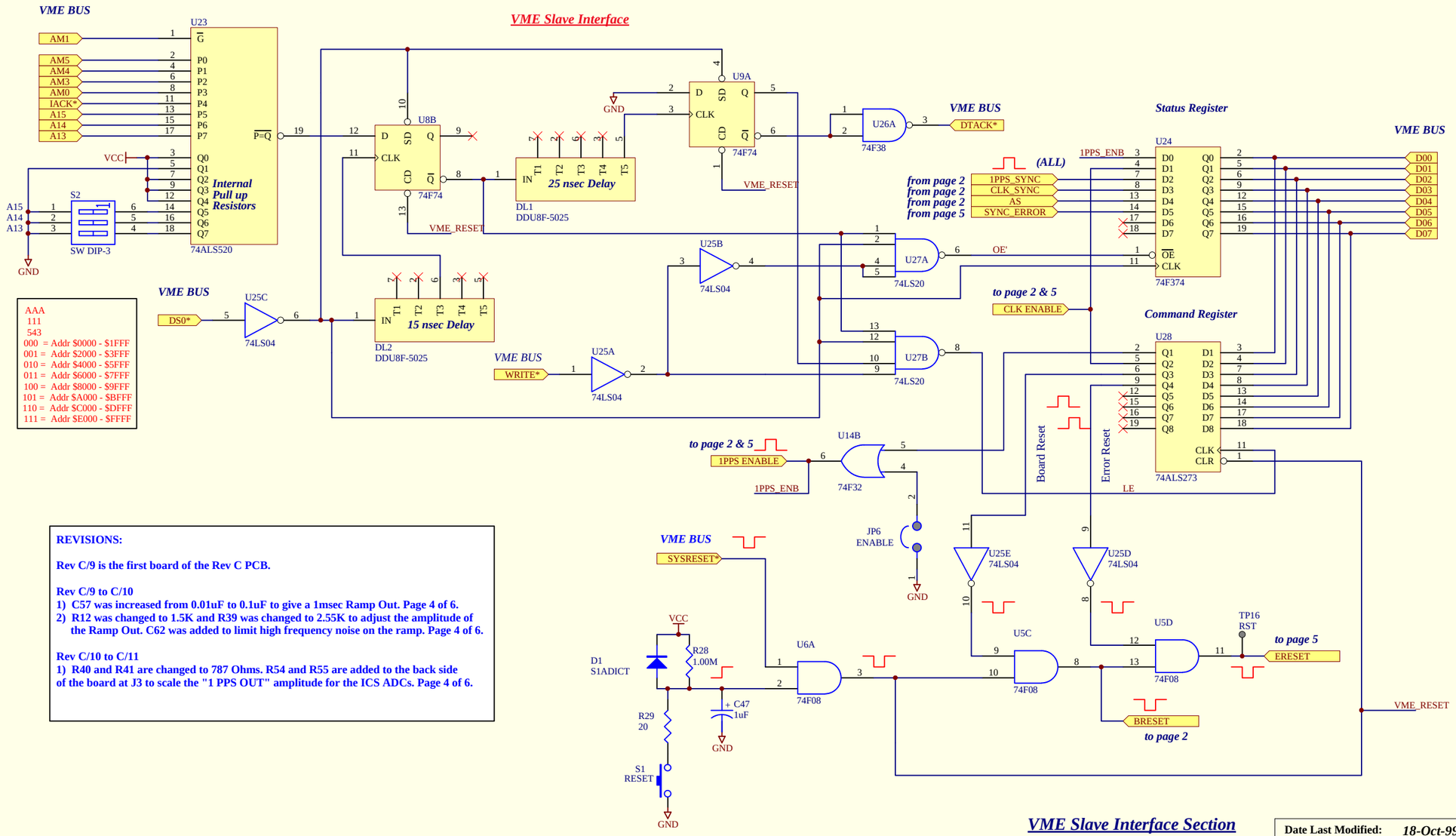
to page 5 S_1PPS

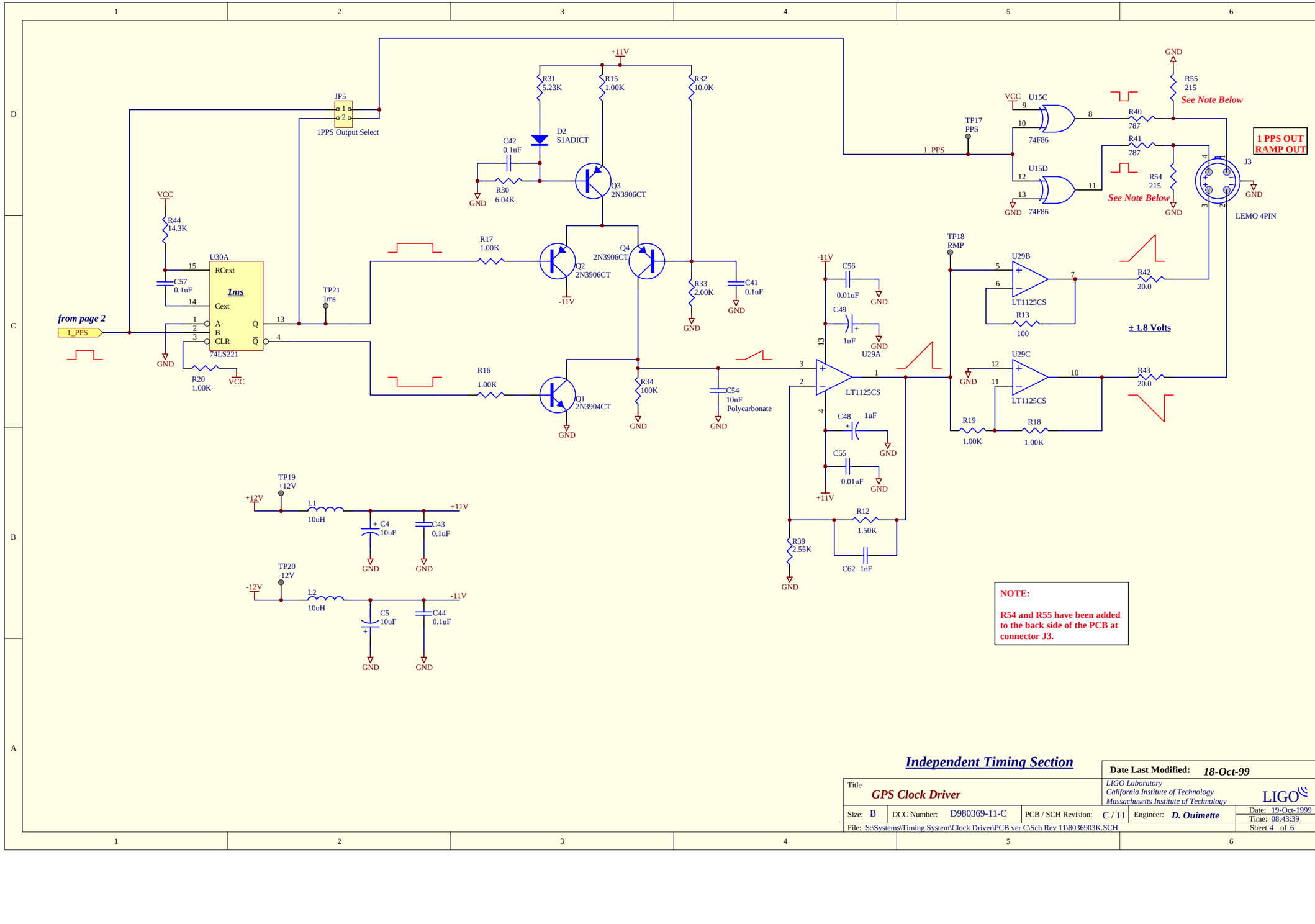
2^22 Hz CLOCK

Main Timing Section

Date Last Modified: *18-Oct-99*

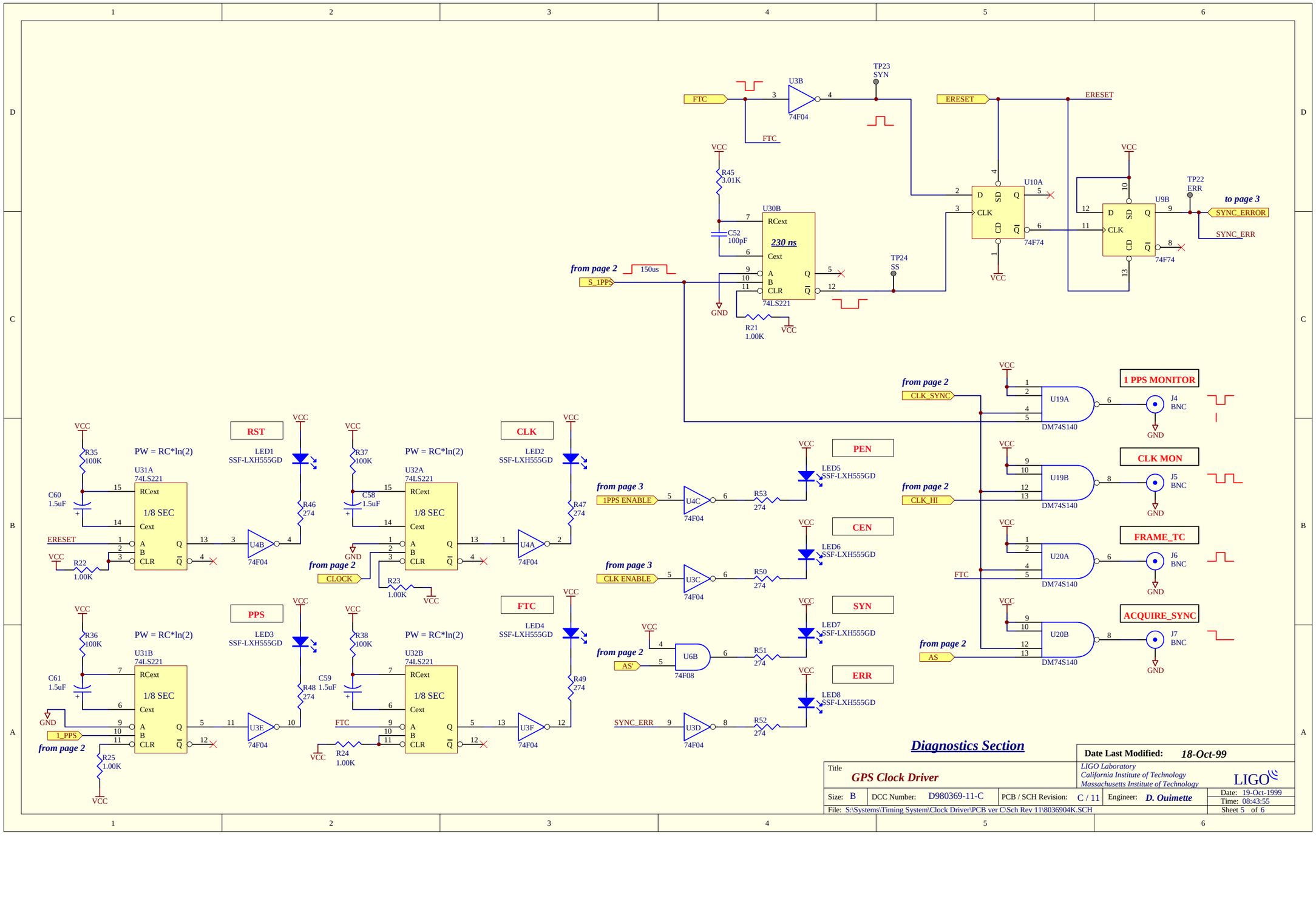
Title: *GPS Clock Driver*				*LIGO Laboratory* / *California Institute of Technology* / *Massachusetts Institute of Technology*	LIGO
Size: B	DCC Number: D980369-11-C	PCB / SCH Revision: C / 11	Engineer: *D. Ouimette*	Date: 19-Oct-1999	
File: S:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036901K.SCH				Time: 08:42:39	
				Sheet 2 of 6	


VME Slave Interface
VME BUS
U23
AM1
AM5
AM4
AM3
AM0
IACK*
A15
A14
A13
P=Q
Internal Pull up Resistors
VCC
S2
SW DIP-3
74ALS520
GND
U8B
74F74
25 nsec Delay
DL1
DDU8F-5025
U9A
74F74
VME_RESET
U26A
74F38
DTACK*
Status Register
(ALL)
1PPS_ENB
1PPS_SYNC
CLK_SYNC
AS
SYNC_ERROR
from page 2
from page 2
from page 2
from page 5
U24
74F374
D00
D01
D02
D03
D04
D05
D06
D07
U25B
74LS04
U27A
74LS20
OE'
to page 2 & 5
CLK ENABLE
Command Register
U28
74ALS273
CLK
CLR
LE
Board Reset
Error Reset
U27B
74LS20
DS0*
U25C
74LS04
15 nsec Delay
DL2
DDU8F-5025
WRITE*
U25A
74LS04
AAA
111
543
000 = Addr $0000 - $1FFF
001 = Addr $2000 - $3FFF
010 = Addr $4000 - $5FFF
011 = Addr $6000 - $7FFF
100 = Addr $8000 - $9FFF
101 = Addr $A000 - $BFFF
110 = Addr $C000 - $DFFF
111 = Addr $E000 - $FFFF
to page 2 & 5
1PPS ENABLE
1PPS_ENB
U14B
74F32
JP6
ENABLE
GND
U25E
74LS04
U25D
74LS04
VME BUS
SYSRESET
VCC
D1
S1ADICT
R28
1.00M
C47
1uF
R29
20
S1
RESET
U6A
74F08
U5C
74F08
U5D
74F08
TP16
RST
to page 5
ERESET
BRESET
to page 2
VME_RESET
REVISIONS:
Rev C/9 is the first board of the Rev C PCB.
Rev C/9 to C/10
1) C57 was increased from 0.01uF to 0.1uF to give a 1msec Ramp Out. Page 4 of 6.
2) R12 was changed to 1.5K and R39 was changed to 2.55K to adjust the amplitude of the Ramp Out. C62 was added to limit high frequency noise on the ramp. Page 4 of 6.
Rev C/10 to C/11
1) R40 and R41 are changed to 787 Ohms. R54 and R55 are added to the back side of the board at J3 to scale the "1 PPS OUT" amplitude for the ICS ADCs. Page 4 of 6.
VME Slave Interface Section
Date Last Modified: 18-Oct-99
Title
GPS Clock Driver
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
LIGO
Size: B
DCC Number: D980369-11-C
PCB / SCH Revision: C / 11
Engineer: D. Ouimette
Date: 19-Oct-1999
Time: 08:43:15
File: S:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036902K.SCH
Sheet 3 of 6

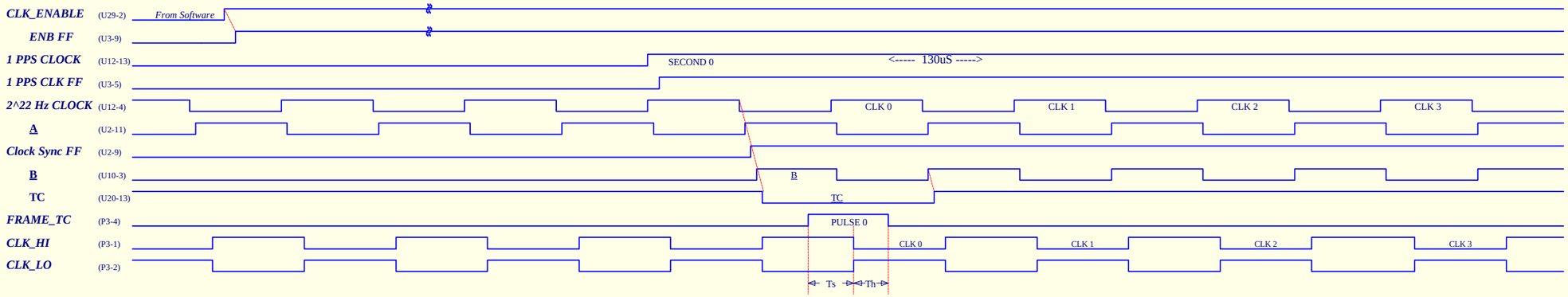


Independent Timing Section

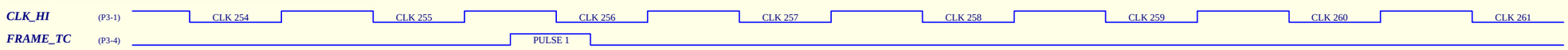
Title: GPS Clock Driver				Date Last Modified: 18-Oct-99	
LIGO Laboratory, California Institute of Technology, Massachusetts Institute of Technology					
Size: B	DCC Number: D980369-11-C	PCB / SCH Revision: C / 11	Engineer: D. Ouimette	Date: 19-Oct-1999	
File: S:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036903K.SCH				Time: 08:43:39	
				Sheet 4 of 6	


FTC
U3B
74F04
TP23
SYN
ERESET
ERESET
FTC
VCC
R45
3.01K
U30B
RCext
230 ns
Cext
C52
100pF
74LS221
from page 2
150us
S_1PPS
GND
R21
1.00K
TP24
SS
U10A
74F74
U9B
74F74
TP22
ERR
to page 3
SYNC_ERROR
SYNC_ERR
from page 2
CLK_SYNC
1 PPS MONITOR
U19A
DM74S140
J4
BNC
CLK MON
U19B
J5
FRAME_TC
U20A
J6
ACQUIRE_SYNC
U20B
J7
from page 2
CLK_HI
FTC
from page 2
AS
RST
PPS
CLK
FTC
PEN
CEN
SYN
ERR
PW = RC*ln(2)
U31A
U31B
U32A
U32B
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
SSF-LXH555GD
R35
100K
R36
R37
R38
C60
1.5uF
C61
C58
C59
R22
1.00K
R23
R24
R25
R46
274
R47
R48
R49
R53
R50
R51
R52
from page 3
1PPS ENABLE
CLK ENABLE
from page 2
AS'
SYNC_ERR
U4C
U4A
U4B
U3C
U6B
U3D
U3E
U3F
74F08
1_PPS
Diagnostics Section
Title
GPS Clock Driver
Date Last Modified: 18-Oct-99
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
LIGO
Size: B
DCC Number: D980369-11-C
PCB / SCH Revision: C / 11
Engineer: D. Ouimette
Date: 19-Oct-1999
Time: 08:43:55
Sheet 5 of 6
File: S:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036904K.SCH

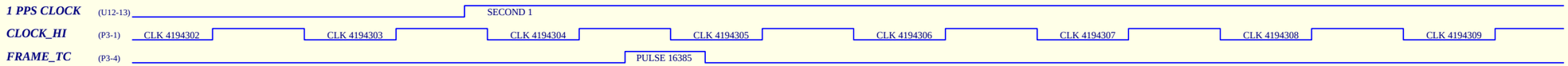
Initialize timing by sending a software 'CLK ENABLE"



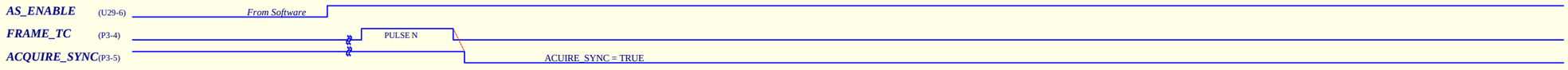
Timing relation of second FRAME_TC and CLK_HI outputs



Timing relation of FRAME_TC and CLOCK_HI at the end of the first second



After ADCs are initialized send a software acquire sync enable "AS_ENABLE"



NOTE:
This Timing Diagram has not yet been updated to the rev C / 11 version of the board.

Timing Diagram

Date Last Modified: ***18-Oct-99***

Title: ***GPS Clock driver***

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology

LIGO

Size: B	DCC Number: D980369-11-C	PCB / SCH Revision: C / 11	Engineer: ***D. Ouimette***	Date: 23-Jan-2000
				Time: 11:21:28
File: D:\Systems\Timing System\Clock Driver\PCB ver C\Sch Rev 11\8036905K.SCH				Sheet 6 of 6