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CONVERTER BACKPLANE

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1 Introduction and Overview

This document describes the enclosure, form factor and backplane of the new converter design.

2 Form Factor

2.1 Crate

We use an EMI compatible enclosure and follow the eurocrate standard as described by IEEE 1101.1/1101.10. This is basically the familiar VME type chassis, but we include keyable guide rails with ground pins and ESD clip and type IV injector/extractor handles. An example crate assembly can be found at http://www.kaparel.com (Ripac Vario EMC).

The total crate height will either be 7U or 8U to support circulating air both above and below the boards. This additional space will also be used to add a power switch and a series of LEDs indicating the status of the supply voltages.

Cooling is envisioned to be internal by circulating cool air from below the boards, up and down again behind the backplane. A water cooled heat exchanger is used to cool the air behind the backplane. A set of low noise slow rotating fans below the heat exchanger blowing downward may be required to keep the air flow going.

2.2 Slot Assignment

The width of a board assembly will be 6 HP (30.48 mm). This allows 14 slots in a full width crate. The slot to the most left (position 1) is dedicated as the power controller board. It contains voltage and current monitors, flow indication for the water cooling, temperature readouts and the fan controllers. The next board in slot 2 is the uplink and timing board. There are 4 dedicated controller slots in position 4, position 7, position 10 and position 13. All others slots are used for

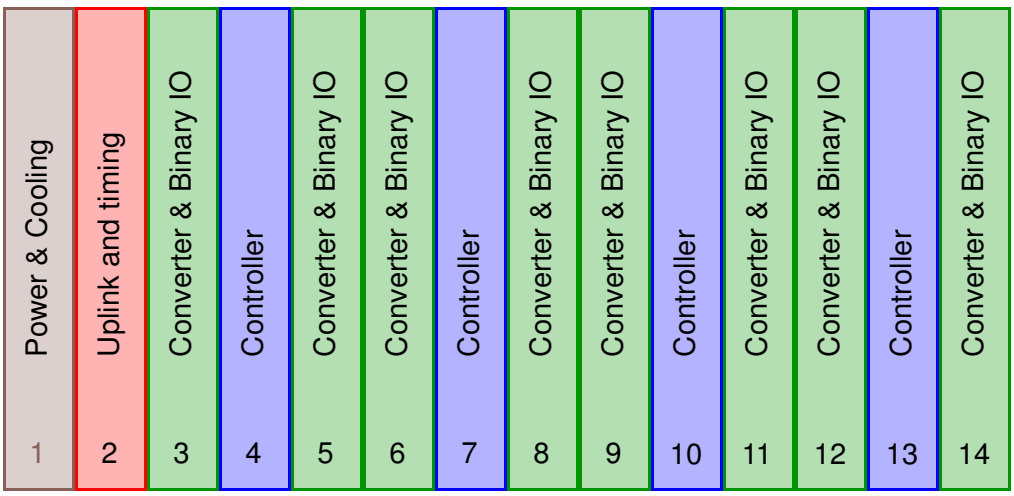

Figure 1: Slot assignment.

converter and interface boards. Slots are keyed to prevent wrong insertion. (An alternate configuration could be controllers in slot 4, 8 and 12 and converters in the 9 remaing slots.)

2.3 Board Dimensions

The board height is 6U or 233 mm. The board width has been set to 280 mm (120 mm deeper than a standard VME type board). Board assemblies are 6 HP wide or 30.48 mm. The clearance below the board is then 1 HP + 2.5 mm (7.6 mm) total. The bottom surface of a board can be used for components such as bypass capacitors. With a board thickness of 1.6 mm the maximum component height on the top surface is 18.8 mm—leaving a 2.5 mm gap to the next board.

2.4 Connectors

Converter boards use two standard 96-pin DIN 41612 connectors (P1 at the top and P2 at the bottom). This gives a total number of 192 individual connections. Connectors are mounted at the same position as on a standard VME board.

The uplink and controller boards use 2 mm hard metric connectors (IEC 61076-4-101). The 2 mm connectors are 5 row versions as in the CompactPCI specification. We follow the CompactPCI standard and use a 25 position type A connector (J1, starting at the bottom), a 22 position type B connector (J2), a 19 position type B connector (J3), another 25 position type A connector (J4) and another 22 position type B connector (J5). This gives a total of 107 usable positions (3 positions on each type A connector are used for a guiding cavity) and a total of 535 individual connections.

3 Signal Convention

3.1 Converter Interface

3.2 FPGA Interconnect

3.3 Timing

3.4 Gigabit Interface

4 CONFIGURATION

4.1 CONFIGURATION EEPROM

4.2 FPGA CONFIGURATION

4.3 POWER SUPPLY STATUS

5 Power Supplies

A sketch of the power supply components is shown in Figure 2. The power supplies are mounted at the back of the rack behind the heat exchanger. The back of the crate will employ a cool plate on which the regulators and converters can be mounted. In the current sketch all voltages are derived from 48V DC using low noise switching regulators. Both input EMI filters and output ripple filters are used to suppress noise. The total power provided to the backplane cannot exceed the thermal rating of the crate.

5.1 Analog Supplies

Analog supplies are provided to the converter board as well as the uplink board (phase-locked loop and voltage-controlled oscillator). The analog supply voltages are meant to be regulated to 5.0V and 15.0V, respectively, using low drop-out linear regulators. Due to the sad state of low drop-out negative voltage regulators an additional ±24V is provided, so that a suitable supply voltage will be available for an on-board controller circuit.

Table 1: Analog Supplies

Name	Voltage	Tolerance	Current	Board
+AV1	+6.5V	±0.3V	10A	Converter
–AV1	–6.5V	±0.3V	10A	Converter
+AV2	+16.5V	±0.8V	10A	Converter/Uplink
–AV2	–16.5V	±0.8V	10A	Converter/Uplink
+AV3	+24V	±1.0V	10A	Converter/Uplink
–AV3	–24V	±1.0V	10A	Converter/Uplink

Since there are 10 A of current available for each rail, each converter board has a maximum rating of 1 A per rail.

5.2 Digital Supplies

Only a +12V supply is provided to the uplink and controller boards. Local regulators are used to generate +5V, +3.3V and any other required digital voltage. The controller boards extend the +5V and the +3.3V digital supply to the converter boards. Converter boards may generate their digital supply which is most likely +3.3V from the +5V by use of a linear voltage regulator.

Table 2: Digital Supplies

Name	Voltage	Tolerance	Current	Board
DV1	+5.0V	±0.3V	6A	Converter
DV2	+3.3V	±0.16V	6A	Converter
DV3	+12V	±0.6V	20A	Controller/Uplink
DV4	+48V	±1.2V	—	Auxiliary and stand-by power (not switched)

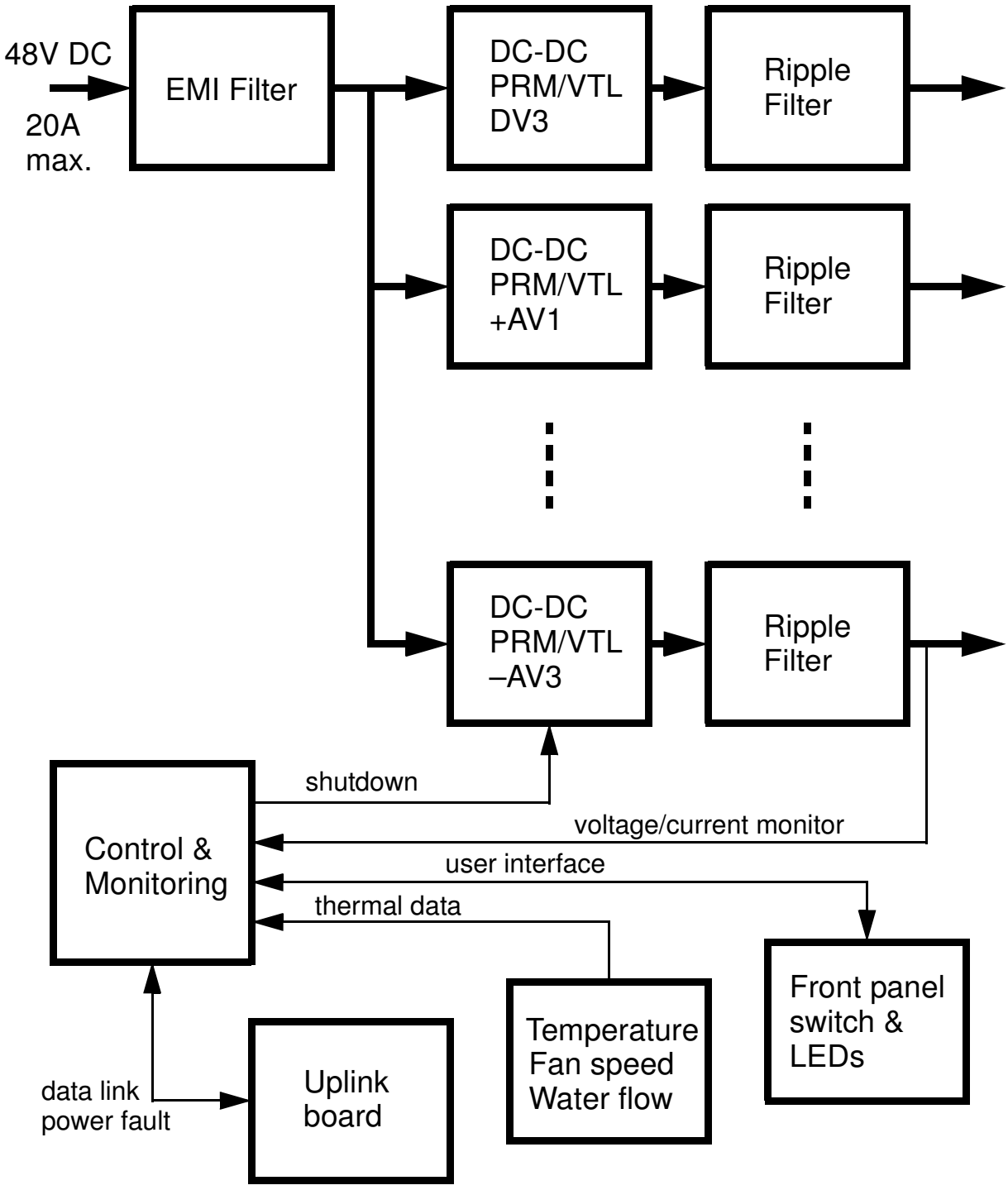

Figure 2: Sketch of power supply components.

The 20A of current for the +12V supply is distributed over the uplink and controller boards. This gives a maximum rating of 4A per board. DV1 and DV2 are generated on the controller boards and a maximum of 6A is provided for the converter boards, yielding a maximum rating of 3A per board and rail. Since these voltages are derived from the +12V rail, one has to be careful not to exceed the maximum rating for the +12V supply.

5.3 Control and Monitoring

The main power which is provided by the +48V input voltage is used for powering the power and cooling board. All other supplies in the back of the crate will have a thermal shutdown when the internal temperature exceeds 70°C, upon a fan failure or when the water flow in the cooling systems is interrupted. A front panel on-off switch can also be used to switch these DC-DC regulators in the back of the crate. The front panel switch does not disconnect the power supply but rather uses the shutdown control of the DC-DC converters. A true power switch is provided in the back to disconnect the 48V DC feed. Access to a set of fuses protecting each individual power rail as well as the 48V DC feed are also located in the back.

The power and cooling board reads both voltage and current from each power rail. The front panel of the power and cooling board consists of a power switch, a series of LEDs indicating the status of each supply line, and it has tip jacks (mini banana jacks) to hook up a DVM. Fan speed, probes to measure the crate tempearure(s) and a water flow indicator are all made available by the power and cooling board. In the case of fan failures or high temperature alarm the power supplies will shut down automatically. An interface to the uplink board is provided by a serial interface. The control and monitoring board also employs a configuration EEPROM. The power fault signal is an open collector drive which could also be used by a controller board or the uplink board to indicate a temperature alarm.

6 PIN ASSIGNMENT

Table 3: Signal Names

Signal	Description
DV1	Converter board digital power supply, +5V
DV2	Converter board digital power supply, +3.3V
DV3	Controller/uplink board digital power supply, +12V
DV4	Power and cooling board, +48V
GND	Digital ground
+AV1	Converter board analog power supply, +6V
–AV1	Converter board analog power supply, –6V
+AV2	Converter board analog power supply, +16.5V
–AV2	Converter board analog power supply, –16.5V
+AV3	Converter board analog power supply, +24V
–AV3	Converter board analog power supply, –24V
AGND	Converter board analog ground
Sx_P/Sx_N	28 LVDS signals between converter boards (A to D) and a controller board 8 LVDS signals between uplink and (E) and power & cooling board
Ux_P/Ux_N	uplink between uplink board and controller board; one clock and 10 LVDS signals
Dx_P/Dx_N	downlink between uplink board and controller board; one clock and 10 LVDS signals
CLK_P/CLK_N	67.108864 MHz clock, LVDS
SYNC_P/SYNC_N	1PPS, LVDS
CLKx_P/CLKx_N	spare clock signals, LVDS
CFG_VCC/CFG_GND	Power supply for serial configuration EEPROM
CFG_CLK	Clock for serial configuration EEPROM
CFG_SI/CFG_SO	Serial input and output of configuration EEPROM
CFG_CS	Chip select for serial configuration EEPROM
CFG_RDY	Board present bit (must be connected to CFG_GND on converter and controller boards)
FP_CLK/FP_D	FPGA programming, clock and serial data
FP_SEL/FP_Ax	FPGA programming, board select and FPGA select
FP_START/FP_DONE	FPGA programming, start configuration and configuration finished
FP_WAIT/FP_INIT	FPGA programming, set wait and initialization flag
PWR_xxx	Serial interface to power supply
PWR_STDBY	+5V stand-by power, 200mA per controller/uplink board
PWR_FAULT	power fault indicator/power shutdown (open-collector)

Analog ground (AGND) and digital ground (GND) are connected together in the backplane.

Table 4: Converter board P1

position	row a	row b	row c
1	GND	GND	DV1
2	S1_N	GND	DV1
3	S1_P	GND	DV1
4	GND	GND	DV1
5	S2_P	GND	DV1
6	S2_N	GND	DV1
7	GND	GND	DV2
8	S3_N	GND	DV2
9	S3_P	GND	DV2
10	GND	GND	DV2
11	S4_P	GND	DV2
12	S4_N	GND	DV2
13	GND	GND	DV3
14	S5_N	GND	DV3
15	S5_P	GND	
16	GND	GND	
17	S6_P	GND	
18	S6_N	GND	
19	GND	GND	
20	S7_N	GND	
21	S7_P	GND	
22	GND	GND	
23	S8_P	GND	
24	S8_N	GND	
25	S9_N	GND	+AV1
26	S9_P	GND	+AV1
27	S10_P	GND	+AV1
28	S10_N	GND	+AV1
29	S11_N	GND	–AV1
30	S11_P	GND	–AV1
31	S12_P	GND	–AV1
32	S12_N	GND	–AV1

Table 5: Converter board P2

position	row a	row b	row c
1	S13_N	GND	+AV2
2	S13_P	GND	+AV2
3	S14_P	GND	+AV2
4	S14_N	GND	+AV2
5	S15_N	GND	–AV2
6	S15_P	GND	–AV2
7	S16_P	GND	–AV2
8	S16_N	GND	–AV2
9	S17_N	GND	+AV3
10	S17_P	GND	+AV3
11	S18_P	GND	–AV3
12	S18_N	GND	–AV3
13	S19_N	GND	
14	S19_P	GND	
15	S20_P	GND	
16	S20_N	GND	
17	S21_N	GND	
18	S21_P	GND	
19	S22_P	GND	
20	S22_N	GND	
21	S23_N	GND	
22	S23_P	GND	
23	S24_P	GND	
24	S24_N	GND	
25	S25_N	GND	
26	S25_P	GND	CFG_GND
27	S26_P	GND	CFG_CLK
28	S26_N	GND	CFG_VCC
29	S27_N	GND	CFG_CS
30	S27_P	GND	CFG_SI
31	S28_P	GND	CFG_SO
32	S28_N	GND	CFG_RDY

Table 6: Controller board J5 (type B)

position	row a	row b	row c	row d	row e
22	FP_CLK	GND	FP_A0	FP_A1	FP_A2
21	GND	GND	FP_D	FP_START	FP_INIT
20	GND	GND	FP_SEL	FP_DONE	FP_WAIT
19	GND	GND	GND	GND	GND
18	S1A_P	S1A_N	GND	S1B_P	S1B_N
17	DV3	DV3	DV3	DV3	DV3
16	S1C_P	S1C_N	GND	S1D_P	S1D_N
15	GND	GND	GND	GND	GND
14	S2A_P	S2A_N	GND	S2B_P	S2B_N
13	DV3	DV3	DV3	DV3	DV3
12	S2C_P	S2C_N	GND	S2D_P	S2D_N
11	GND	GND	GND	GND	GND
10	S3A_P	S3A_N	GND	S3B_P	S3B_N
9	DV3	DV3	DV3	DV3	DV3
8	S3C_P	S3C_N	GND	S3D_P	S3D_N
7	GND	GND	GND	GND	GND
6	S4A_P	S4A_N	GND	S4B_P	S4B_N
5	DV3	DV3	DV3	DV3	DV3
4	S4C_P	S4C_N	GND	S4D_P	S4D_N
3	GND	GND	GND	GND	GND
2	S5A_P	S5A_N	GND	S5B_P	S5B_N
1	DV3	DV3	DV3	DV3	DV3

Table 7: Controller board J4 (type A)

position	row a	row b	row c	row d	row e
25	S5C_P	S5C_N	GND	S5D_P	S5D_N
24	GND	GND	GND	GND	GND
23	S6A_P	S6A_N	GND	S6B_P	S6B_N
22	DV3	DV3	DV3	DV3	DV3
21	S6C_P	S6C_N	GND	S6D_P	S6D_N
20	GND	GND	GND	GND	GND
19	S7A_P	S7A_N	GND	S7B_P	S7B_N
18	DV3	DV3	DV3	DV3	DV3
17	S7C_P	S7C_N	GND	S7D_P	S7D_N
16	GND	GND	GND	GND	GND
15	S8A_P	S8A_N	GND	S8B_P	S8B_N
14					
13					
12					
11	S9A_P	S9A_N	GND	S9B_P	S9B_N
10	S10A_P	S10A_N	GND	S10B_P	S10B_N
9	S11A_P	S11A_N	GND	S11B_P	S11B_N
8	S12A_P	S12A_N	GND	S12B_P	S12B_N
7	GND	GND	GND	GND	GND
6	S8C_P	S8C_N	GND	S8D_P	S8D_N
5	S9C_P	S9C_N	GND	S9D_P	S9D_N
4	S10C_P	S10C_N	GND	S10D_P	S10D_N
3	S11C_P	S11C_N	GND	S11D_P	S11D_N
2	S12C_P	S12C_N	GND	S12D_P	S12D_N
1	GND	GND	GND	GND	GND

Table 8: Controller board J3 (type B)

position	row a	row b	row c	row d	row e
19	GND	GND	GND	GND	GND
18	CLK_P	CLK_N	GND	GND	GND
17	GND	GND	GND	CLK2_P	CLK2_N
16	GND	GND	GND	GND	GND
15	SYNC_P	SYNC_N	GND	CLK3_P	CLK3_N
14	GND	GND	GND	GND	GND
13	DCLK_P	DCLK_N	GND	UCLK_P	UCLK_N
12	GND	GND	GND	GND	GND
11	D0_P	D0_N	GND	U0_P	U0_N
10	D1_P	D1_N	GND	U1_P	U1_N
9	D2_P	D2_N	GND	U2_P	U2_N
8	D3_P	D3_N	GND	U3_P	U3_N
7	D4_P	D4_N	GND	U4_P	U4_N
6	D5_P	D5_N	GND	U5_P	U5_N
5	D6_P	D6_N	GND	U6_P	U6_N
4	D7_P	D7_N	GND	U7_P	U7_N
3	D8_P	D8_N	GND	U8_P	U8_N
2	D9_P	D9_N	GND	U9_P	U9_N
1	GND	GND	GND	GND	GND

Table 9: Controller board J2 (type B)

position	row a	row b	row c	row d	row e
22	S13A_P	S13A_N	GND	S13B_P	S13B_N
21	S14A_P	S14A_N	GND	S14B_P	S14B_N
20	S15A_P	S15A_N	GND	S15B_P	S15B_N
19	S16A_P	S16A_N	GND	S16B_P	S16B_N
18	DV3	DV3	DV3	DV3	DV3
17	S13C_P	S13C_N	GND	S13D_P	S13D_N
16	S14C_P	S14C_N	GND	S14D_P	S14D_N
15	S15C_P	S15C_N	GND	S15D_P	S15D_N
14	S16C_P	S16C_N	GND	S16D_P	S16D_N
13	DV3	DV3	DV3	DV3	DV3
12	S17A_P	S17A_N	GND	S17B_P	S17B_N
11	S18A_P	S18A_N	GND	S18B_P	S18B_N
10	S19A_P	S19A_N	GND	S19B_P	S19B_N
9	S20A_P	S20A_N	GND	S20B_P	S20B_N
8	DV3	DV3	DV3	DV3	DV3
7	S17C_P	S17C_N	GND	S17D_P	S17D_N
6	S18C_P	S18C_N	GND	S18D_P	S18D_N
5	S19C_P	S19C_N	GND	S19D_P	S19D_N
4	S2C0_P	S20C_N	GND	S20D_P	S20D_N
3	DV3	DV3	DV3	DV3	DV3
2	S21A_P	S21A_N	GND	S21B_P	S21B_N
1	S22A_P	S22A_N	GND	S22B_P	S22B_N

Table 10: Controller board J1 (type A)

position	row a	row b	row c	row d	row e
25	S23A_P	S23A_N	GND	S23B_P	S23B_N
24	S24A_P	S24A_N	GND	S24B_P	S24B_N
23	DV3	DV3	DV3	DV3	DV3
22	S21C_P	S21C_N	GND	S21D_P	S21D_N
21	S22C_P	S22C_N	GND	S22D_P	S22D_N
20	S23C_P	S23C_N	GND	S23D_P	S23D_N
19	S24C_P	S24C_N	GND	S24D_P	S24D_N
18	DV3	DV3	DV3	DV3	DV3
17	S25A_P	S25A_N	GND	S25B_P	S25B_N
16	S26A_P	S26A_N	GND	S26B_P	S26B_N
15	S27A_P	S27A_N	GND	S27B_P	S27B_N
14					
13					
12					
11	S28A_P	S28A_N	GND	S28B_P	S28B_N
10	DV5	DV5	DV5	DV5	DV5
9	S25C_P	S25C_N	GND	S25D_P	S25D_N
8	S26C_P	S26C_N	GND	S26D_P	S26D_N
7	S27C_P	S27C_N	GND	S27D_P	S27D_N
6	S28C_P	S28C_N	GND	S28D_P	S28D_N
5	GND	GND	GND	GND	GND
4	CFG_GND	CFG_CS	GND	GND	GND
3	CFG_CLK	CFG_GND	GND	GND	GND
2	CFG_VCC	CFG_SI	GND	GND	PWR_STDBY
1	CFG_RDY	CFG_SO	GND	GND	PWR_FAULT

Table 11: Uplink/timing board J5 (type B)

position	row a	row b	row c	row d	row e
22	FP_CLK	GND	FP_A0	FP_A1	FP_A2
21	GND	FP_SELa	FP_D	FP_START	FP_INIT
20	FP_SELb	FP_SELc	FP_SELd	FP_DONE	FP_WAIT
19	DV3	DV3	DV3	DV3	DV3
18	PWR_CLK	PWR_STDBY	PWR_RW	PWR_SI	PWR_CFG
17	GND	GND	PWR_SEL	PWR_SO	PWR_FAULT
16	GND	GND	GND	GND	GND
15	CLKd_P	CLKd_N	GND	GND	GND
14	GND	GND	GND	CLK2d_P	CLK2d_N
13	GND	GND	GND	GND	GND
12	SYNCd_P	SYNCd_N	GND	CLK3d_P	CLK3d_N
11	GND	GND	GND	GND	GND
10	DCLKd_P	DCLKd_N	GND	UCLKd_P	UCLKd_N
9	DV3	DV3	DV3	DV3	DV3
8	D0d_P	D0d_N	GND	U0d_P	U0d_N
7	D1d_P	D1d_N	GND	U1d_P	U1d_N
6	D2d_P	D2d_N	GND	U2d_P	U2d_N
5	D3d_P	D3d_N	GND	U3d_P	U3d_N
4	D4d_P	D4d_N	GND	U4d_P	U4d_N
3	D5d_P	D5d_N	GND	U5d_P	U5d_N
2	D6d_P	D6d_N	GND	U6d_P	U6d_N
1	D7d_P	D7d_N	GND	U7d_P	U7d_N

Table 12: Uplink/timing J4 (type A)

position	row a	row b	row c	row d	row e
25	D8d_P	D8d_N	GND	U8d_P	U8d_N
24	D9d_P	D9d_N	GND	U9d_P	U9d_N
23	GND	GND	GND	GND	GND
22	GND	GND	GND	GND	GND
21	CLKc_P	CLKc_N	GND	GND	GND
20	GND	GND	GND	CLK2c_P	CLK2c_N
19	GND	GND	GND	GND	GND
18	SYNCc_P	SYNCc_N	GND	CLK3c_P	CLK3c_N
17	GND	GND	GND	GND	GND
16	DCLKc_P	DCLKc_N	GND	UCLKc_P	UCLKc_N
15	DV3	DV3	DV3	DV3	DV3
14					
13					
12					
11	D0c_P	D0c_N	GND	U0c_P	U0c_N
10	D1c_P	D1c_N	GND	U1c_P	U1c_N
9	D2c_P	D2c_N	GND	U2c_P	U2c_N
8	D3c_P	D3c_N	GND	U3c_P	U3c_N
7	D4c_P	D4c_N	GND	U4c_P	U4c_N
6	D5c_P	D5c_N	GND	U5c_P	U5c_N
5	D6c_P	D6c_N	GND	U6c_P	U6c_N
4	D7c_P	D7c_N	GND	U7c_P	U7c_N
3	D8c_P	D8c_N	GND	U8c_P	U8c_N
2	D9c_P	D9c_N	GND	U9c_P	U9c_N
1	GND	GND	GND	GND	GND

Table 13: Uplink/timing J3 (type B)

position	row a	row b	row c	row d	row e
19	GND	GND	GND	GND	GND
18	CLKa_P	CLKa_N	GND	GND	GND
17	GND	GND	GND	CLK2a_P	CLK2a_N
16	GND	GND	GND	GND	GND
15	SYNCa_P	SYNCa_N	GND	CLK3a_P	CLK3a_N
14	GND	GND	GND	GND	GND
13	DCLKa_P	DCLKa_N	GND	UCLKa_P	UCLKa_N
12	DV3	DV3	DV3	DV3	DV3
11	D0a_P	D0a_N	GND	U0a_P	U0a_N
10	D1a_P	D1a_N	GND	U1a_P	U1a_N
9	D2a_P	D2a_N	GND	U2a_P	U2a_N
8	D3a_P	D3a_N	GND	U3a_P	U3a_N
7	D4a_P	D4a_N	GND	U4a_P	U4a_N
6	D5a_P	D5a_N	GND	U5a_P	U5a_N
5	D6a_P	D6a_N	GND	U6a_P	U6a_N
4	D7a_P	D7a_N	GND	U7a_P	U7a_N
3	D8a_P	D8a_N	GND	U8a_P	U8a_N
2	D9a_P	D9_aN	GND	U9a_P	U9a_N
1	GND	GND	GND	GND	GND

Table 14: Uplink/timing J2 (type B)

position	row a	row b	row c	row d	row e
22	GND	GND	GND	GND	GND
21	CLKb_P	CLKb_N	GND	GND	GND
20	GND	GND	GND	CLK2b_P	CLK2b_N
19	GND	GND	GND	GND	GND
18	SYNCb_P	SYNCb_N	GND	CLK3b_P	CLK3b_N
17	GND	GND	GND	GND	GND
16	DCLKb_P	DCLKb_N	GND	UCLKb_P	UCLKb_N
15	DV3	DV3	DV3	DV3	DV3
14	D0b_P	D0b_N	GND	U0b_P	U0b_N
13	D1b_P	D1b_N	GND	U1b_P	U1b_N
12	D2b_P	D2b_N	GND	U2b_P	U2b_N
11	D3b_P	D3b_N	GND	U3b_P	U3b_N
10	D4b_P	D4b_N	GND	U4b_P	U4b_N
9	D5b_P	D5b_N	GND	U5b_P	U5b_N
8	D6b_P	D6b_N	GND	U6b_P	U6b_N
7	D7b_P	D7b_N	GND	U7b_P	U7b_N
6	D8b_P	D8b_N	GND	U8b_P	U8b_N
5	D9b_P	D9b_N	GND	U9b_P	U9b_N
4	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND
2	S1E_P	S1E_N	DV3	DV3	DV3
1	GND	GND	DV3	DV3	DV3

Table 15: Uplink/timing board J1 (type A)

position	row a	row b	row c	row d	row e
25	S2E_P	S2E_N	DV3	DV3	DV3
24	S3E_P	S3E_N	DV3	DV3	DV3
23	S4E_P	S4E_N	GND	GND	GND
22	S5E_P	S5E_N	GND	GND	GND
21	S6E_P	S6E_N	DV3	DV3	DV3
20	S7E_P	S7E_N	DV3	DV3	DV3
19	S8E_P	S8E_N	DV3	DV3	DV3
18	GND	GND	GND	GND	GND
17	GND	AV3	GND	–AV3	GND
16	AGND	AV2	AGND	–AV2	AGND
15	AGND	AV2	AGND	–AV2	AGND
14					
13					
12					
11	GND	CFG_CS2	PWR_RW	PWR_CFG	PWR_FAULT
10	PWR_CLK	PWR_STDBY	PWR_SEL	PWR_SO	PWR_SI
9	CFG_GND	CFG_CS3	CFG_CS4	CFG_CS5	CFG_CS6
8	CFG_CLK	CFG_GND	CFG_CS7	CFG_CS8	CFG_CS9
7	CFG_VCC	CFG_CS10	CFG_CS11	CFG_CS12	CFG_CS13
6	CFG_SI	CFG_CS14	CFG_CS15	CFG_CS16	CFG_CS17
5	CFG_SO	CFG_CS18	CFG_CS19	CFG_CS20	CFG_CS21
4	CFG_RDY2	CFG_RDY3	CFG_RDY4	CFG_RDY5	CFG_RDY6
3	CFG_RDY7	CFG_RDY8	CFG_RDY9	CFG_RDY10	CFG_RDY11
2	CFG_RDY12	CFG_RDY13	CFG_RDY14	CFG_RDY15	CFG_RDY16
1	CFG_RDY17	CFG_RDY18	CFG_RDY19	CFG_RDY20	CFG_RDY21

Table 16: Power and Cooling board P1

position	row a	row b	row c
1	12VCC	GND	12VCC
2	12VCC	GND	12VCC
3	SYNC12	GND	SYNC24
4	RUN	GND	GND
5	I12P	GND	I24P
6	GND	GND	I24N
7	V12P	GND	V24P
8	GND	GND	V24N
9	LED12P	GND	LED24P
10	GND	GND	LED24N
11	12VCC	GND	12VCC
12	12VCC	GND	12VCC
13	SYNC7	GND	SYNC17
14	GND	GND	GND
15	I7P	GND	I17P
16	I7N	GND	I17N
17	V7P	GND	V17P
18	V7N	GND	V17N
19	LED7P	GND	LED17P
20	LED7N	GND	LED17N
21	GND	GND	GND
22	T1P	GND	T1N
23	T2P	GND	T2N
24	T3P	GND	T3N
25	GND	GND	GND
26	V48P	GND	P24V
27	FAN1P	GND	FAN2P
28	FAN1N	GND	FAN2N
29	FAN1S	GND	FAN2S
30	FAN3P	GND	FLOWP
31	FAN3N	GND	FLOWN
32	FAN3S	GND	FLOWS

Table 17: Power and Cooling board P2

position	row a	row b	row c
1		GND	PWRFAIL
2		GND	
3		GND	
4		GND	
5		GND	
6		GND	
7		GND	
8		GND	
9	GND	GND	
10	S1_N	GND	
11	S1_P	GND	
12	GND	GND	
13	S2_P	GND	
14	S2_N	GND	
15	GND	GND	
16	S3_N	GND	
17	S3_P	GND	
18	GND	GND	
19	S4_P	GND	
20	S4_N	GND	
21	GND	GND	
22	S5_N	GND	
23	S5_P	GND	
24	GND	GND	
25	S6_P	GND	
26	S6_N	GND	CFG_GND
27	GND	GND	CFG_CLK
28	S7_N	GND	CFG_VCC
29	S7_P	GND	CFG_CS
30	GND	GND	CFG_SI
31	S8_P	GND	CFG_SO
32	S8_N	GND	CFG_RDY