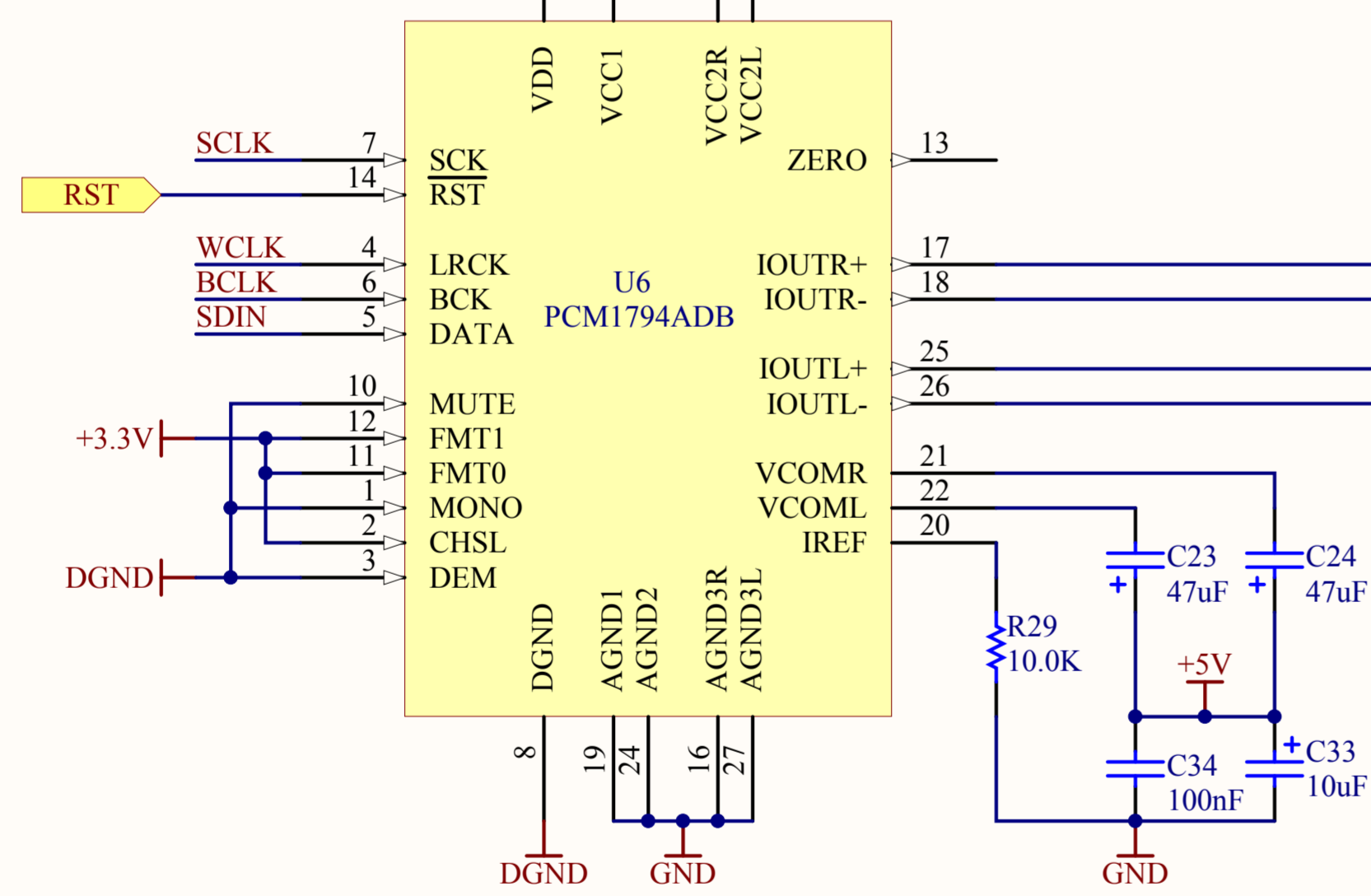
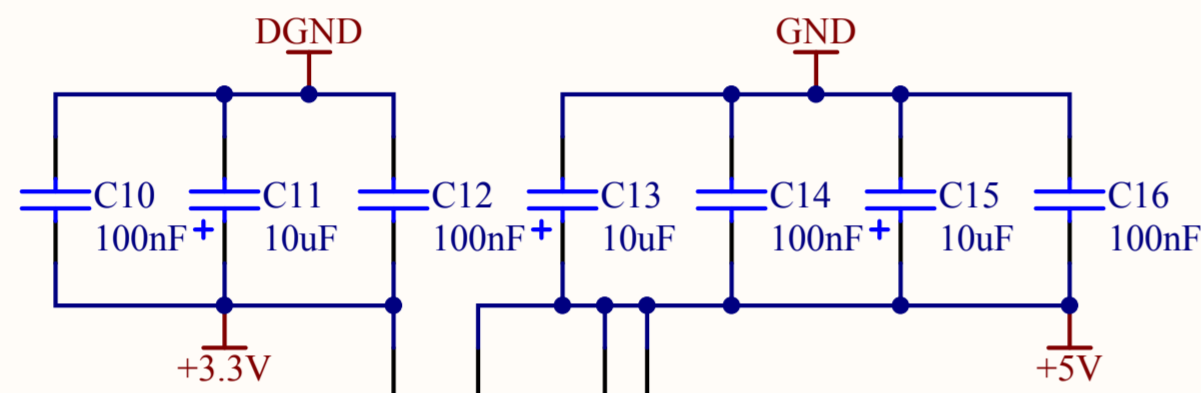
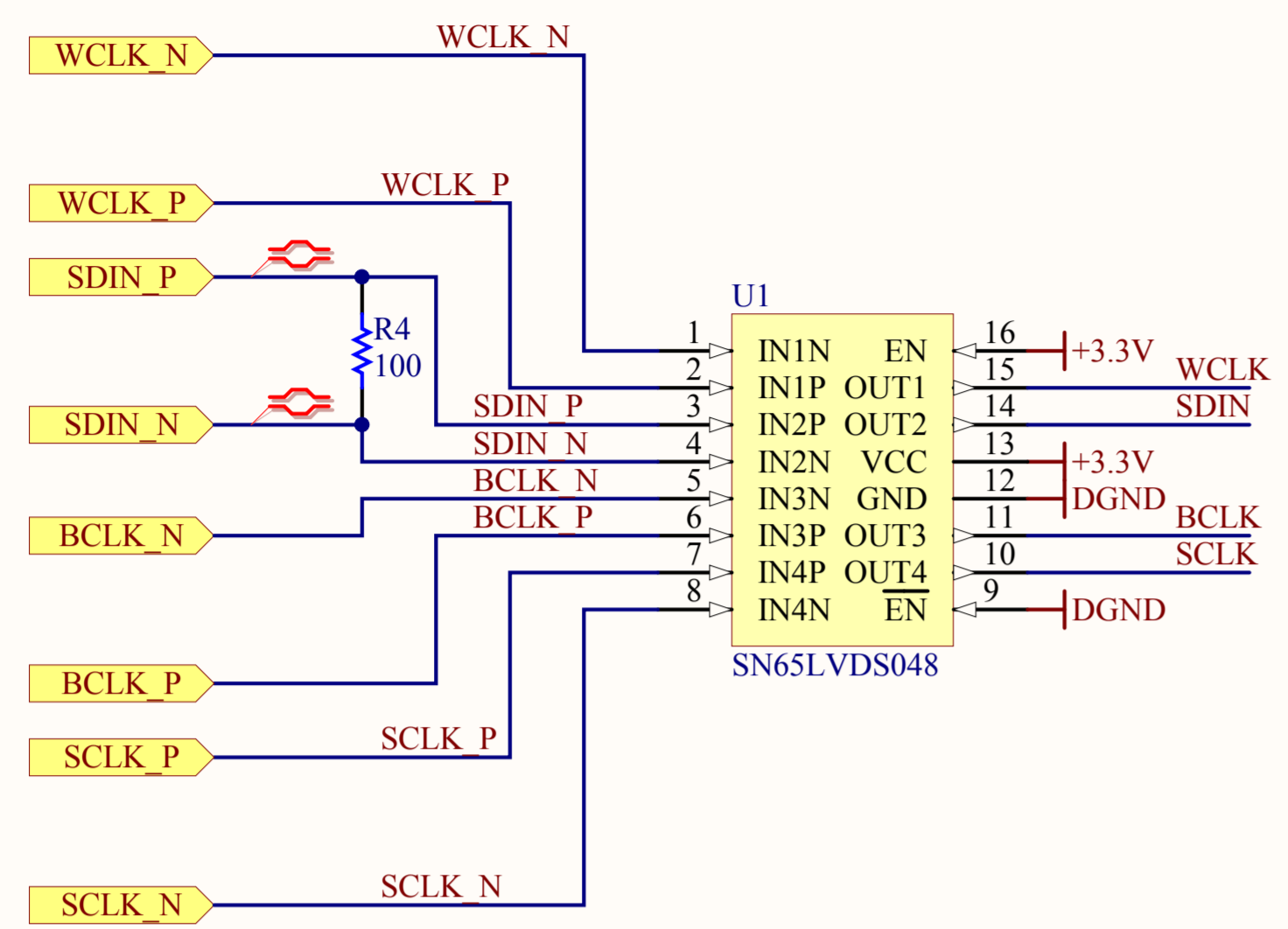
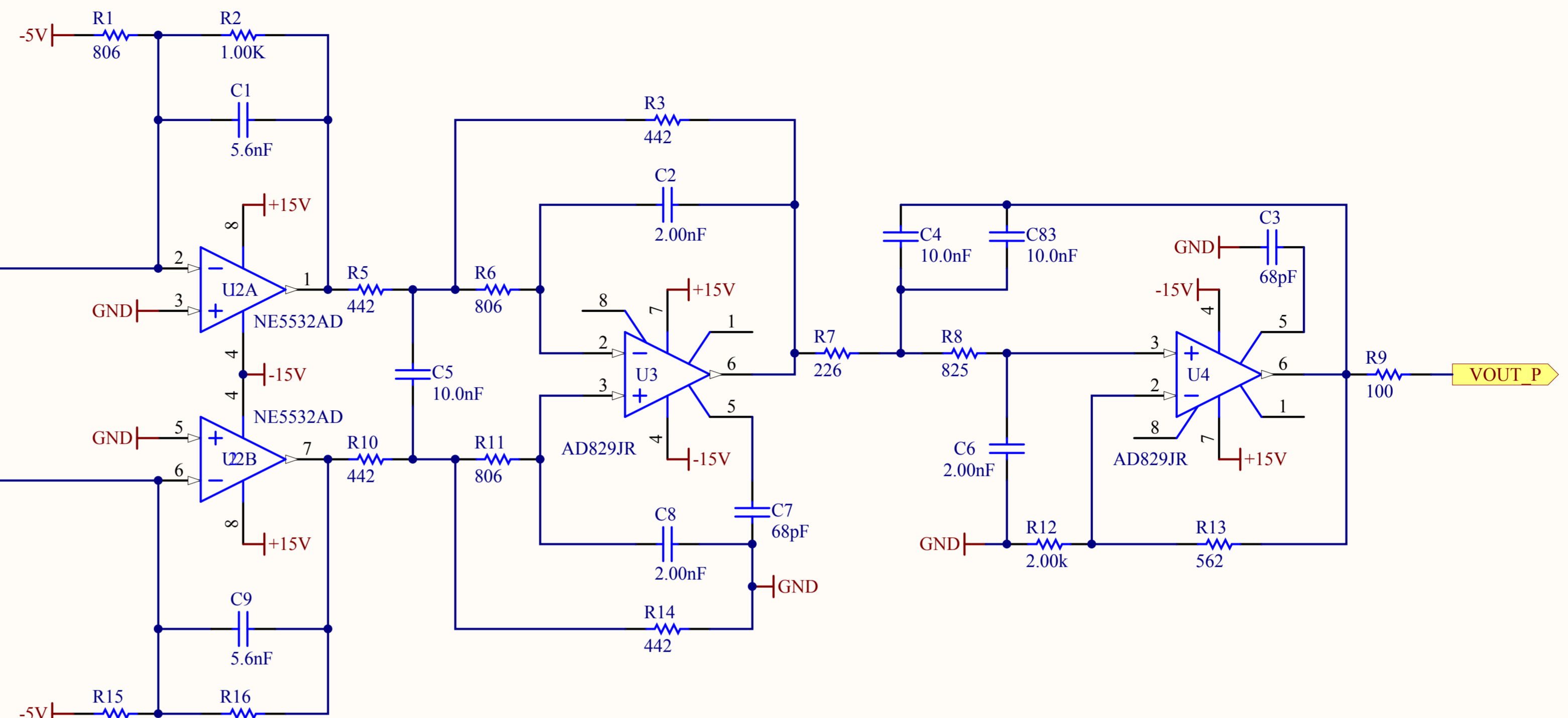


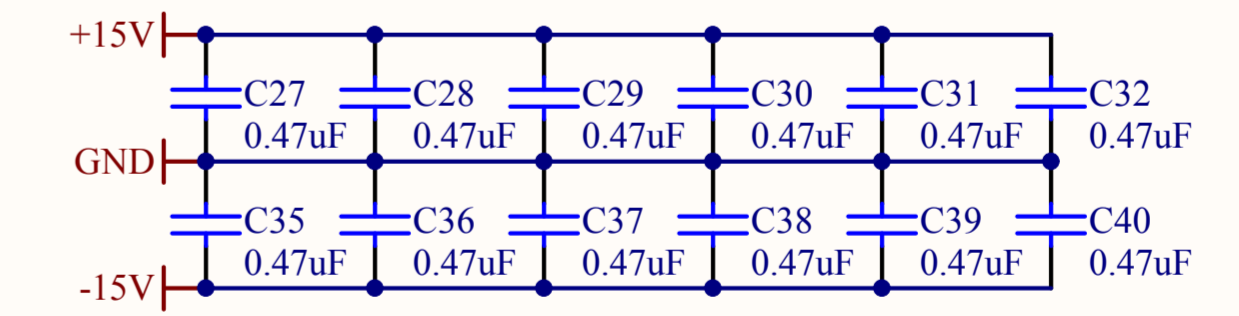
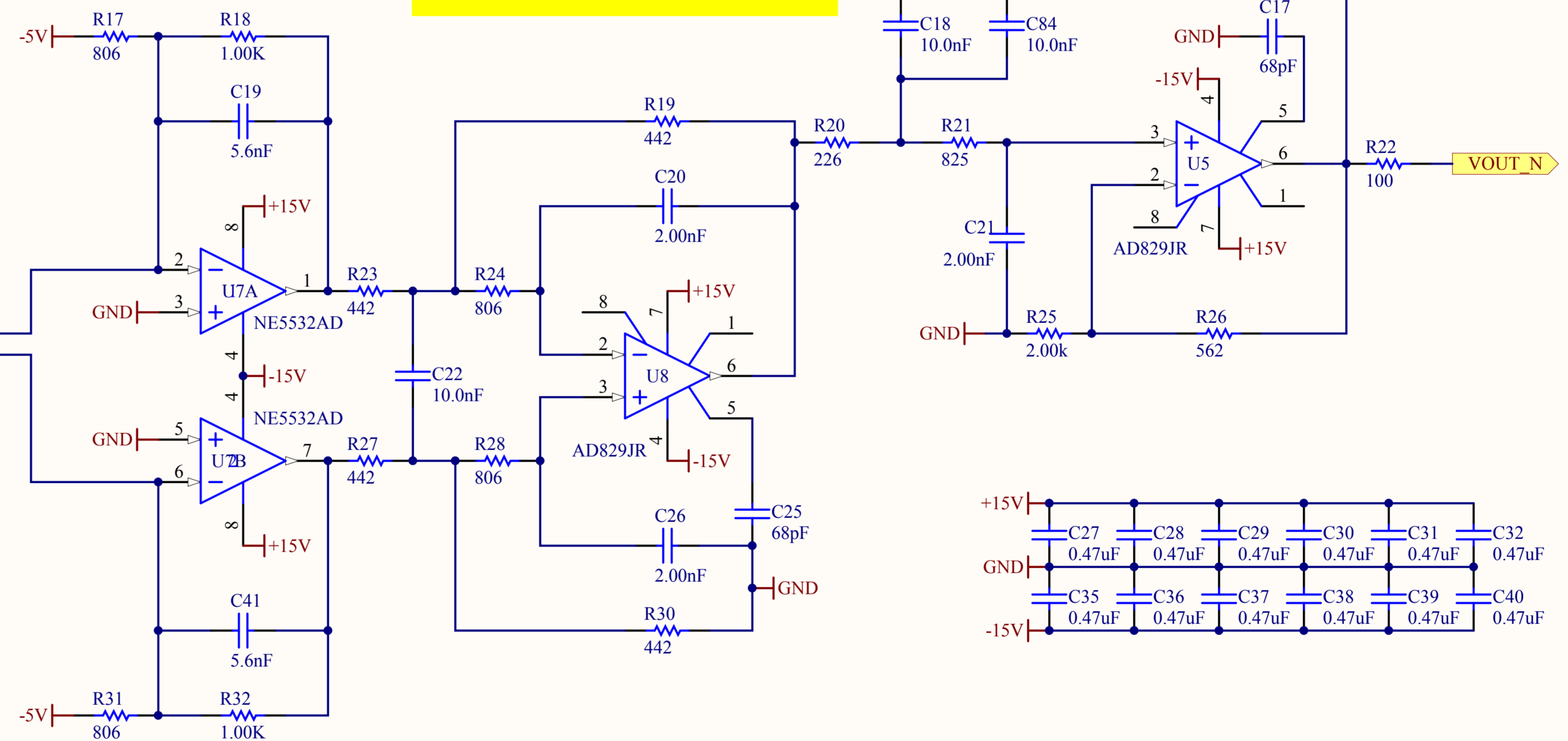
Title			DAC1794A / Top Sheet		
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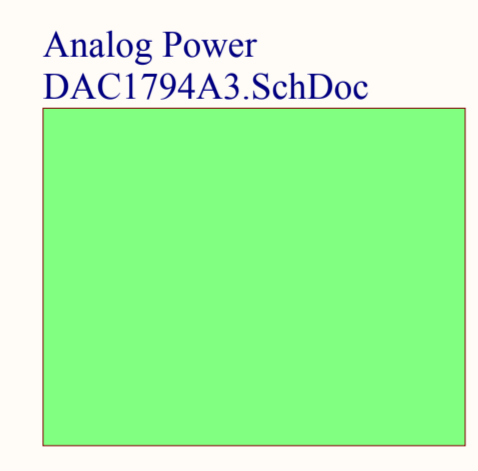
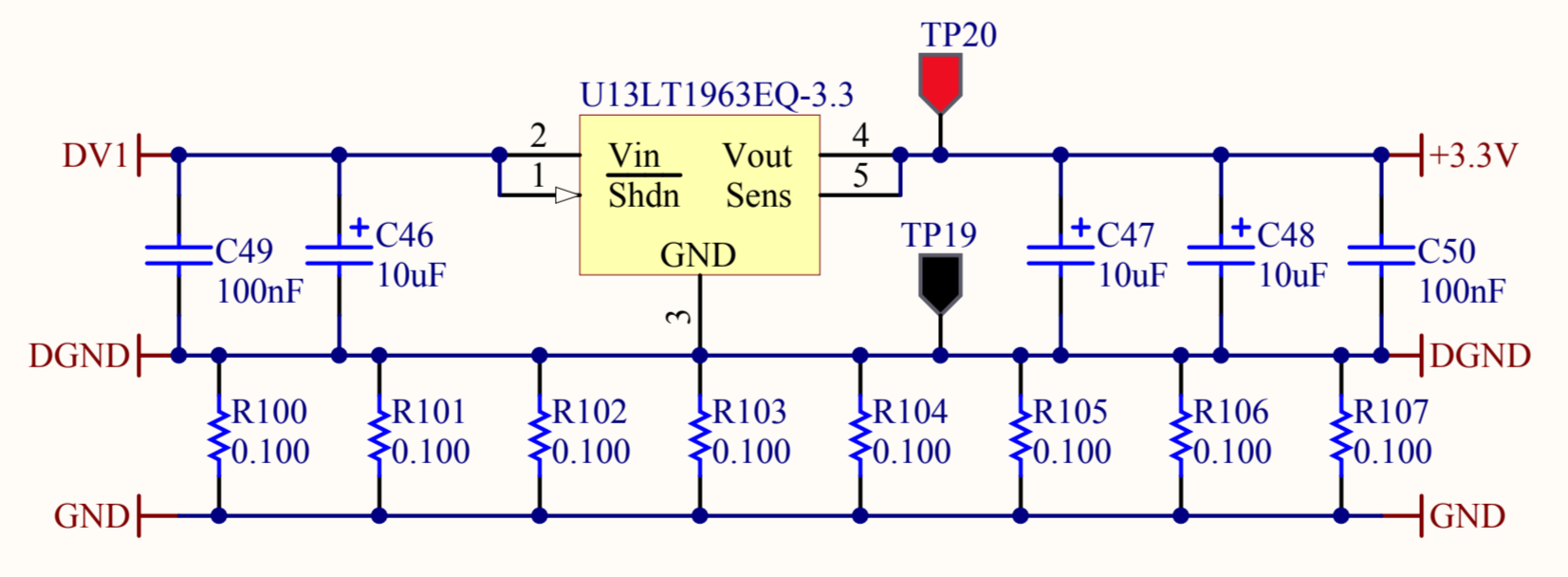
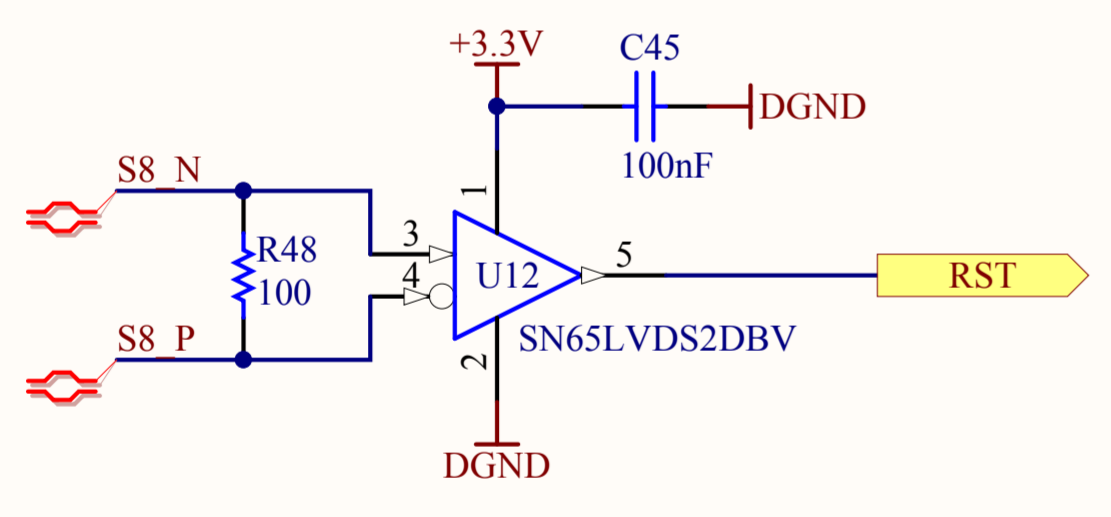
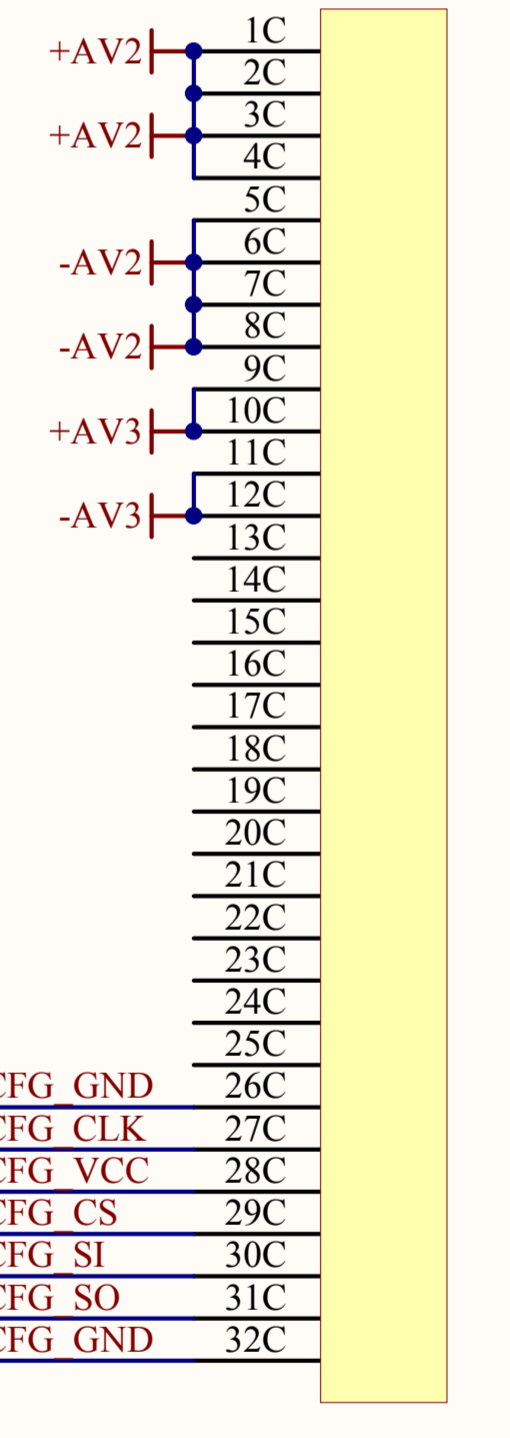
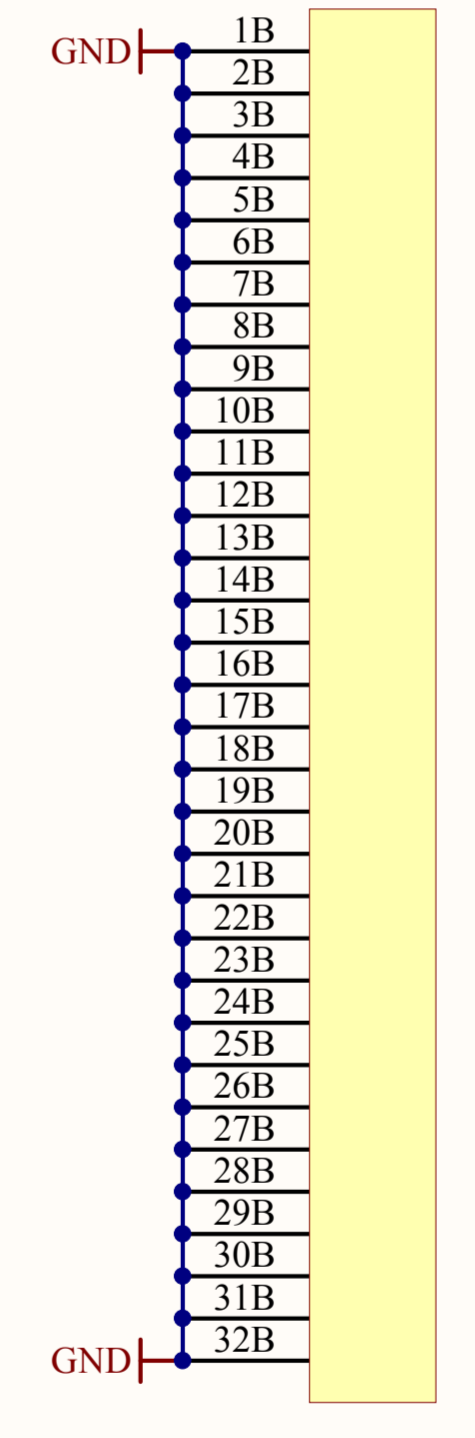
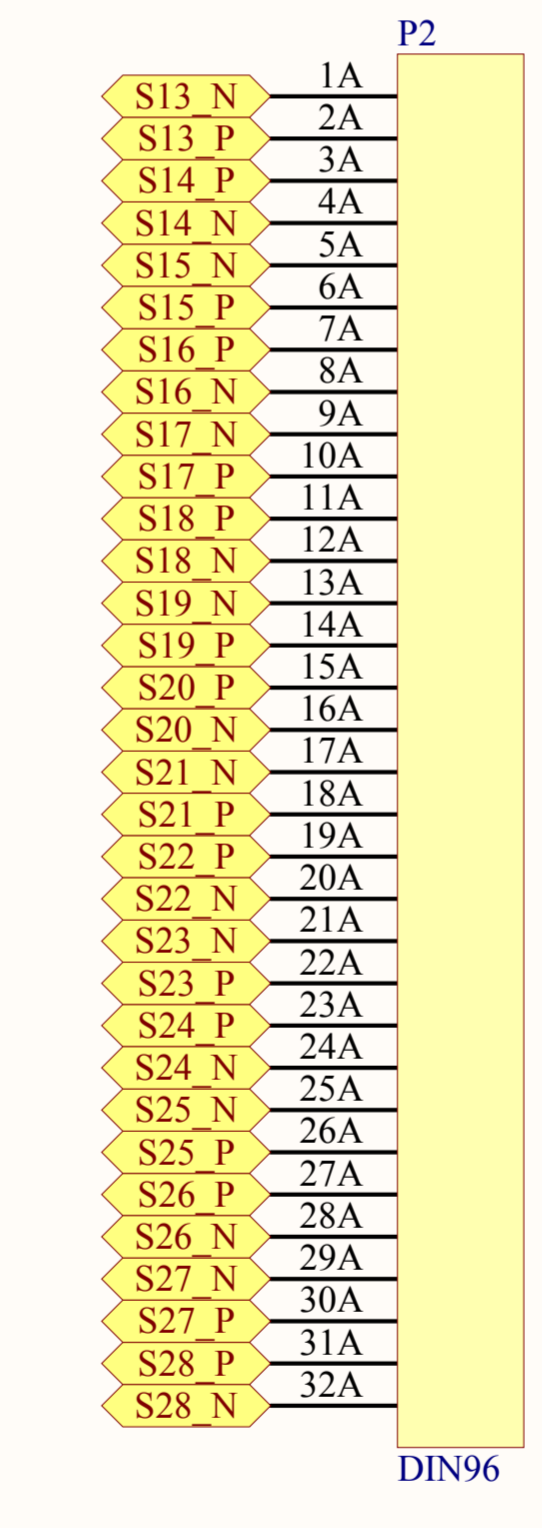
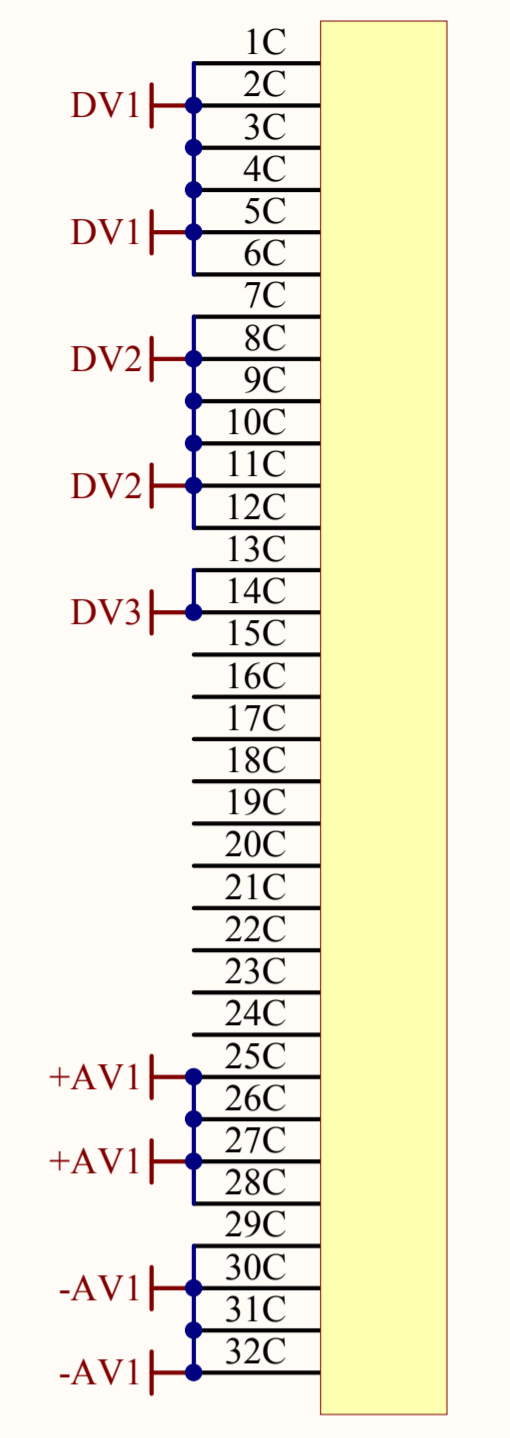
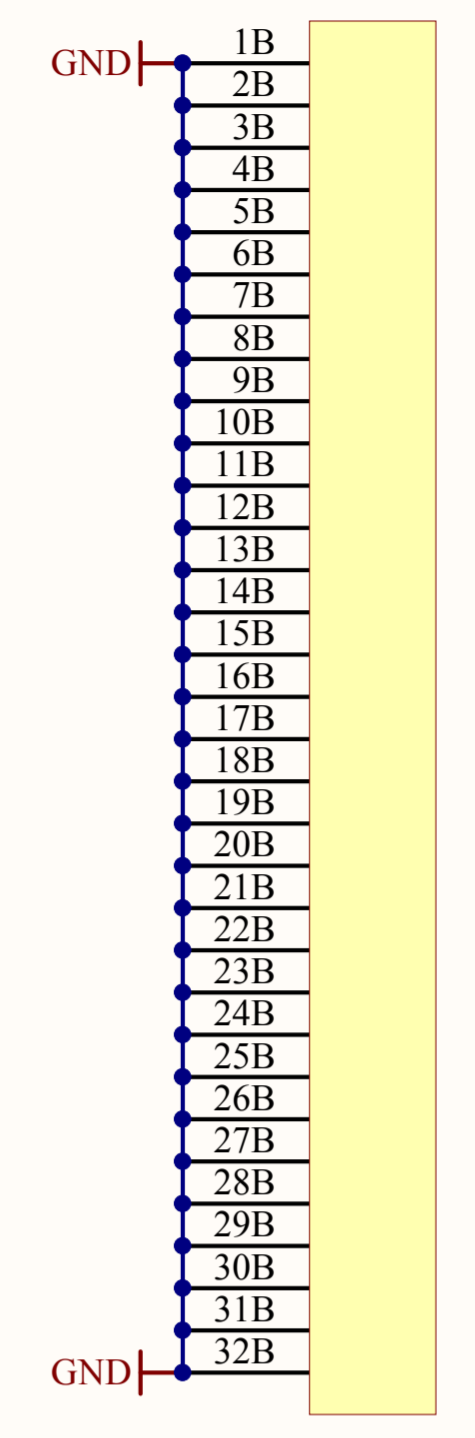
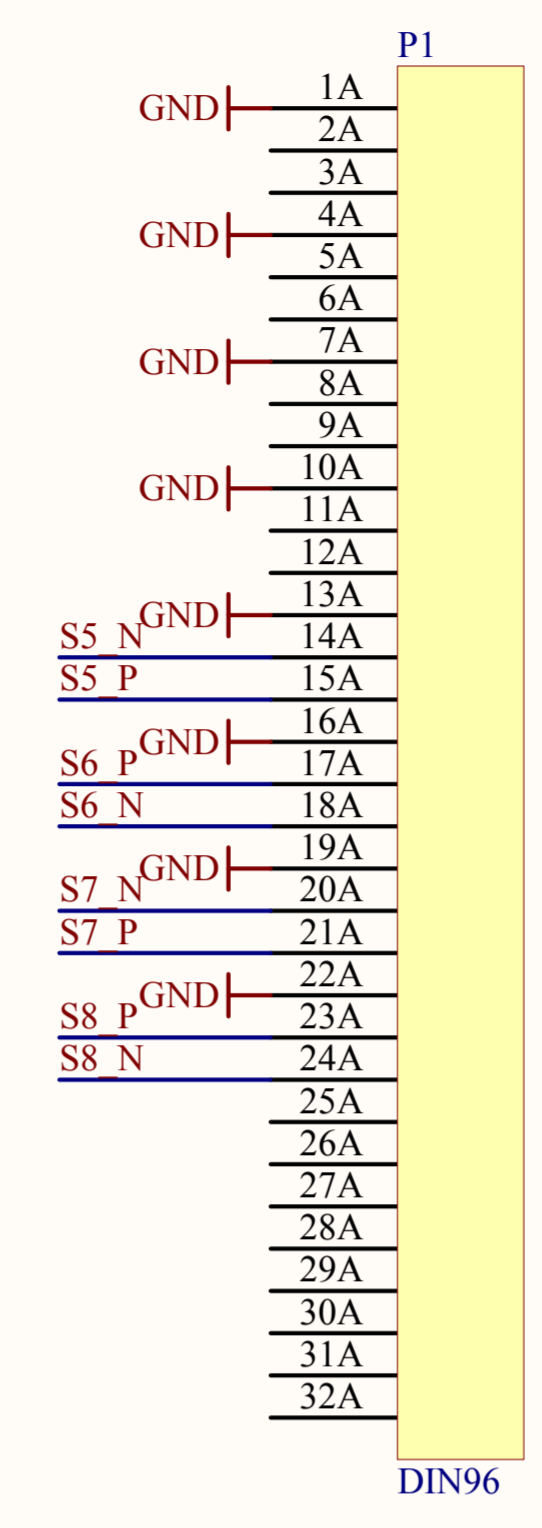
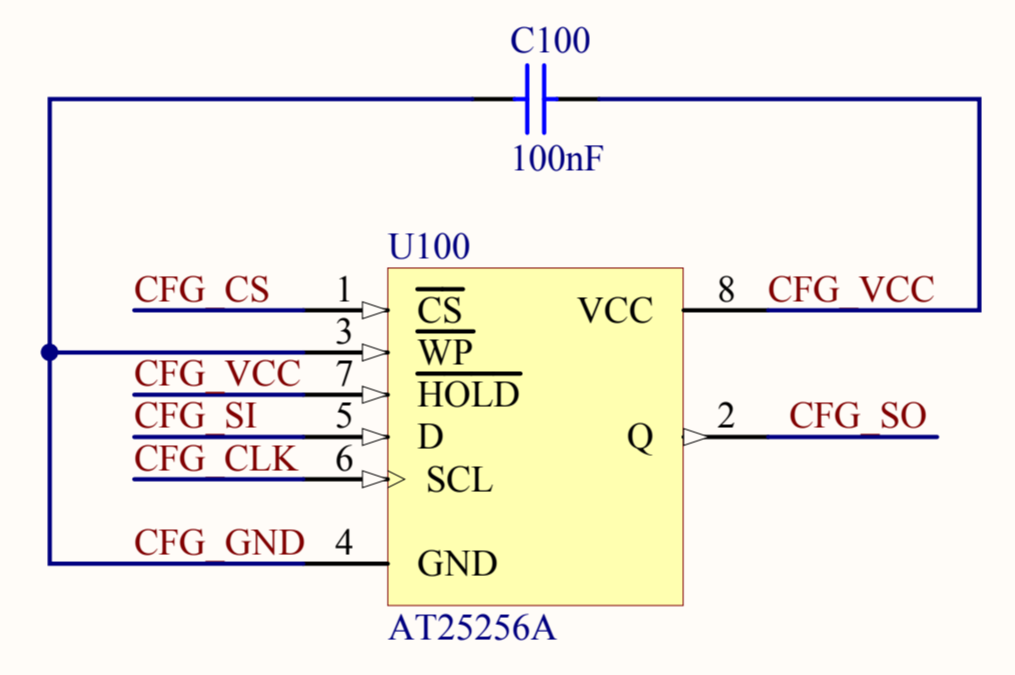
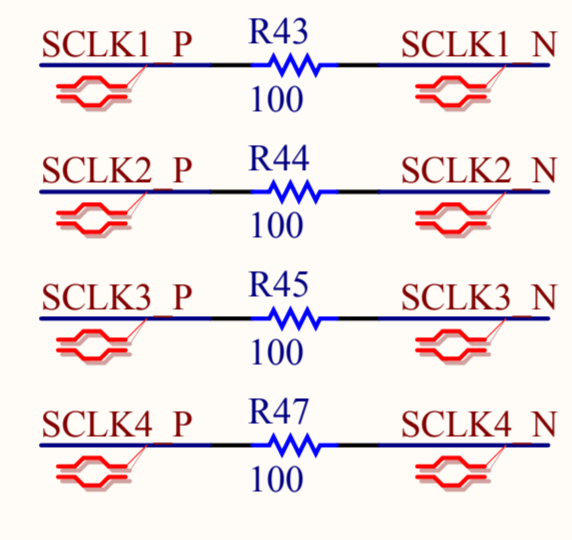
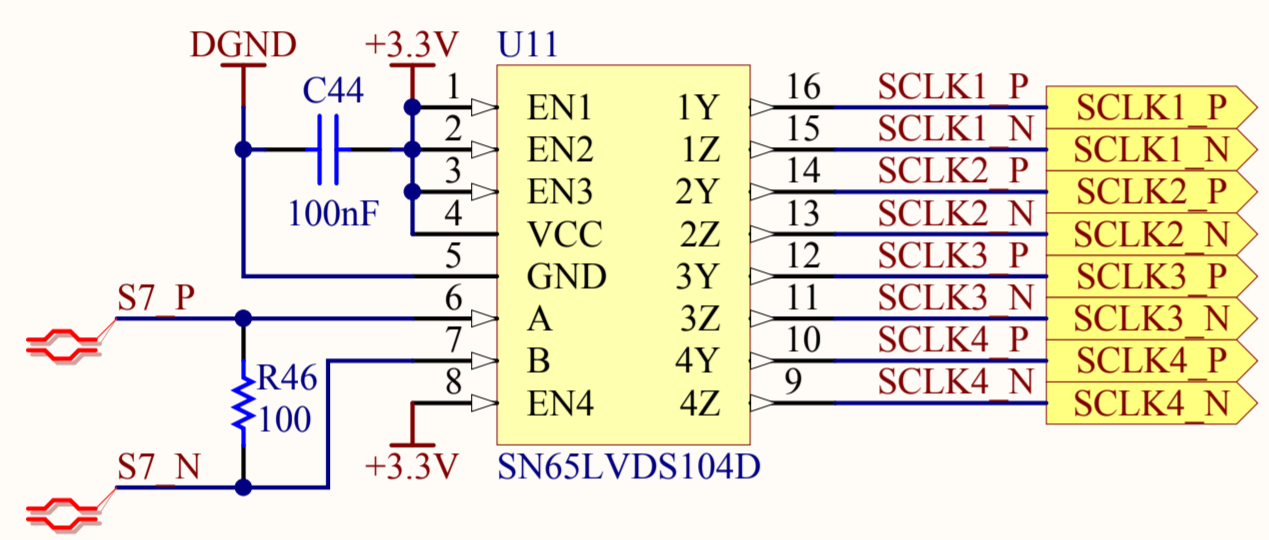
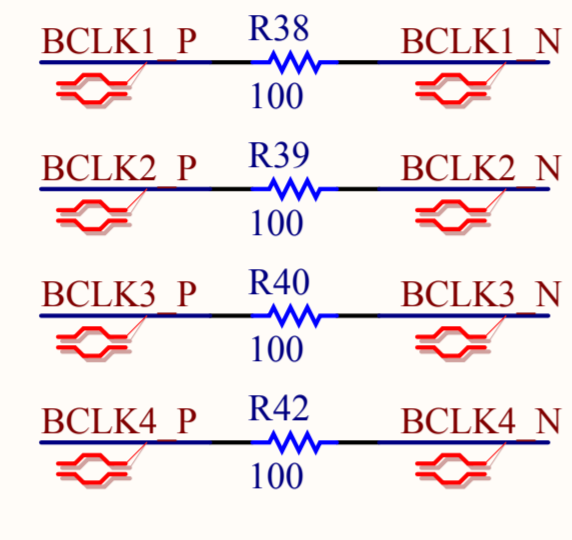
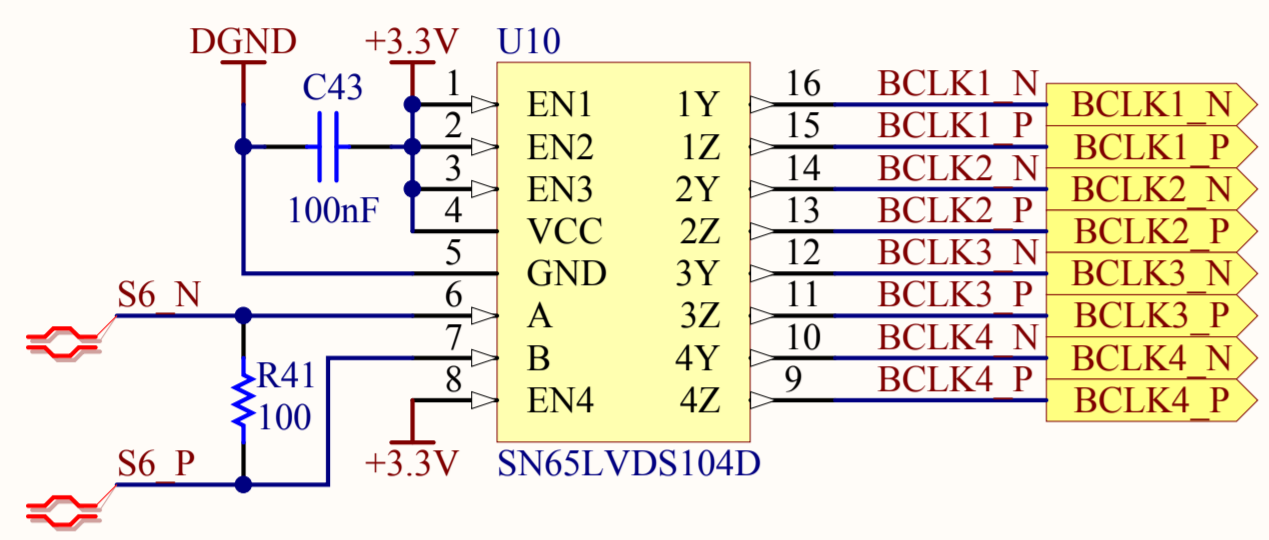
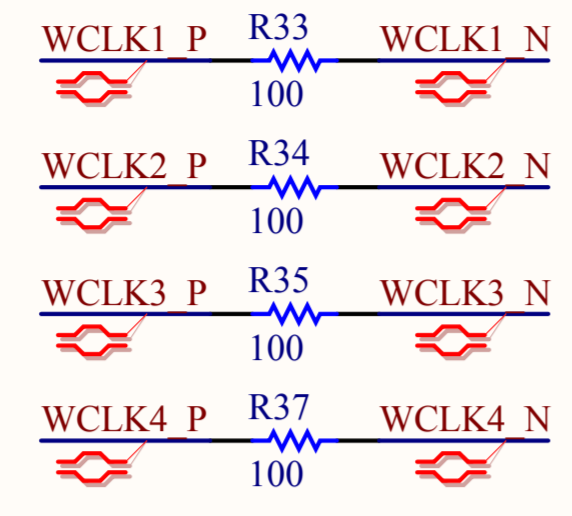
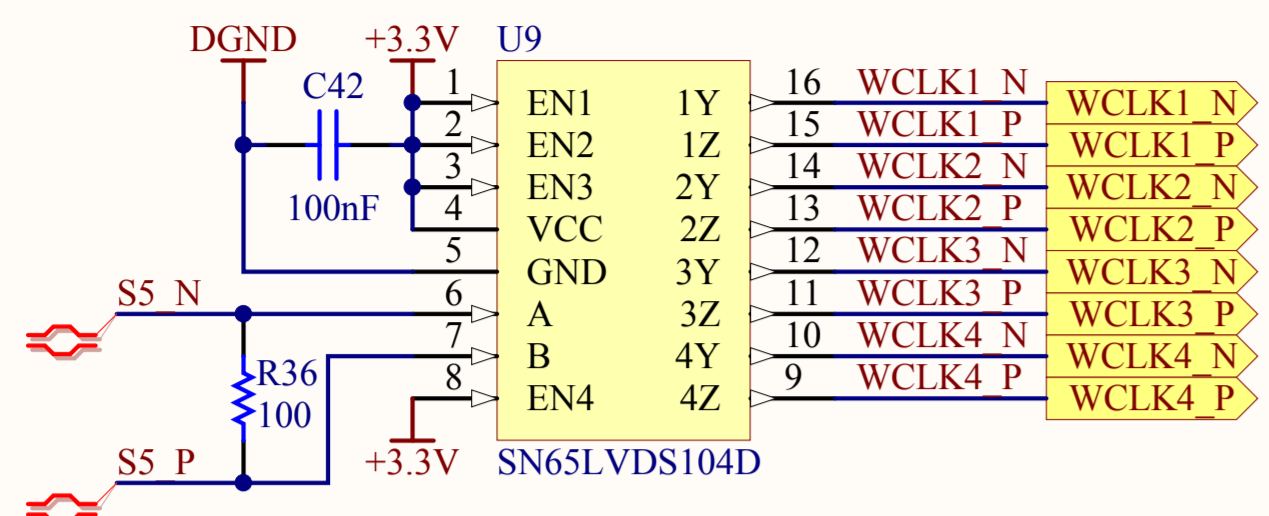
Bypass caps placed between Vcc or Vdd and associated GND pin.



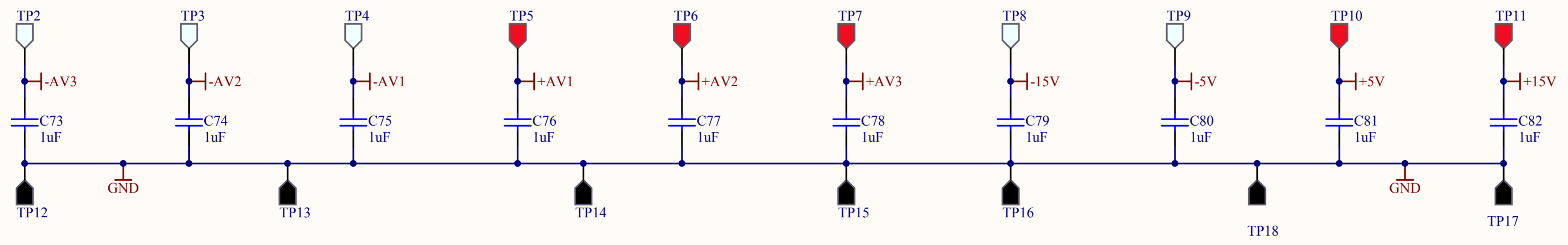
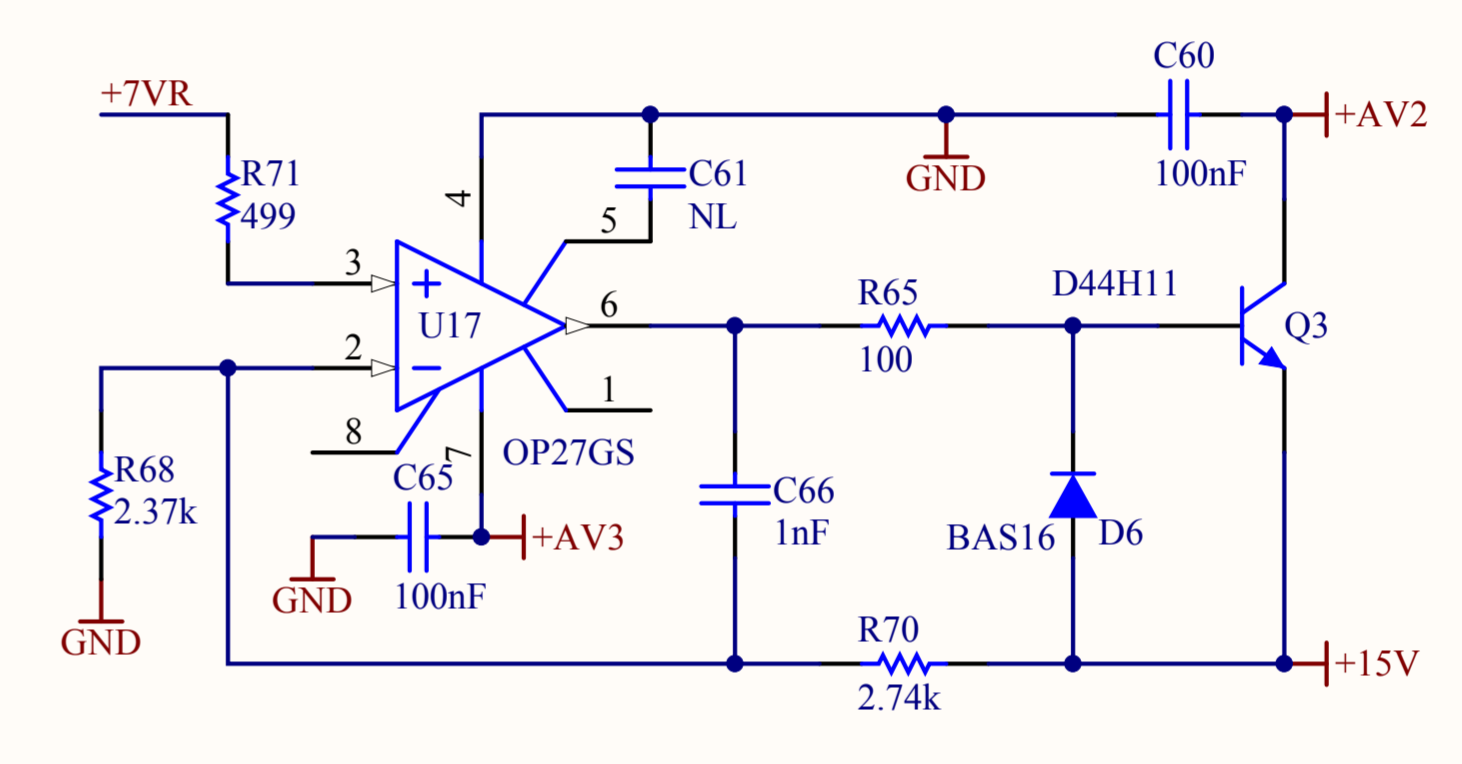
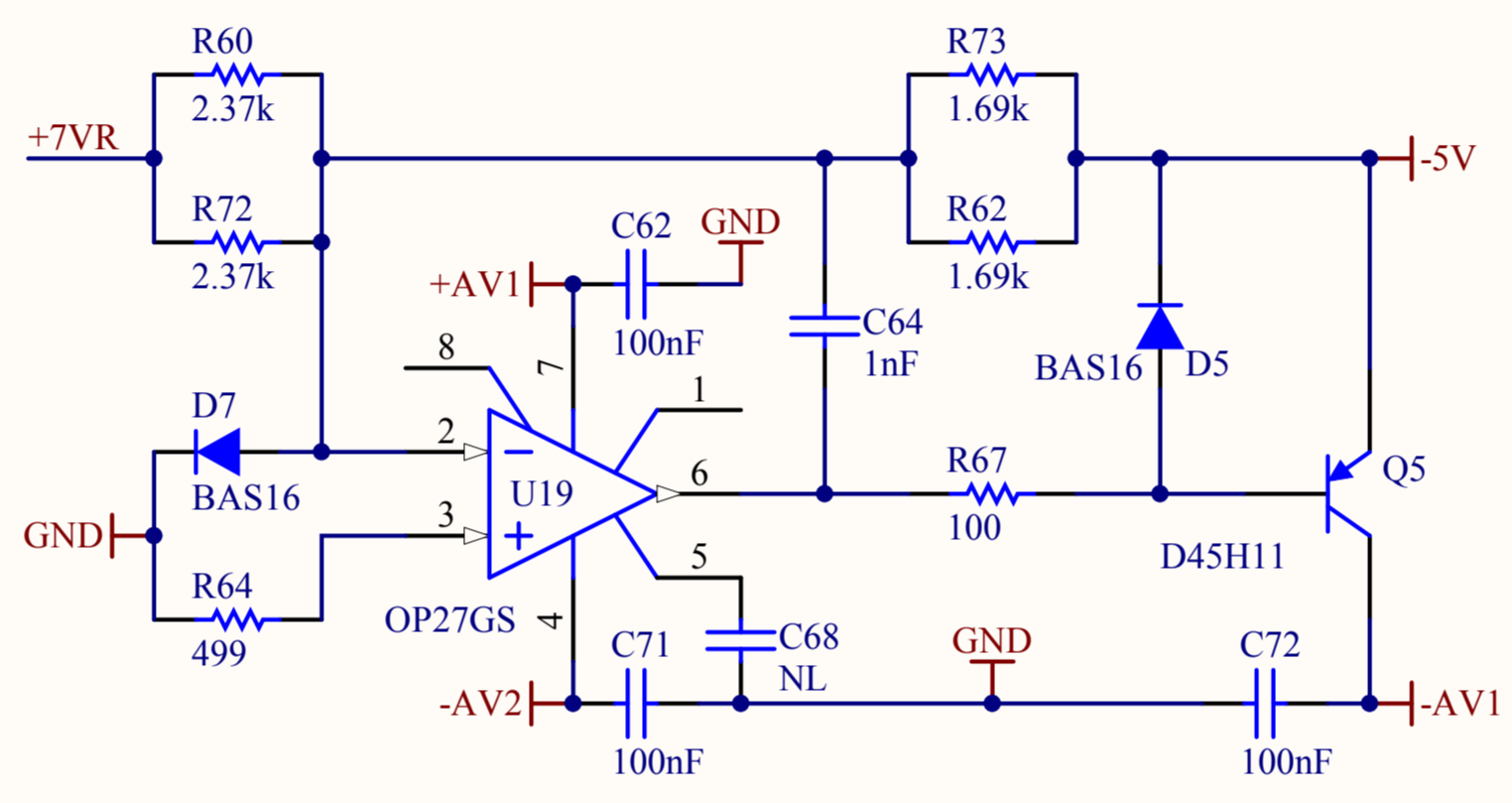
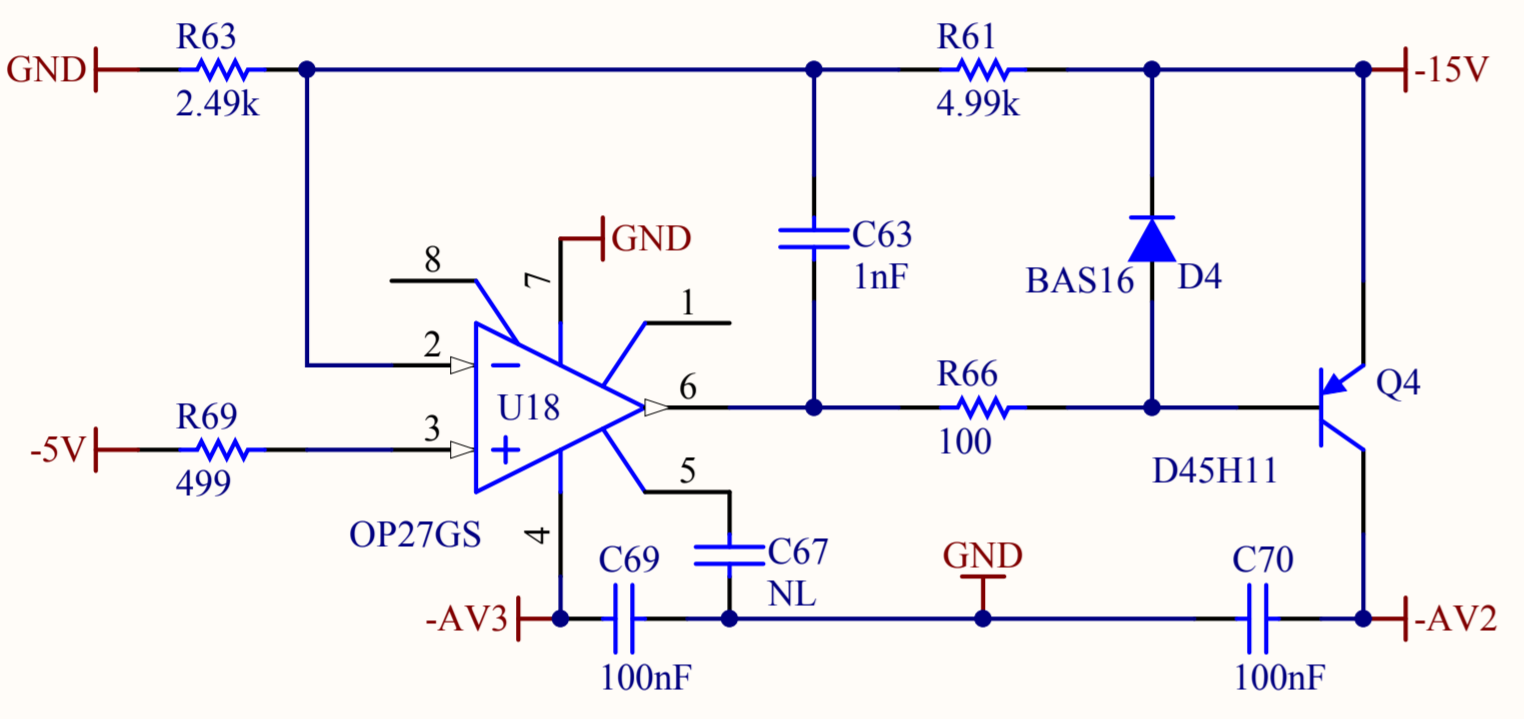
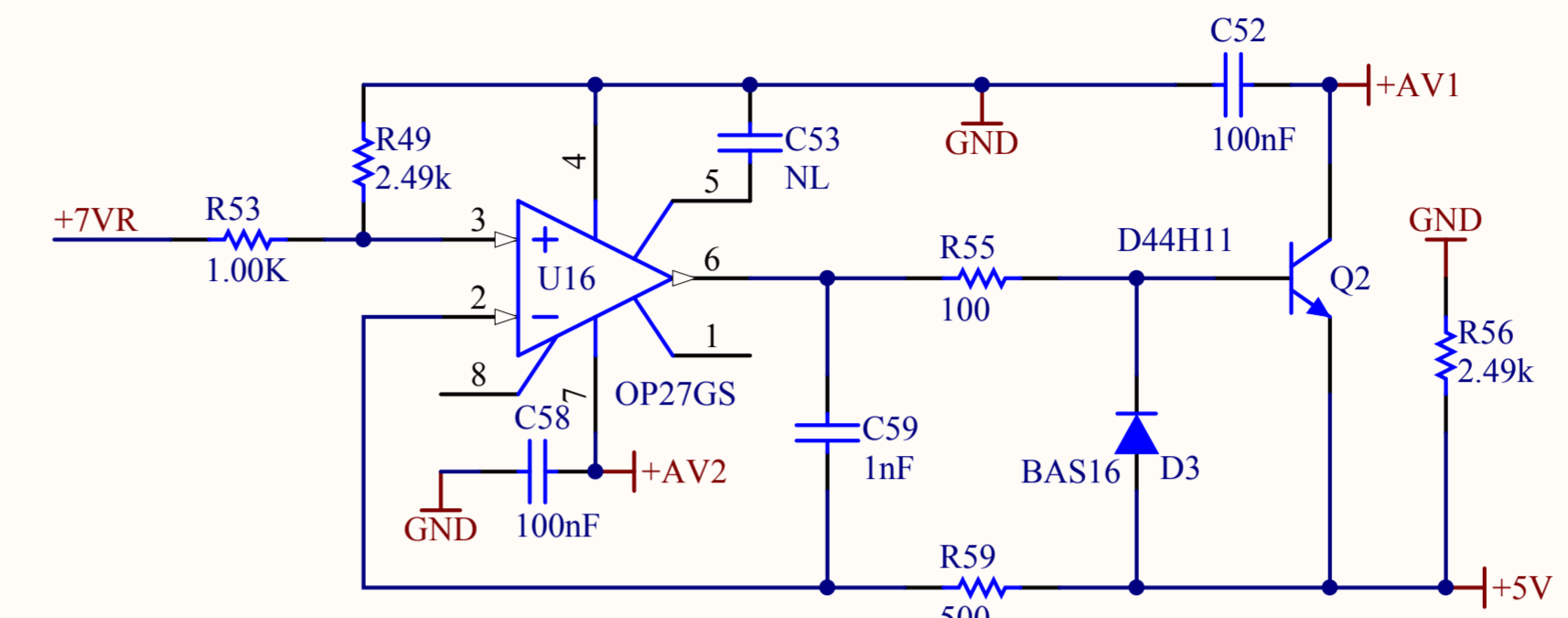
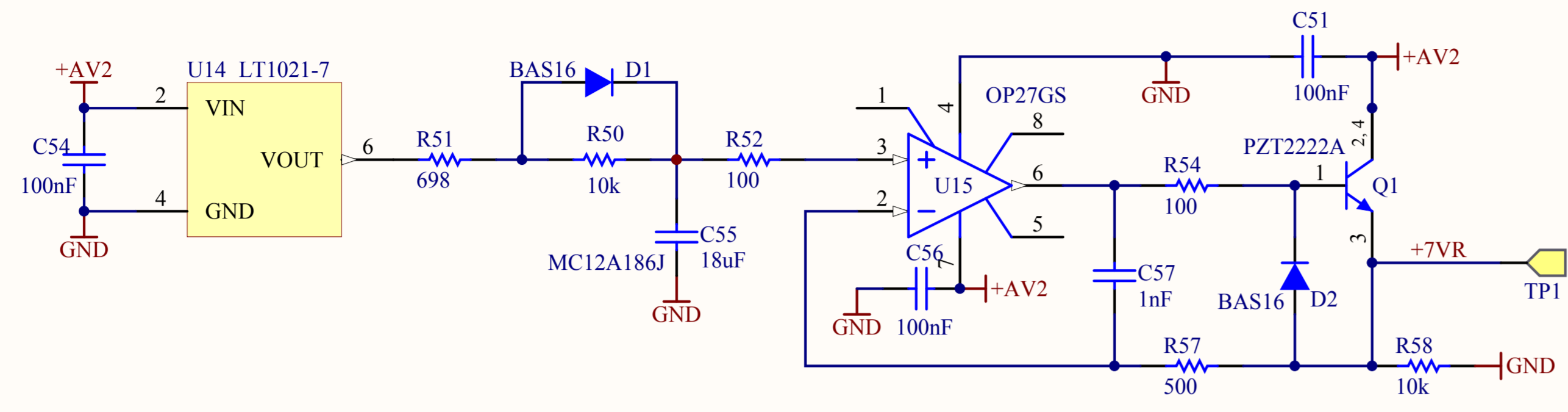
5th order Cheby, 53 kHz cutoff, 0.1 dB ripple



Title		
DAC1794A / DAC Channel		
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B	D060293-00	A			
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File:	E:\LIGO\DAC1794\DAC1794A2.SchDoc	Drawn By:	Paul Schwinberg		



Title			DAC1794A / Analog Power Regulators		
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B	D060293-00	A			
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File:	E:\LIGO\DAC1794\DAC1794A3.SchDoc	Drawn By: Paul Schwinberg			