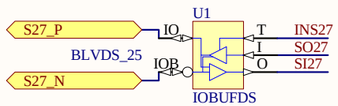

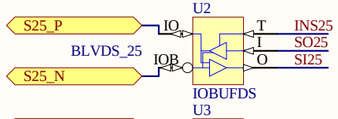

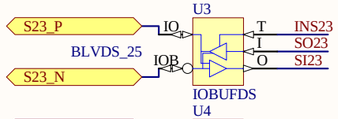

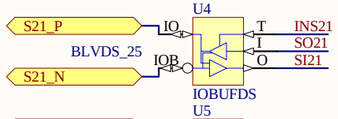

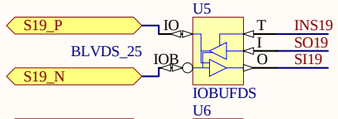

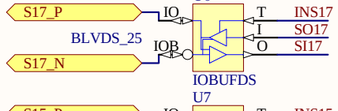

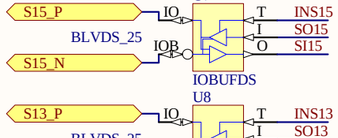

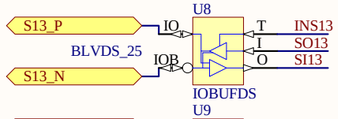

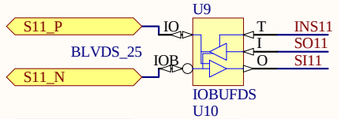

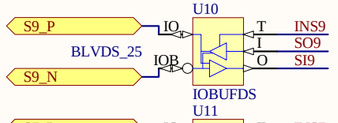

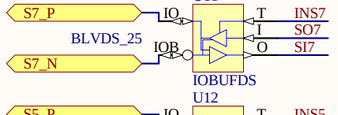

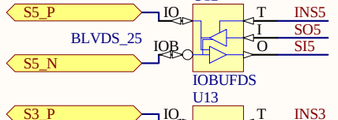

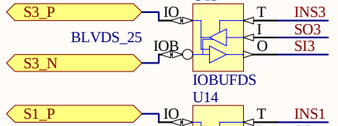

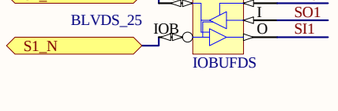

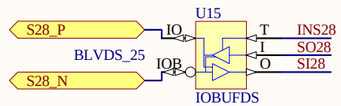

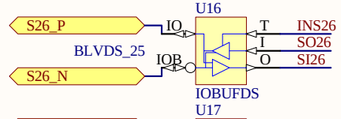

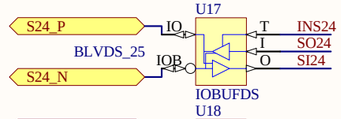

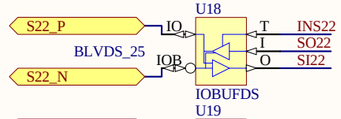

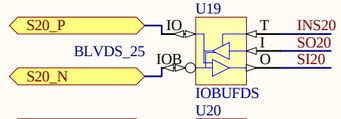

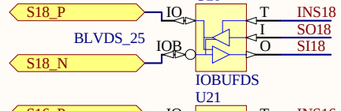

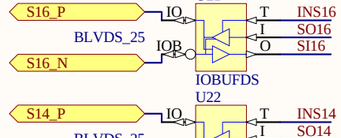

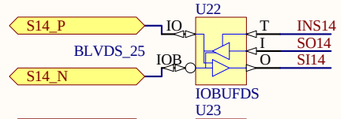

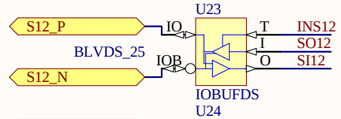

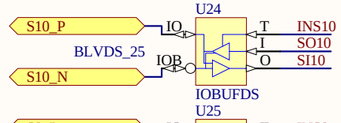

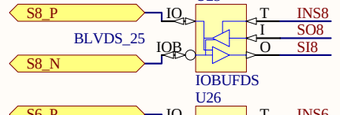

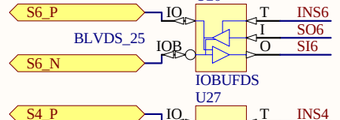

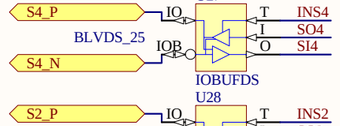

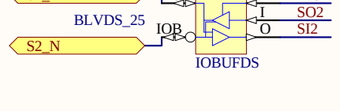

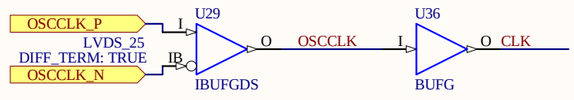

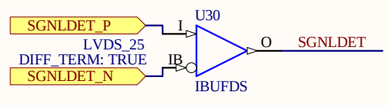

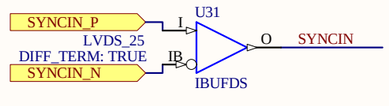

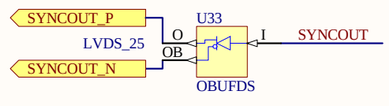

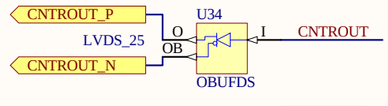

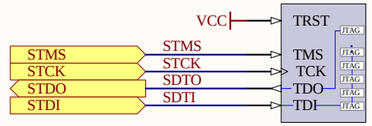

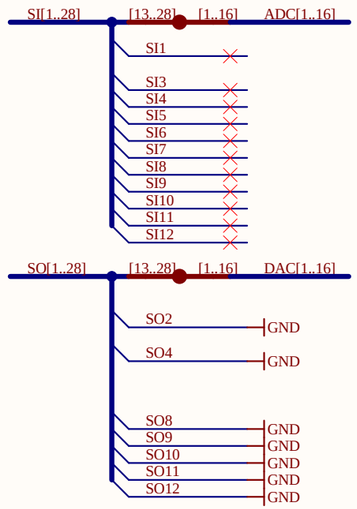

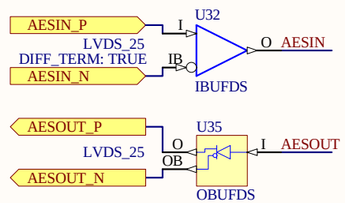

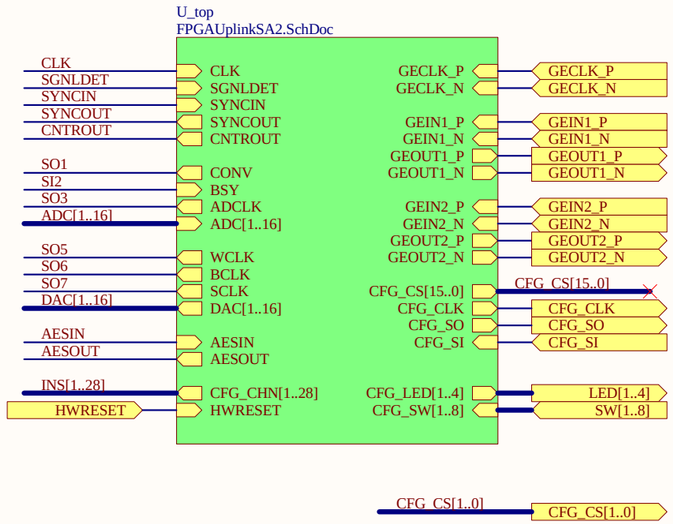

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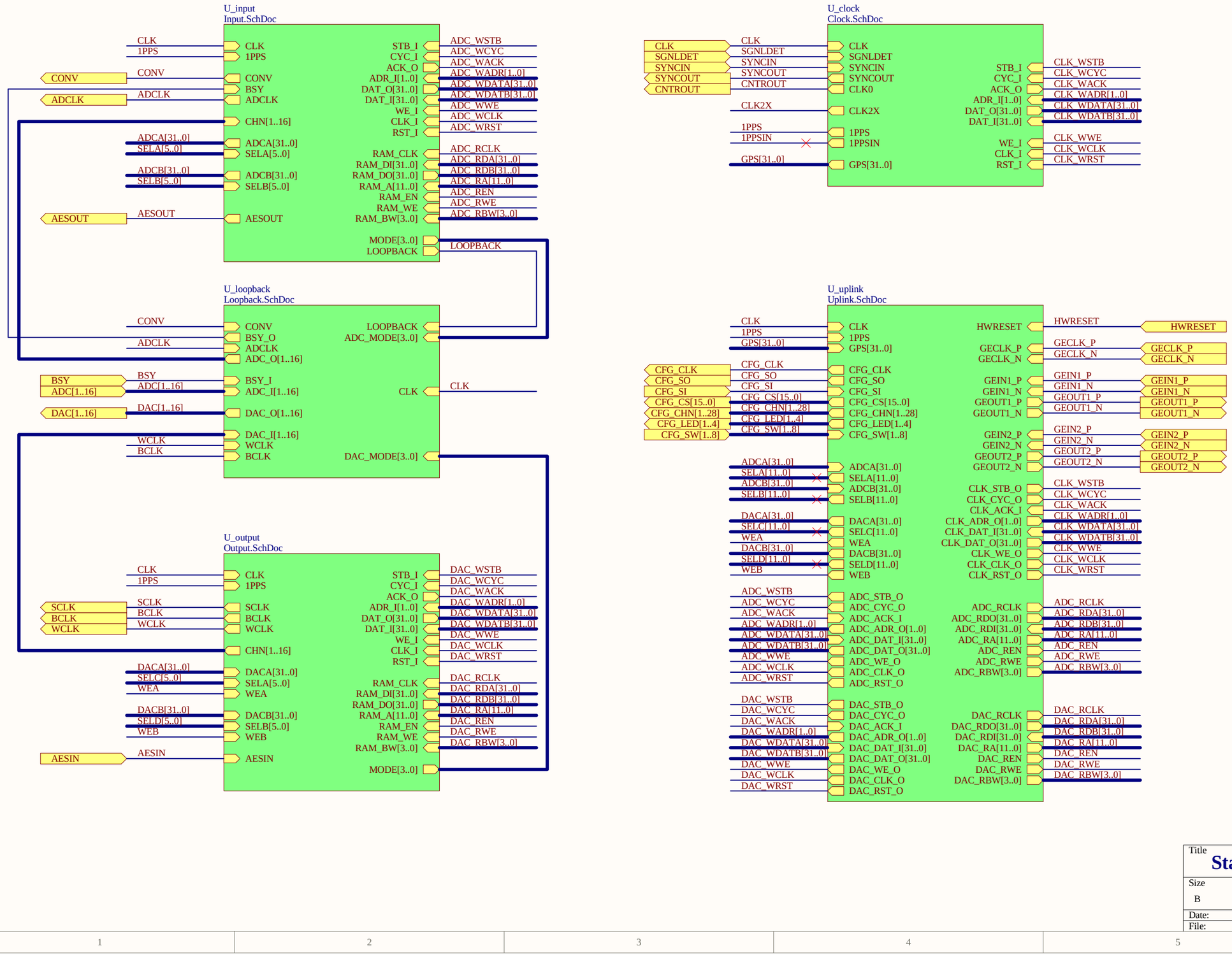

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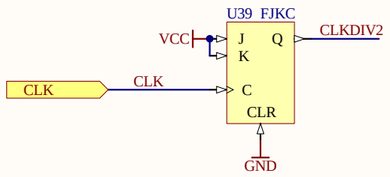

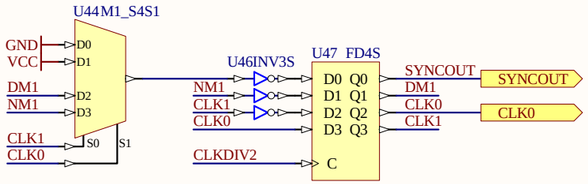

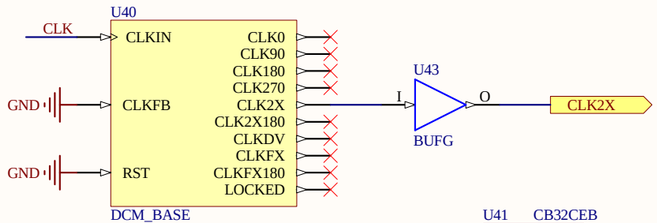

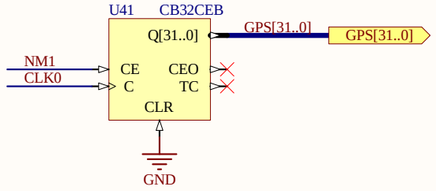

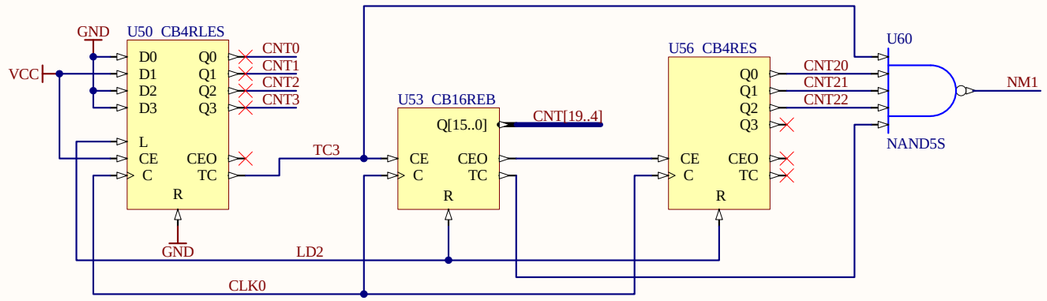

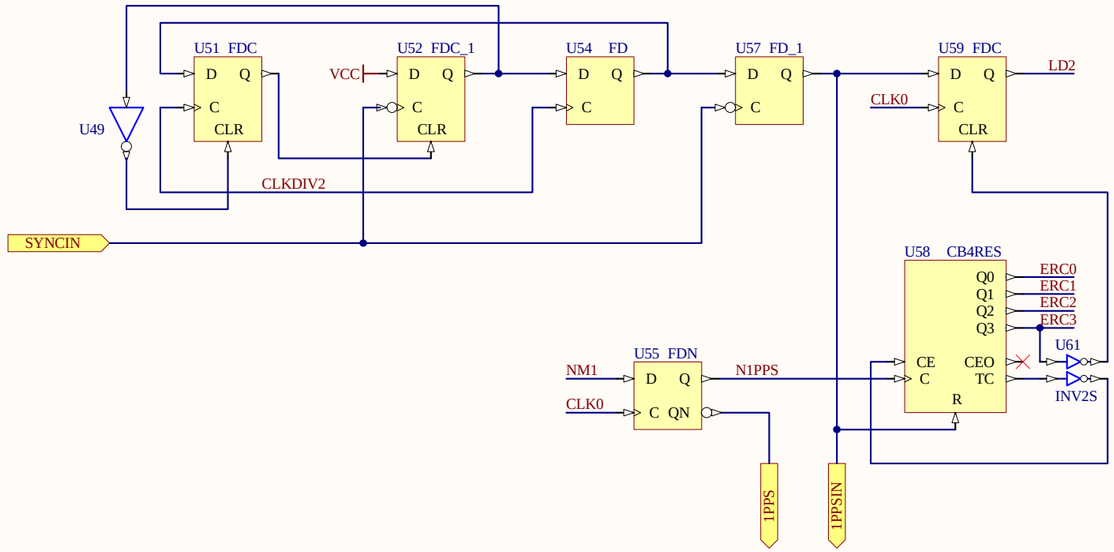

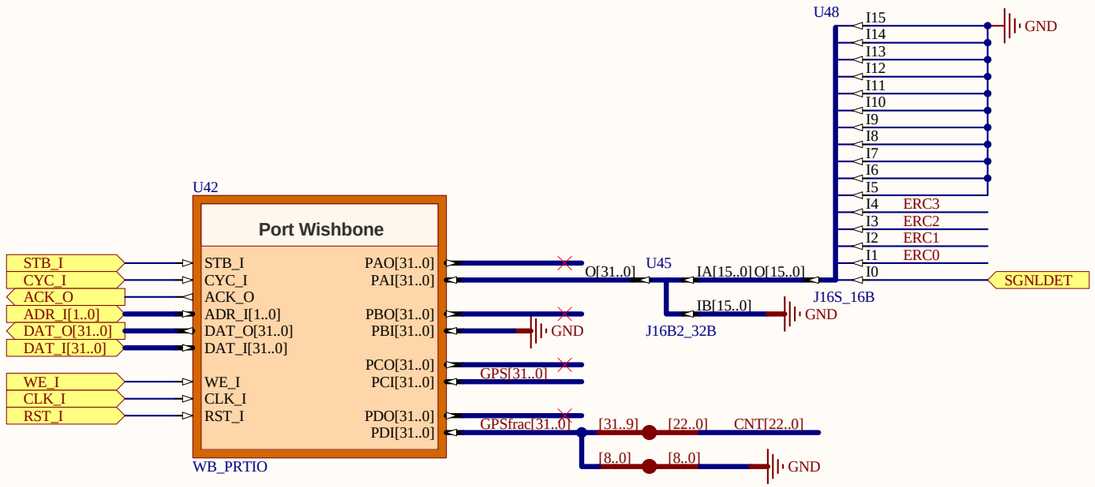

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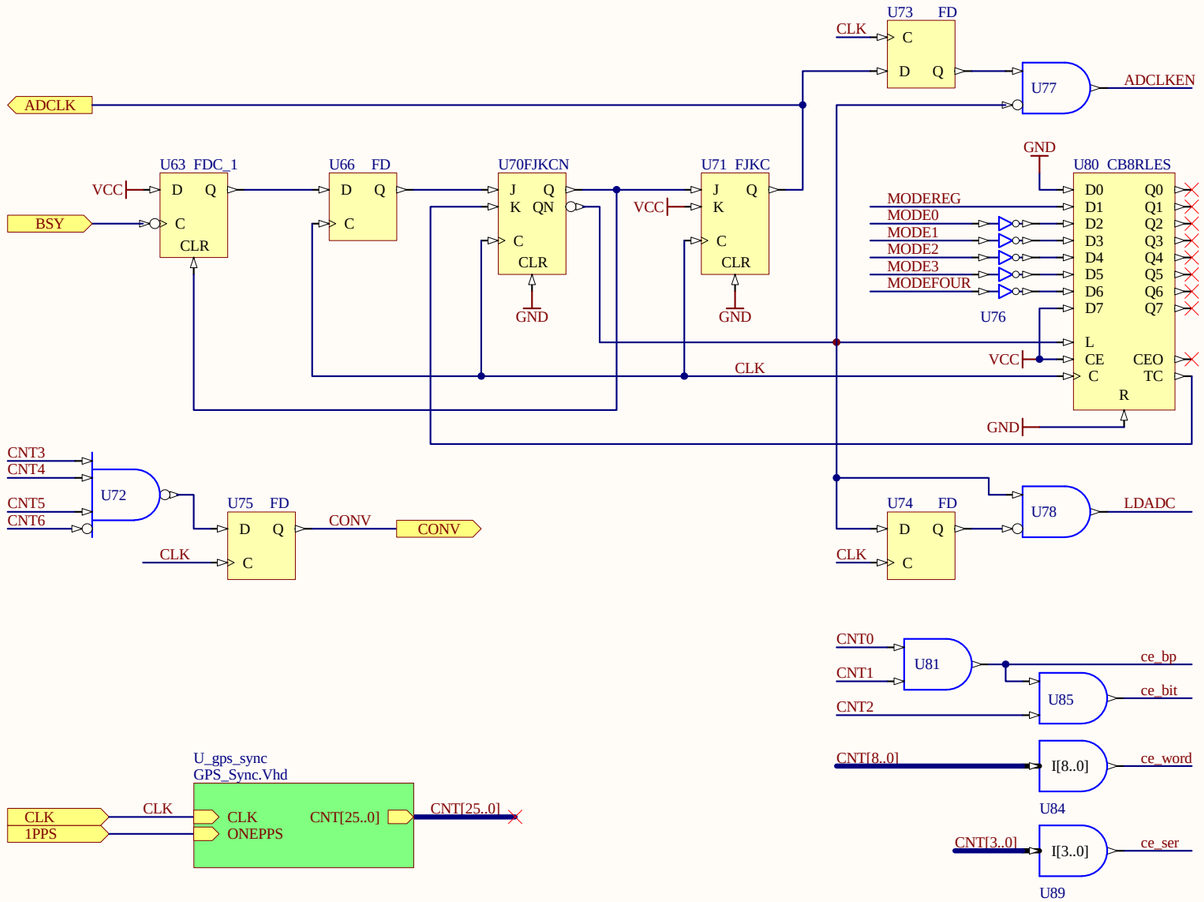

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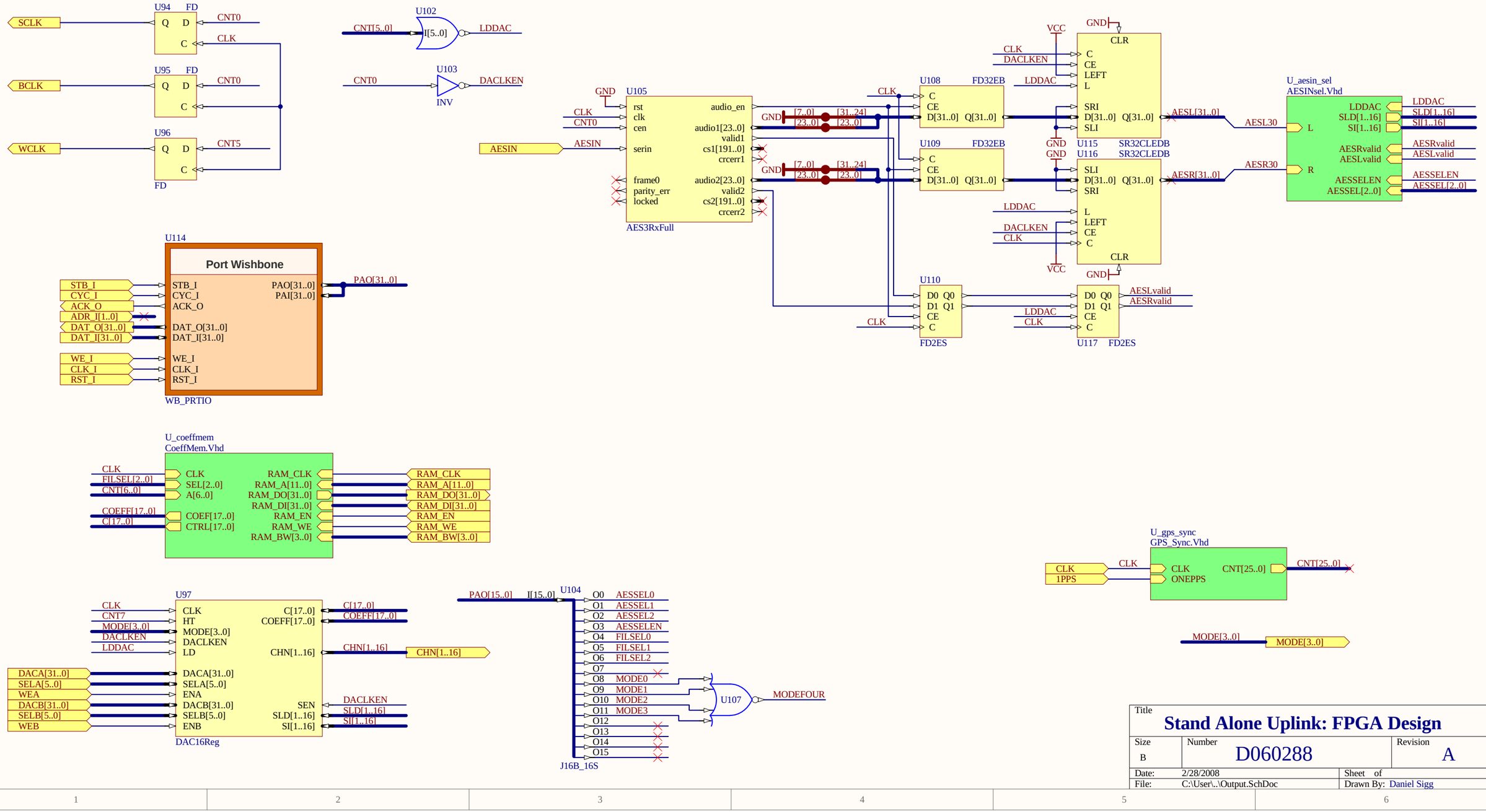

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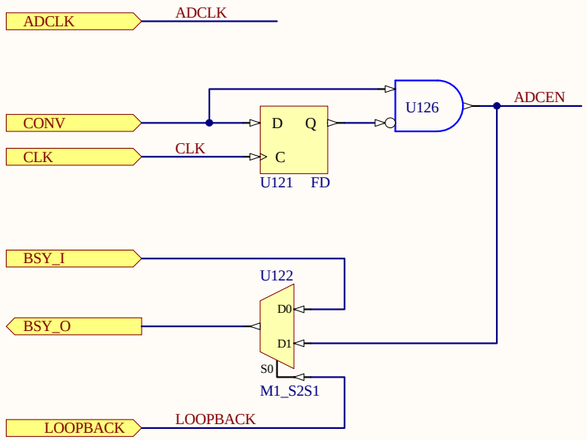

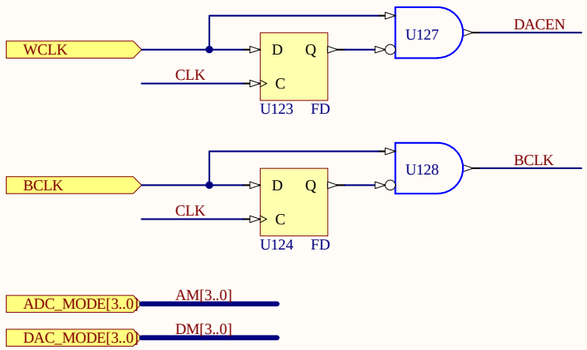

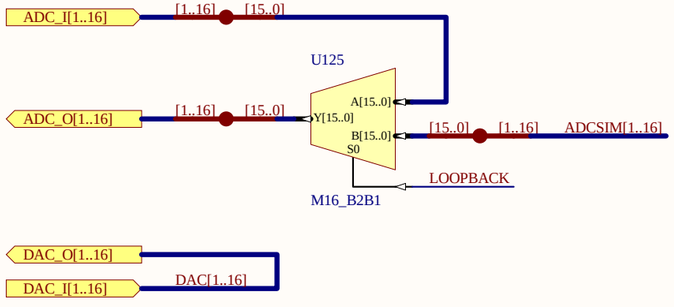

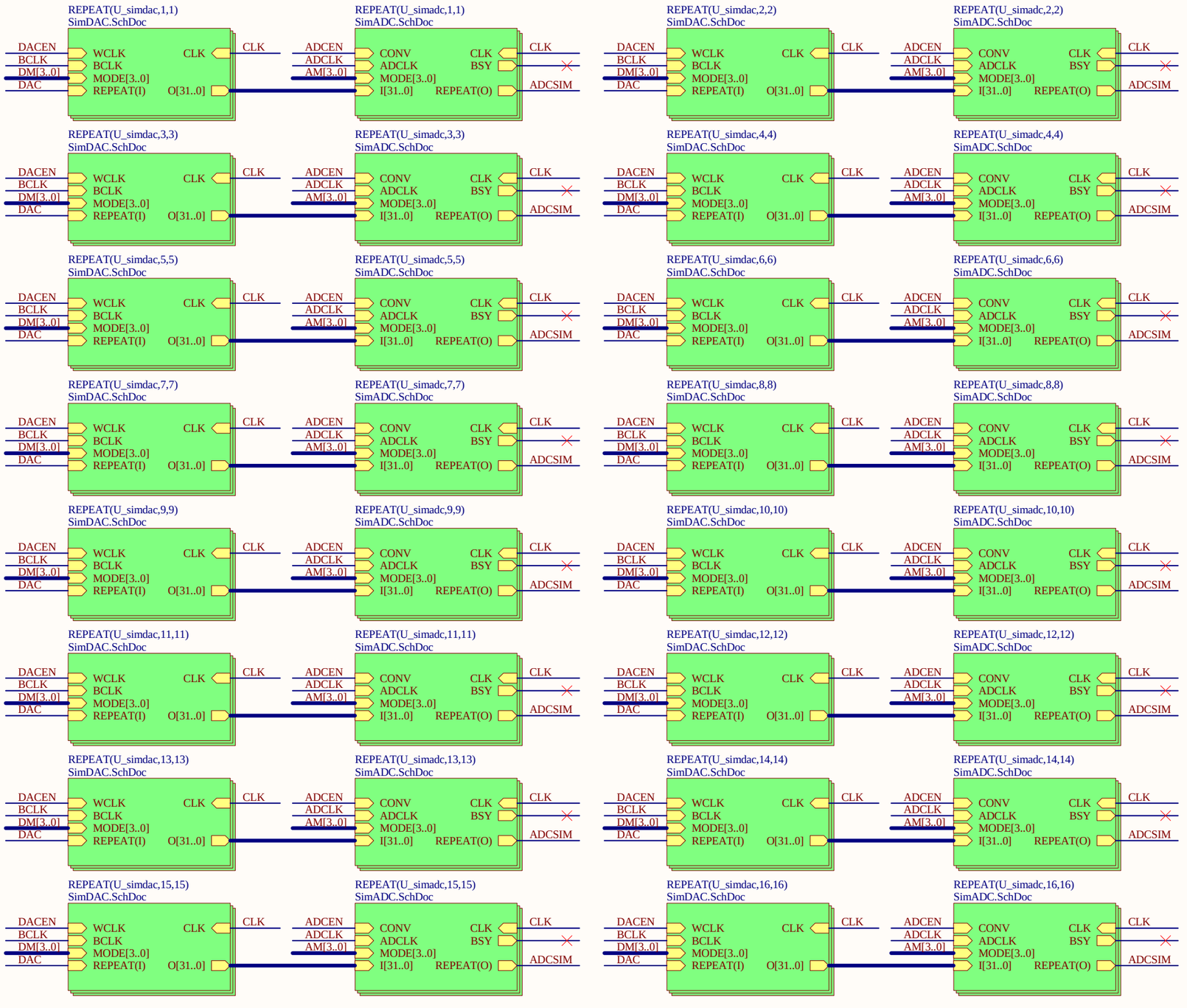

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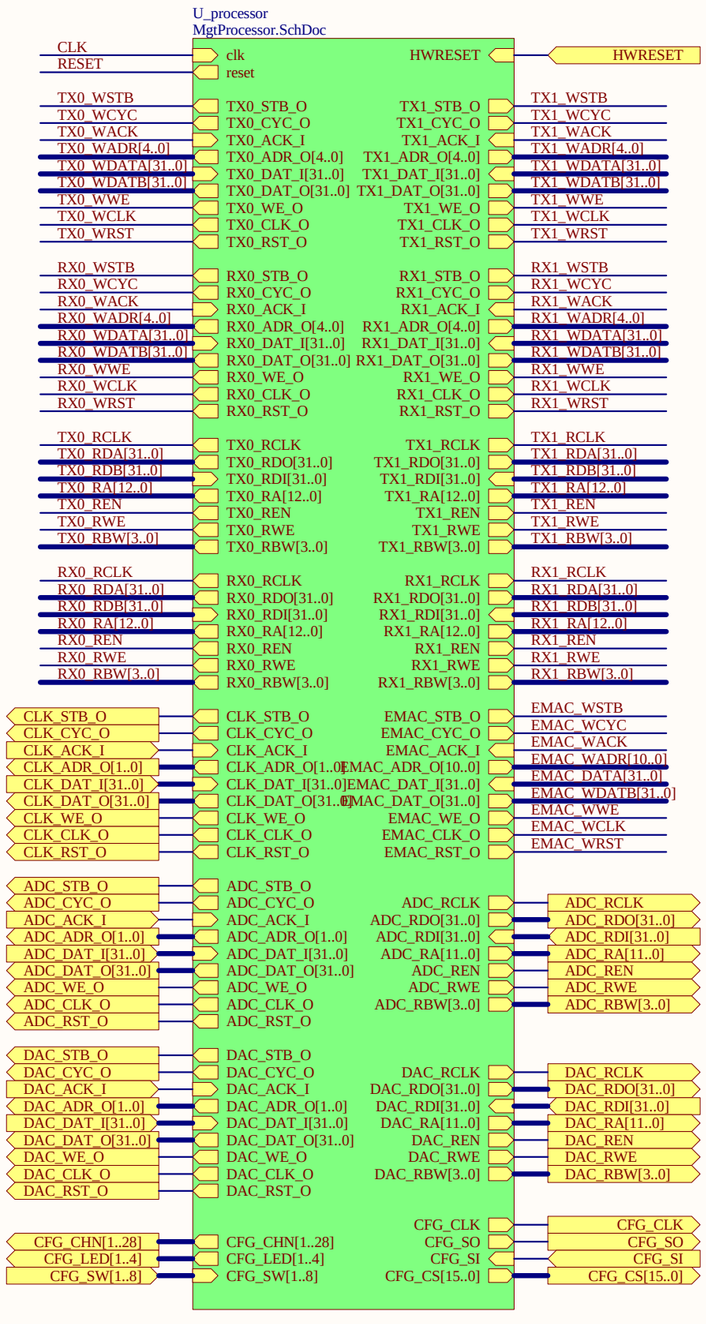

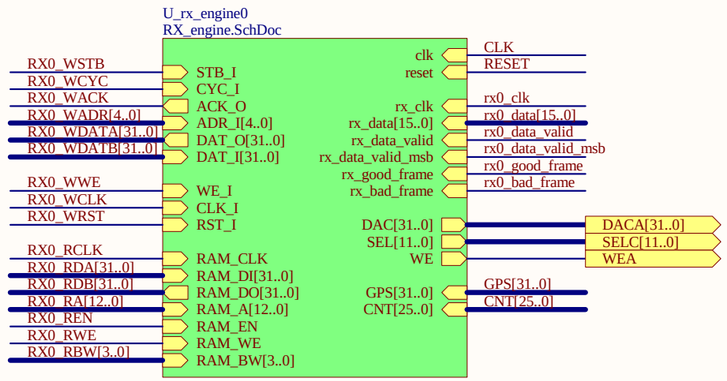

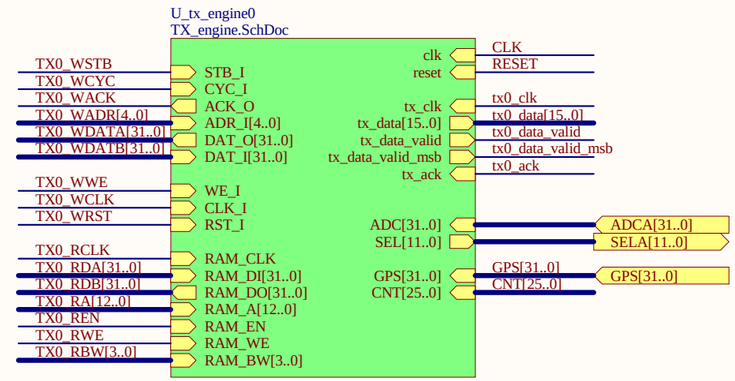

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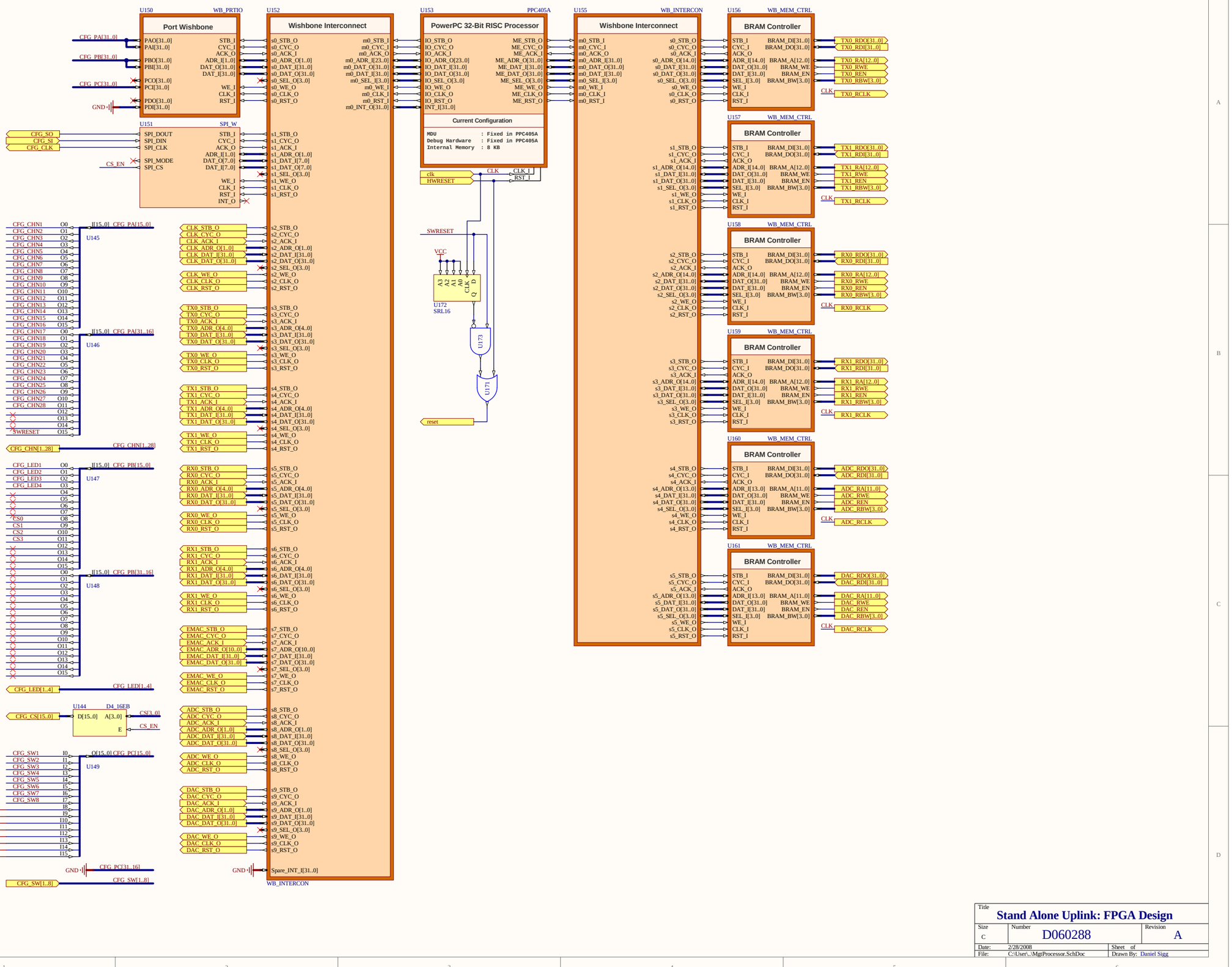
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PBI[31..0]
PCO[31..0]
PCI[31..0]
PDO[31..0]
PDI[31..0]
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CYC_I
ACK_O
ADR_I[1..0]
DAT_O[31..0]
DAT_I[31..0]
WE_I
CLK_I
RST_I
U151 SPI_W
CFG_SO
CFG_SI
CFG_CLK
CS_EN
SPI_DOUT
SPI_DIN
SPI_CLK
SPI_MODE
SPI_CS
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DAT_O[7..0]
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INT_O
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Wishbone Interconnect
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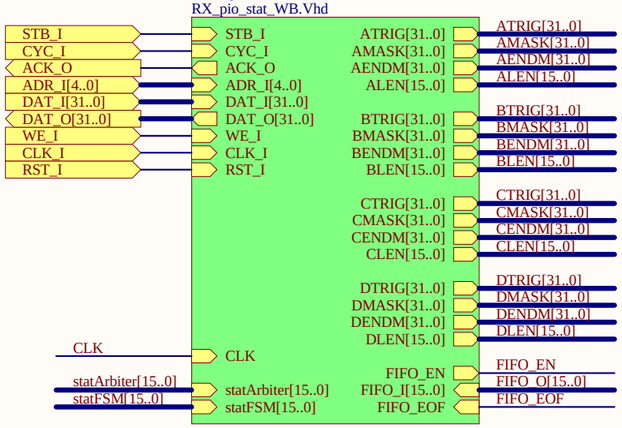
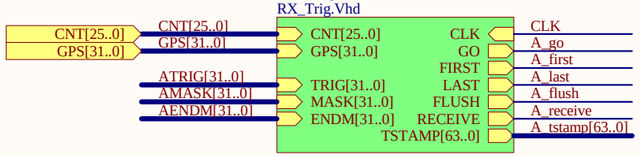
U153 PPC405A
PowerPC 32-Bit RISC Processor
IO_STB_O
IO_CYC_O
IO_ACK_I
IO_ADR_O[23..0]
IO_DAT_I[31..0]
IO_DAT_O[31..0]
IO_SEL_O[3..0]
IO_WE_O
IO_CLK_O
IO_RST_O
INT_I[31..0]
ME_STB_O
ME_CYC_O
ME_ACK_I
ME_ADR_O[31..0]
ME_DAT_I[31..0]
ME_DAT_O[31..0]
ME_SEL_O[3..0]
ME_WE_O
ME_CLK_O
ME_RST_O
Current Configuration
MDU : Fixed in PPC405A
Debug Hardware : Fixed in PPC405A
Internal Memory : 8 KB
clk
HWRESET
CLK
CLK_I
RST_I
SWRESET
VCC
A2
A1
A0
CLK
Q
U172
SRL16
U173
U171
reset
U155 WB_INTERCON
Wishbone Interconnect
m0_STB_I
m0_CYC_I
m0_ACK_O
m0_ADR_I[31..0]
m0_DAT_O[31..0]
m0_DAT_I[31..0]
m0_SEL_I[3..0]
m0_WE_I
m0_CLK_I
m0_RST_I
s0_STB_O
s0_CYC_O
s0_ACK_I
s0_ADR_O[14..0]
s0_DAT_I[31..0]
s0_DAT_O[31..0]
s0_SEL_O[3..0]
s0_WE_O
s0_CLK_O
s0_RST_O
s1_STB_O
s1_CYC_O
s1_ACK_I
s1_ADR_O[14..0]
s1_DAT_I[31..0]
s1_DAT_O[31..0]
s1_SEL_O[3..0]
s1_WE_O
s1_CLK_O
s1_RST_O
s2_STB_O
s2_CYC_O
s2_ACK_I
s2_ADR_O[14..0]
s2_DAT_I[31..0]
s2_DAT_O[31..0]
s2_SEL_O[3..0]
s2_WE_O
s2_CLK_O
s2_RST_O
s3_STB_O
s3_CYC_O
s3_ACK_I
s3_ADR_O[14..0]
s3_DAT_I[31..0]
s3_DAT_O[31..0]
s3_SEL_O[3..0]
s3_WE_O
s3_CLK_O
s3_RST_O
s4_STB_O
s4_CYC_O
s4_ACK_I
s4_ADR_O[13..0]
s4_DAT_I[31..0]
s4_DAT_O[31..0]
s4_SEL_O[3..0]
s4_WE_O
s4_CLK_O
s4_RST_O
s5_STB_O
s5_CYC_O
s5_ACK_I
s5_ADR_O[13..0]
s5_DAT_I[31..0]
s5_DAT_O[31..0]
s5_SEL_O[3..0]
s5_WE_O
s5_CLK_O
s5_RST_O
U156 WB_MEM_CTRL
BRAM Controller
STB_I
CYC_I
ACK_O
ADR_I[14..0]
DAT_O[31..0]
DAT_I[31..0]
SEL_I[3..0]
WE_I
CLK_I
RST_I
BRAM_DI[31..0]
BRAM_DO[31..0]
BRAM_A[12..0]
BRAM_WE
BRAM_EN
BRAM_BW[3..0]
TX0_RDO[31..0]
TX0_RDI[31..0]
TX0_RA[12..0]
TX0_RWE
TX0_REN
TX0_RBW[3..0]
TX0_RCLK
U157 WB_MEM_CTRL
TX1_RDO[31..0]
TX1_RDI[31..0]
TX1_RA[12..0]
TX1_RWE
TX1_REN
TX1_RBW[3..0]
TX1_RCLK
U158 WB_MEM_CTRL
RX0_RDO[31..0]
RX0_RDI[31..0]
RX0_RA[12..0]
RX0_RWE
RX0_REN
RX0_RBW[3..0]
RX0_RCLK
U159 WB_MEM_CTRL
RX1_RDO[31..0]
RX1_RDI[31..0]
RX1_RA[12..0]
RX1_RWE
RX1_REN
RX1_RBW[3..0]
RX1_RCLK
U160 WB_MEM_CTRL
ADC_RDO[31..0]
ADC_RDI[31..0]
ADC_RA[11..0]
ADC_RWE
ADC_REN
ADC_RBW[3..0]
ADC_RCLK
U161 WB_MEM_CTRL
DAC_RDO[31..0]
DAC_RDI[31..0]
DAC_RA[11..0]
DAC_RWE
DAC_REN
DAC_RBW[3..0]
DAC_RCLK
CFG_CHN1 O0
CFG_CHN2 O1
CFG_CHN3 O2
CFG_CHN4 O3
CFG_CHN5 O4
CFG_CHN6 O5
CFG_CHN7 O6
CFG_CHN8 O7
CFG_CHN9 O8
CFG_CHN10 O9
CFG_CHN11 O10
CFG_CHN12 O11
CFG_CHN13 O12
CFG_CHN14 O13
CFG_CHN15 O14
CFG_CHN16 O15
CFG_CHN17 O0
CFG_CHN18 O1
CFG_CHN19 O2
CFG_CHN20 O3
CFG_CHN21 O4
CFG_CHN22 O5
CFG_CHN23 O6
CFG_CHN24 O7
CFG_CHN25 O8
CFG_CHN26 O9
CFG_CHN27 O10
CFG_CHN28 O11
O12
O13
O14
SWRESET O15
I[15..0] CFG_PA[15..0]
U145
I[15..0] CFG_PA[31..16]
U146
CFG_CHN[1..28]
CFG_LED1 O0
CFG_LED2 O1
CFG_LED3 O2
CFG_LED4 O3
O4
O5
O6
O7
CS0 O8
CS1 O9
CS2 O10
CS3 O11
O12
O13
O14
O15
I[15..0] CFG_PB[15..0]
U147
O0
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
O11
O12
O13
O14
O15
I[15..0] CFG_PB[31..16]
U148
CFG_LED[1..4]
U144 D4_16EB
CFG_CS[15..0]
D[15..0]
A[3..0]
E
CS[3..0]
CS_EN
CFG_SW1 I0
CFG_SW2 I1
CFG_SW3 I2
CFG_SW4 I3
CFG_SW5 I4
CFG_SW6 I5
CFG_SW7 I6
CFG_SW8 I7
GND I8
GND I9
GND I10
GND I11
GND I12
GND I13
GND I14
GND I15
O[15..0] CFG_PC[15..0]
U149
GND
CFG_PC[31..16]
CFG_SW[1..8]
CLK_STB_O
CLK_CYC_O
CLK_ACK_I
CLK_ADR_O[1..0]
CLK_DAT_I[31..0]
CLK_DAT_O[31..0]
CLK_WE_O
CLK_CLK_O
CLK_RST_O
TX0_STB_O
TX0_CYC_O
TX0_ACK_I
TX0_ADR_O[4..0]
TX0_DAT_I[31..0]
TX0_DAT_O[31..0]
TX0_WE_O
TX0_CLK_O
TX0_RST_O
TX1_STB_O
TX1_CYC_O
TX1_ACK_I
TX1_ADR_O[4..0]
TX1_DAT_I[31..0]
TX1_DAT_O[31..0]
TX1_WE_O
TX1_CLK_O
TX1_RST_O
RX0_STB_O
RX0_CYC_O
RX0_ACK_I
RX0_ADR_O[4..0]
RX0_DAT_I[31..0]
RX0_DAT_O[31..0]
RX0_WE_O
RX0_CLK_O
RX0_RST_O
RX1_STB_O
RX1_CYC_O
RX1_ACK_I
RX1_ADR_O[4..0]
RX1_DAT_I[31..0]
RX1_DAT_O[31..0]
RX1_WE_O
RX1_CLK_O
RX1_RST_O
EMAC_STB_O
EMAC_CYC_O
EMAC_ACK_I
EMAC_ADR_O[10..0]
EMAC_DAT_I[31..0]
EMAC_DAT_O[31..0]
EMAC_WE_O
EMAC_CLK_O
EMAC_RST_O
ADC_STB_O
ADC_CYC_O
ADC_ACK_I
ADC_ADR_O[1..0]
ADC_DAT_I[31..0]
ADC_DAT_O[31..0]
ADC_WE_O
ADC_CLK_O
ADC_RST_O
DAC_STB_O
DAC_CYC_O
DAC_ACK_I
DAC_ADR_O[1..0]
DAC_DAT_I[31..0]
DAC_DAT_O[31..0]
DAC_WE_O
DAC_CLK_O
DAC_RST_O
GND
Spare_INT_I[31..0]
WB_INTERCON
Title
Stand Alone Uplink: FPGA Design
Size C
Number D060288
Revision A
Date: 2/28/2008
Sheet of
File: C:\User\..\MgtProcessor.SchDoc
Drawn By: Daniel Sigg

U_rx_pio_stat_wb
RX_pio_stat_WB.Vhd



U_rx_trig_A
RX_Trig.Vhd



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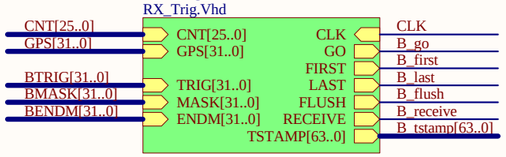
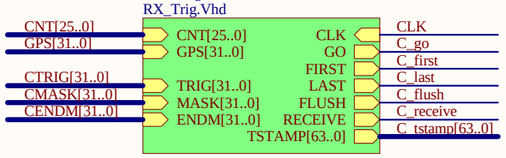
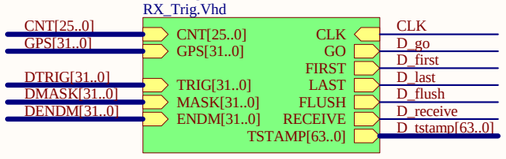
RX_Trig.Vhd



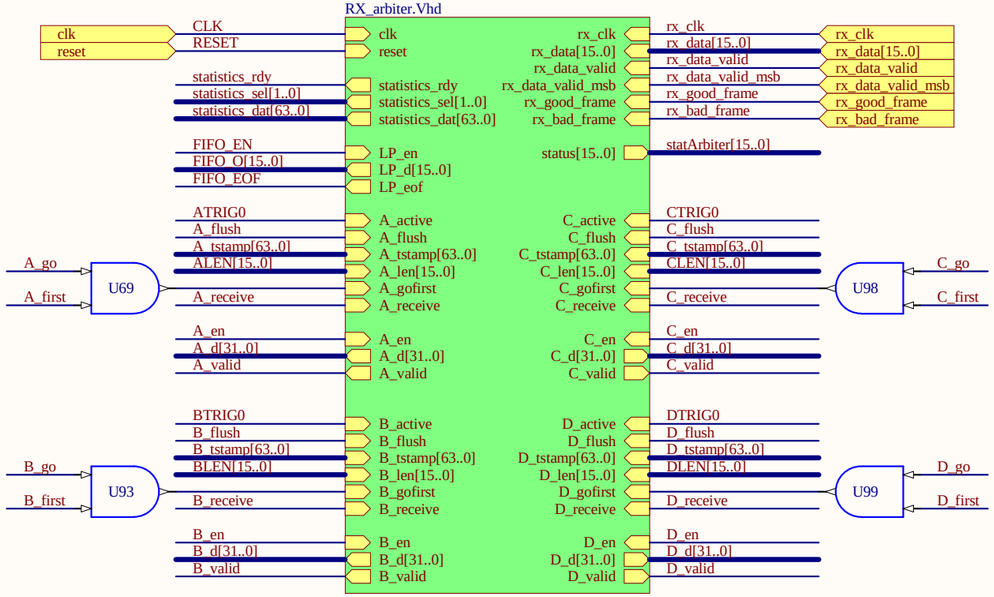
U_rx_trig_C
RX_Trig.Vhd



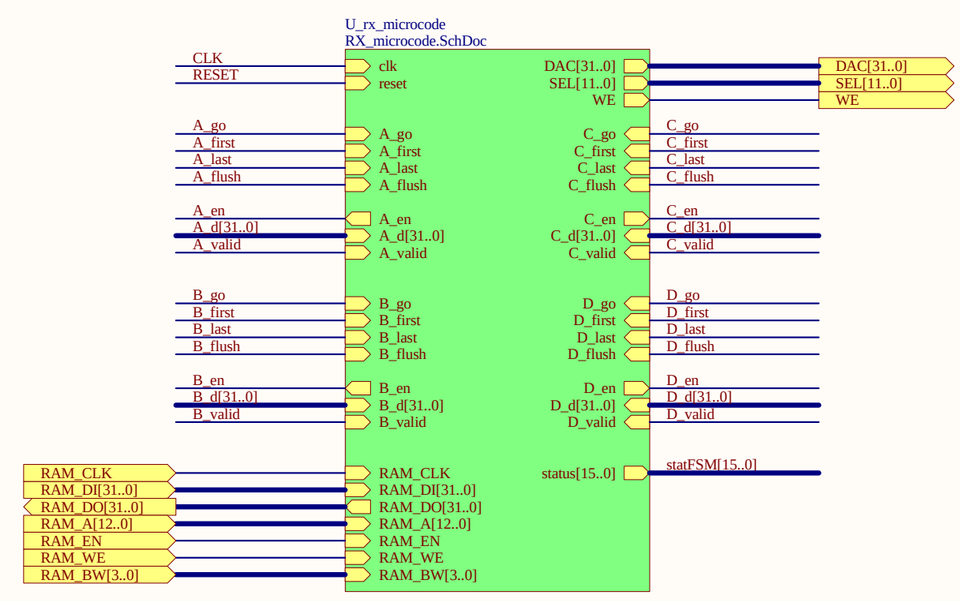
U_rx_trig_D
RX_Trig.Vhd



U_rx_arbiter
RX_arbiter.Vhd



U_rx_microcode
RX_microcode.SchDoc



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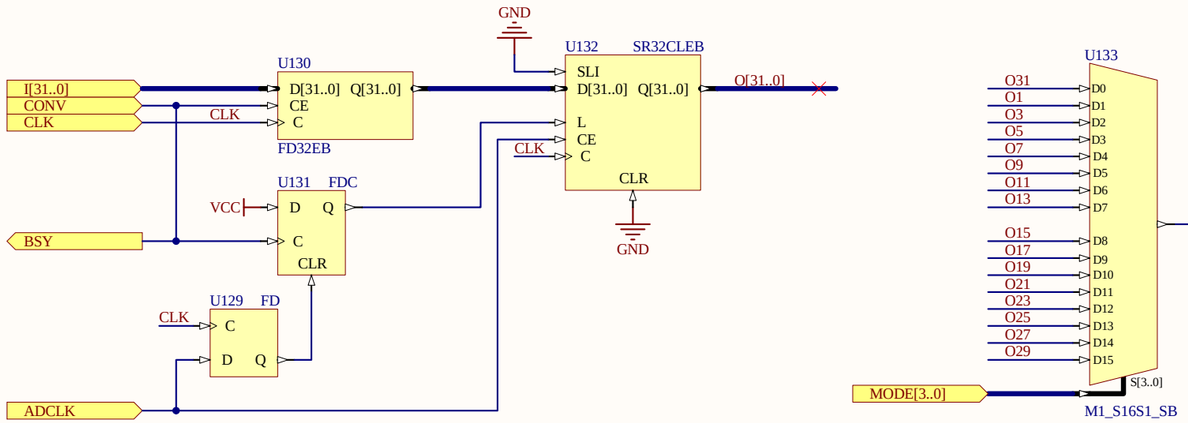
Date: 2/28/2008	Sheet of	
File: C:\User\..\RX_engine.SchDoc	Drawn By: Daniel Sigg	



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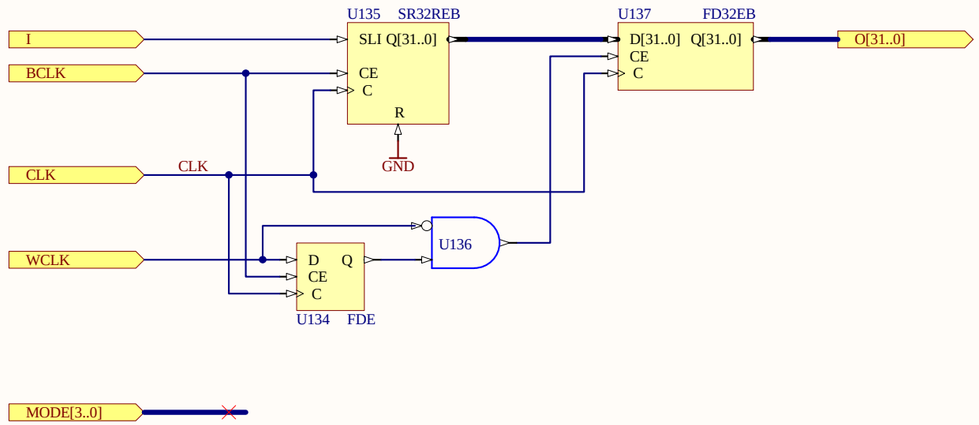

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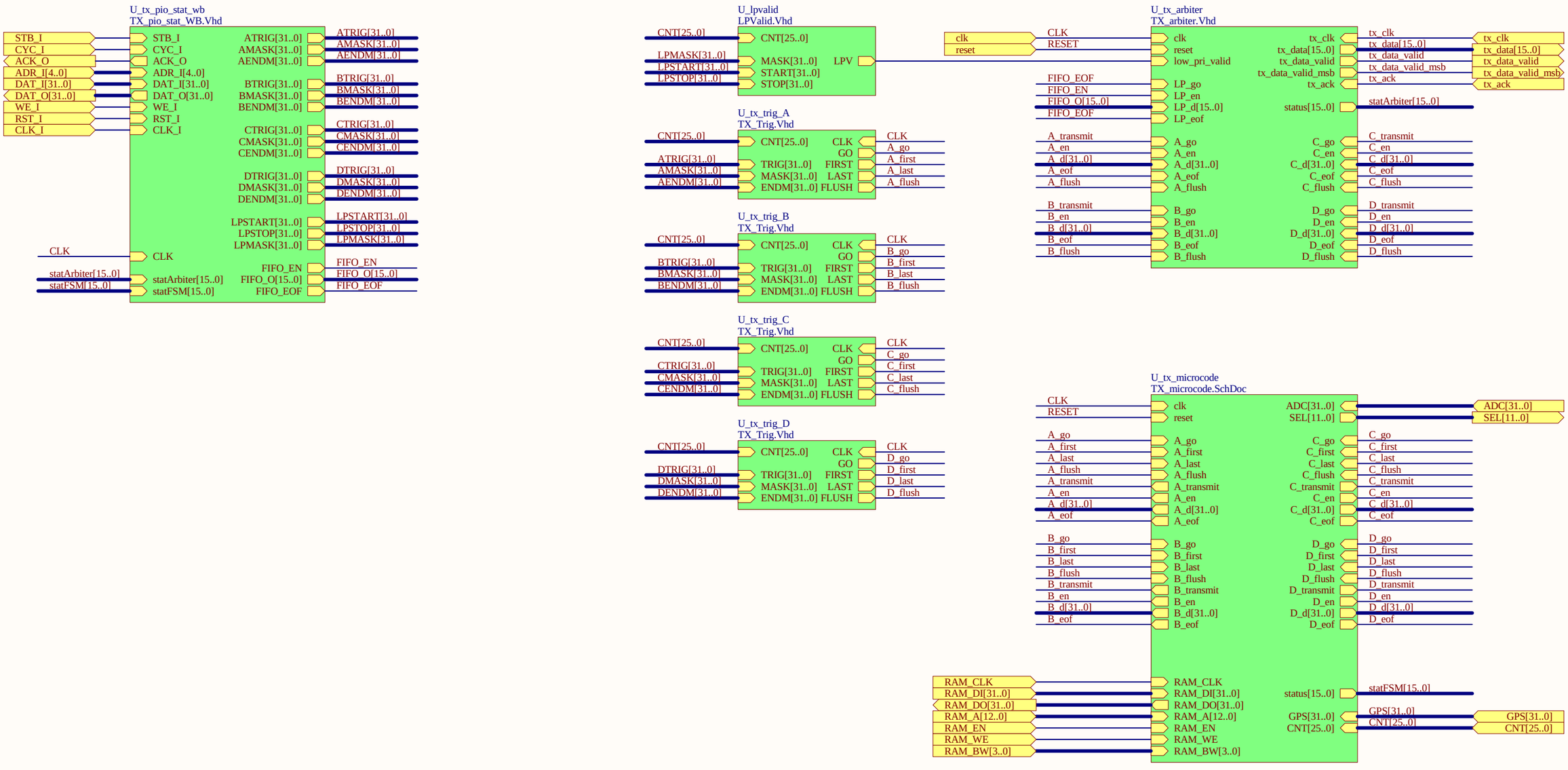

Title	**Stand Alone Uplink: FPGA Design**	
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Date: 2/28/2008	Sheet of	
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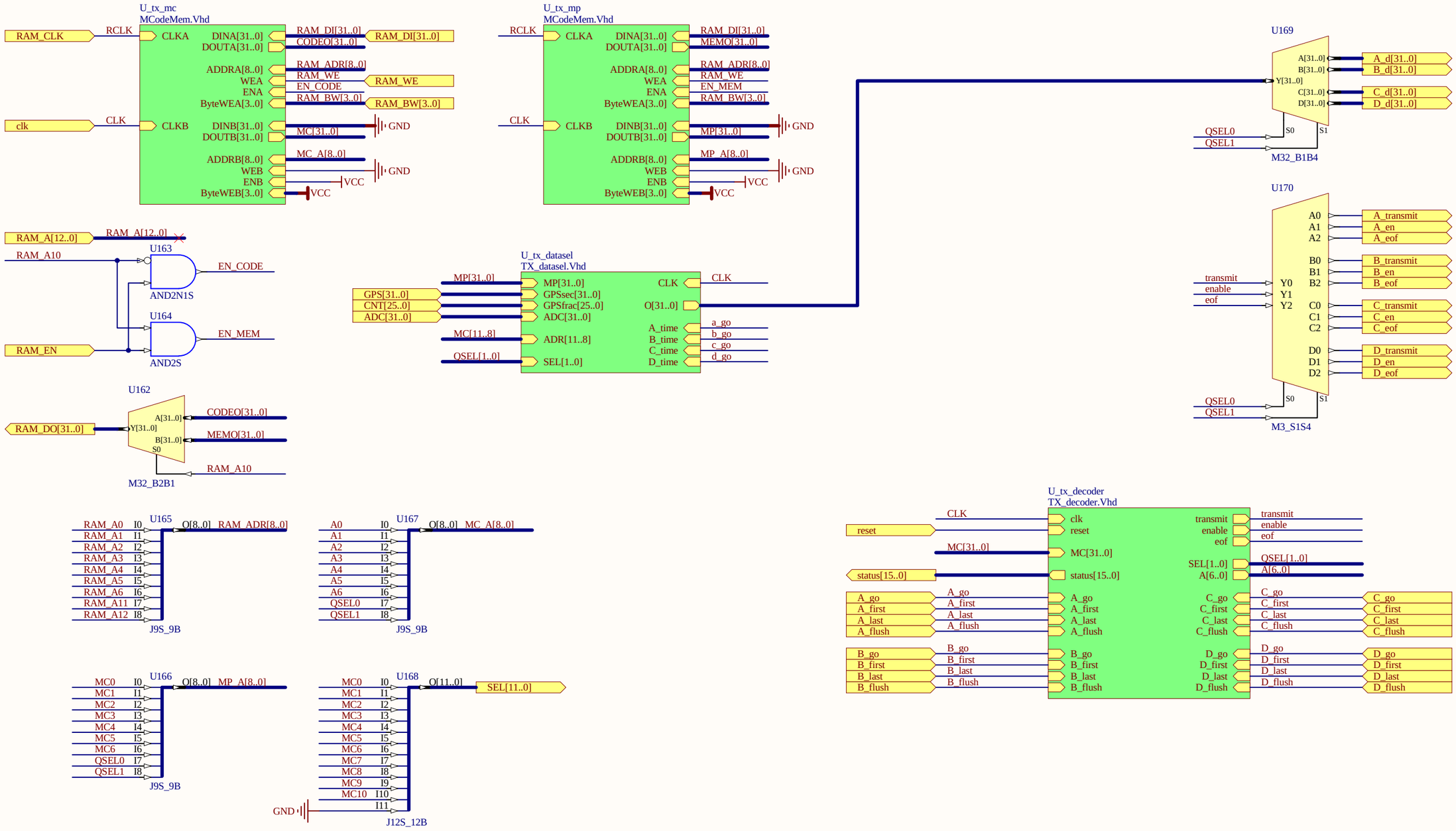

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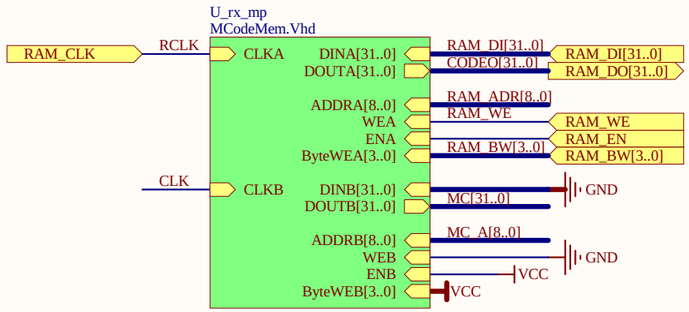

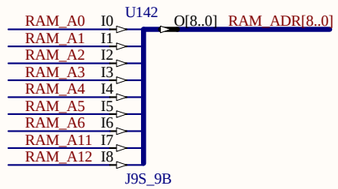

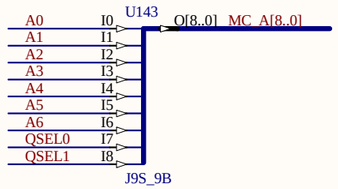

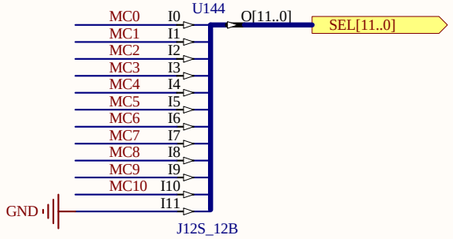

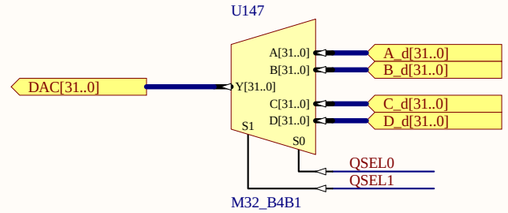

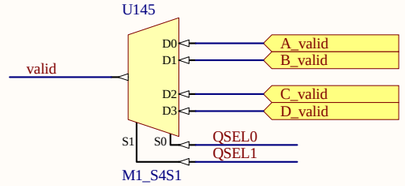

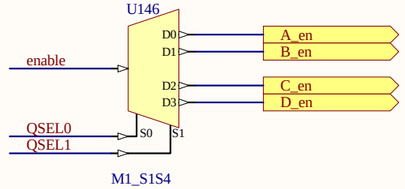

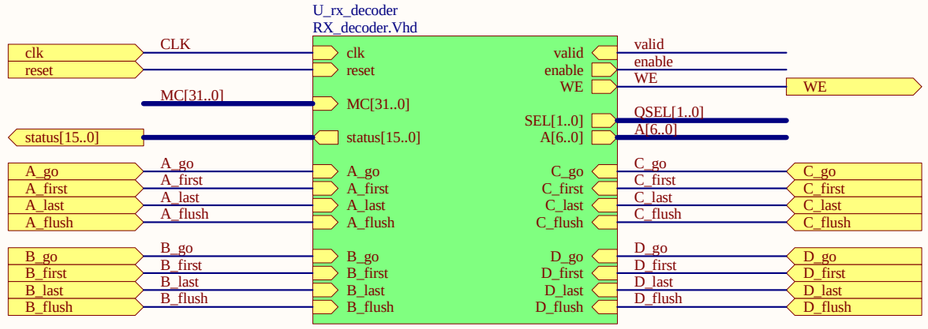

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