LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T1000523-v3 *LIGO* January 16, 2014

CDS I/O Chassis
PCIe Bus Layout

R. Bork

Distribution of this document:
LIGO Scientific Collaboration

This is an internal working note
of the LIGO Laboratory.

California Institute of Technology
LIGO Project – MS 18-34
1200 E. California Blvd.
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – NW22-295
185 Albany St
Cambridge, MA 02139
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

LIGO Hanford Observatory
P.O. Box 1970
Mail Stop S9-02
Richland WA 99352
Phone 509-372-8106
Fax 509-372-8137

LIGO Livingston Observatory
P.O. Box 940
Livingston, LA 70754
Phone 225-686-3100
Fax 225-686-7189

http://www.ligo.caltech.edu/

1 Introduction

The purpose of this document is to describe the PCIe expansion bus, built into every CDS I/O Chassis (IOC), in terms of how the slots are mapped by the computer BIOS.

2 Overview

Every CDS IOC contains a PCIe bus backplane with 17 PCIe slots. The PCIe slots in this backplane do not map to the computer in order from left to right, or right to left. Instead, the slots are mapped according to the most convenient routing of PCIe bridge chip connections to the nearest PCIe slots.

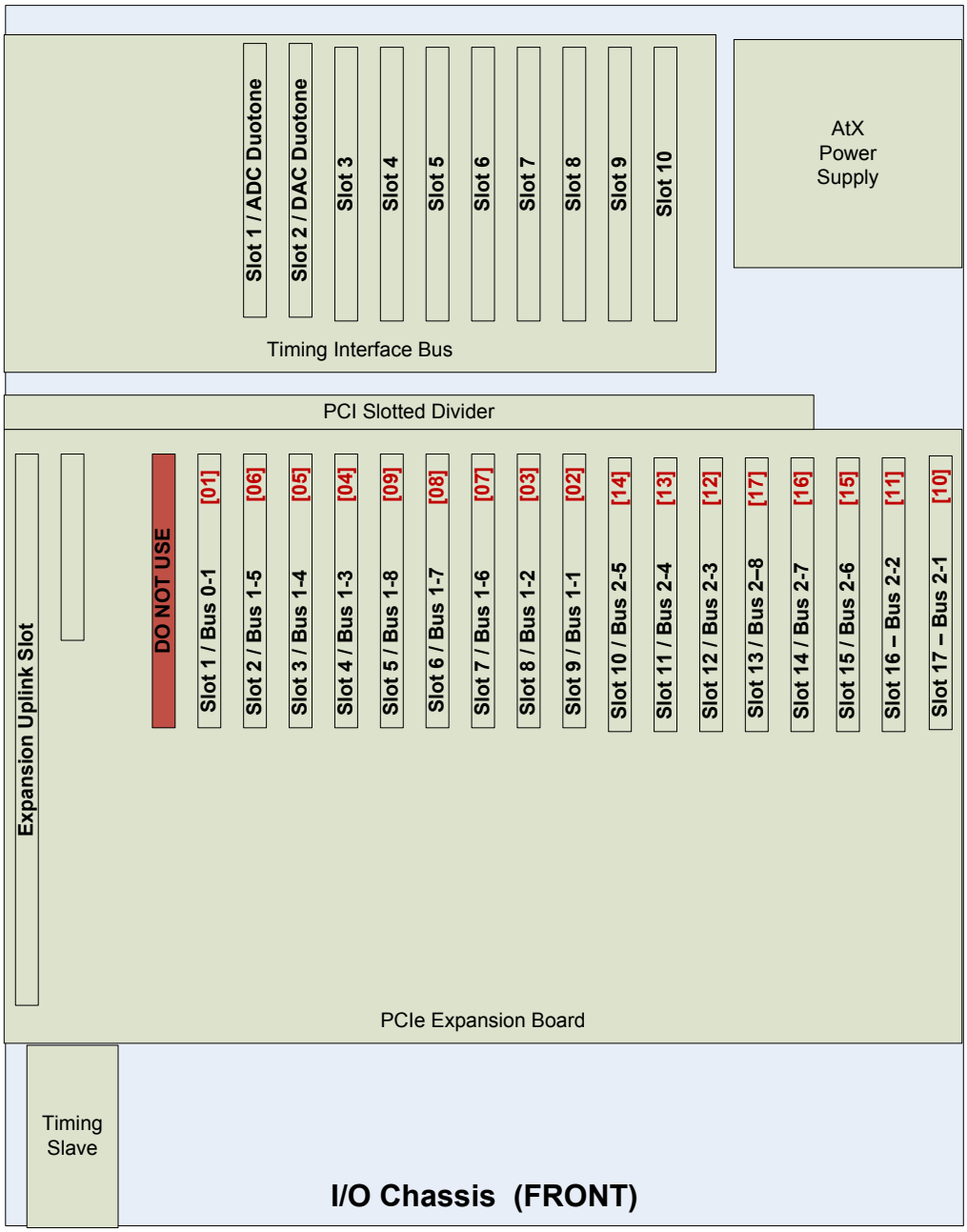
The issue with this mapping is with software developed using the CDS Real-time Code Generator (RCG). It associates PCIe card numbers, defined in the user model, to PCIe cards found in the bus in order. For example, if the user model has ADC card 0 defined, the RCG associates this with the first ADC found on the bus. However, when multiple cards are inserted in the IOC, it is not readily apparent which ADC is ADC 0, ADC 1, etc. Therefore, the following sections describe the mapping to help the user determine which cards will show up where in the software.

3 PCIe Slot to Bus Assignments

The following diagram shows a top view of an IOC, with the front of the IOC at the bottom of the figure. The IOC contains a 17 slot PCIe expansion bus and a 10 slot timing interface bus. For purposes of this document, card slots are numbered left to right, as viewed from the front of the chassis.

For each slot, the following information is provided in the figure:

1) PCIe major / minor bus numbers eg Bus 1/0. The PCIe expansion board contains 3 top level buses (listed here as 0,1,2), along with up to 8 minor addresses. Slot 1 is the only slot on bus 0 and therefore any card in this slot will be the first card mapped. Bus 1 and 2 each contain eight (8) sub address locations. The computer BIOS maps these in order detected ie Bus 0 first, then up to 8 devices on Bus 1 and finally up to 8 devices on Bus 2.
2) The number highlighted in red shows the mapping order of the PCIe slots. For example, a card in slot 1 will always be mapped first and a card in slot 13 will always show up last (17).



4 Recommended PCIe Card Installation

At some point, the RCG code may be modified to use detect bus numbers and automatically 'shuffle' its mapping of cards to match slots 1 to 17. In the meantime, the user should be aware of the mapping, as is, and install cards appropriately.

By proper routing of the PCIe card to timing bus interface card interconnect cable, it is possible to still have the timing interface bus slots mapped 1 to 10, left to right on the diagram, at the back panel of the IOC. If this is not done, then the IOC back panel should be appropriately labeled as to which slot goes to which PCIe module.

The best placement of PCIe cards into slots is dependent on the number and types of cards to be used, and therefore there is no one optimal configuration. However, a few general guidelines:

- Timing slave control binary output module (PCIe slot 16). Each IOC must contain one of these units, connected with a ribbon cable to the timing interface bus to control synchronous startup timing.
- Binary I/O (BIO) Cards. BIO cards should be inserted in Slot 1 thru n on the PCIe bus, where n is the number of BIO cards. This is to allow for the simplest routing of cables from the cards through vacant slots on the IOC back panel.
- ADC/DAC modules. For timing diagnostic purposes, the first ADC and first DAC input/output cables need to be routed to the timing interface cards in the timing backplane slots 1 (ADC) and 2 (DAC). The ADC must be placed into a PCIe backplane slot whereby no other ADC modules will show up first. Same for first DAC ie must show up before any other DAC modules.
- If the IOC is to contain a mix of 18bit and 16bit DAC modules, then all 18bit DAC modules must show up on the PCIe bus before any 16bit modules.
- Remaining ADC/DAC modules should be placed into the IOC PCIe backplane with consideration as to the amount of I/O cable crossing required to map the timing backplane from left to right, for ease of identification from the back of the unit once the lid is on the IOC.