LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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LIGO Laboratory / LIGO Scientific Collaboration

Technical Document	**LIGO-T1000477-v1**	11 August, 2010

IRIG-B Interface Module
Advanced LIGO Timing System

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IRIG-B Interface Module
Advanced LIGO Timing System

Contents

1 Introduction to the Timing IRIG-B Module

The Advanced LIGO Timing System distributes a highly accurate timing signal to the three LIGO interferometers. By synchronizing data collection to better than $1\mu s$ precision, the timing system (1) reduces timing jitter, (2) improves direction reconstruction, and (3) improves background rejection, all of which serve to improve LIGO's overall sensitivity. The timing system consists of a set of electronics modules which collectively distribute a GPS timing signal to LIGO subsystems. The central node of the timing system is a master clock which receives a timing signal via a GPS antenna. Any number of fan-out chassis can be synchronized to the master via a fiber optic cable. These fan-outs serve to propagate the timing signal throughout the timing system. Finally, slave modules synchronized to the fanout boxes are used to interface between the timing system and any given LIGO subsystem [1].

The IRIG-B box is one timing system slave module. It supplies the timing signal to frame-building servers in the Mass Storage Room (MSR) and the interferometer end stations (ETMX, ETMY). The IRIG-B box converts the internal timing system signal encoding to a DCLS IRIG-B signaling standard, which is easy to

[1] For a detailed introduction to the Advanced LIGO Timing System, consult *The Advanced LIGO timing system* by Imre Bartos, *et al.* in C.Q.G. (Ref. [1]). To build your very own Advanced LIGO Timing System, see *Advanced LIGO Optical Timing Distribution System Quick Start Guide* by Imre Bartos, *et al.*, LIGO-E080541-v3 (Ref. [2]). More information is available on the Advanced LIGO Timing Wiki, located at http://ilog.ligo-wa.caltech.edu:7285/advligo/Timing.

interface with commercial servers through use of commercially available PCIe modules. [2] (Note that the IRIG-B standard, while widely-used, is limited in the information it carries and is high in 100Hz harmonics, and so its usefulness in the Advanced LIGO Timing System is largely limited to synchronization of commercial data-processing computers, which are already installed in a noisy environment.) The IRIG-B box provides a user interface for selecting daylight savings time, setting the timezone, adding and subtracting UTC leap seconds, and reading out the current time in GPS, UTC, or local format. The IRIG-B box also provides an input port for an IRIG-B encoded signal, which can be used to verify a server's time stamp. Detailed description of IRIG-B functionality is given below.

2 Assembling & Programming the IRIG-B Module

The IRIG-B box consists of four main components: a timing slave (D070071-C), an IRIG-B timing Daughter Board (D0900305-A), two display units (MasterClock: TCD-200), and three IRIG-B rear PCBs (D0900304-A). The box is housed in a standard chassis, with front and rear panels (D0900302-B & D0900303-A, respectively). The timing slave's FPGA chip must be programmed with the IRIG-B FPGA program, which can be uploaded to the chip using Altium Designer with the Xilinx ISE [3]. Below are detailed assembly instructions. See Fig. 1 for visual assembly procedures.

2.1 Hardware Components

1. IRIG-B Module PCBs
   a. Timing Slave, D070071-C (1)
   b. IRIG-B Timing Daughter Board, D0900305-A (1)
   c. IRIG-B Rear PCBs, D0900304-A (3)
2. Box Enclosure
   a. LCD Display Units, MasterClock: TCD-200 (2)
   b. Standard 2U Chassis (1)
   c. IRIG-B Front Panel, D0900302-B (1)
   d. IRIG-B Rear Panel,D0900303-A (1)
   e. 3-pin Power Connector (1)
3. Internal Cabling
   a. BNC T-connector (1) & short BNC cables (2)
   b. LCD Display Power Cables (2)
   c. 40-pin Ribbon Cables (3)
4. External Hardware
   a. Advanced LIGO Timing System, consisting of at least one fully-functional MFO (1)
   b. Power Supply Unit (PSU), capable of 10W at +12V DC (1)
   c. (Optional) External LED Display, MasterClock: ALD118 [4] (1)
   d. Windows Desktop Workstation with Altium Designer & Xilinx ISE (1)
5. External Cabling

[2] Direct current level shift (DCLS) uses width-coded DC pulses to carry signal information (instead of, e.g., amplitude modulation of a sine wave carrier). The Inter-Range Instrumentation Group time code, version B, (IRIG-B) is defined at https://wsmrc2vger.wsmr.army.mil/rcc/manuals/200-04/TT-45.pdf.

[3] Documentation for Altium Designer can be found at http://wiki.altium.com/. Note that Altium Designer is the IDE used to develop FPGA code and draw PCB schematics. The Xilinx ISE is used transparently by Altium Designer to interface with the FPGA chips manufactured by Xilinx.

[4] Detailed documentation of the ALD118 can be found at http://www.masterclock.com/data_files/ald118-serspec.pdf.

a. Power Cable: PSU to 3-pin Power Connector (1)

b. (Optional) 6-pin RJ12 Jack Cable: IRIG-B Box to External LED Display (1)

c. Fiber Optic Cable (1) + Fiber Optic Cable Transceivers (2) [5].

d. JTAG-USB Adapter (1)

2.2 Front Panel Assembly

1. Slave/Daughter Assembly. The IRIG-B Daughter Board attaches to the timing slave via two 80-pin surface mount connectors. The boards are secured together with four sets of standoffs, as shown in the Fig. 1. An additional support plate (one always seems to be included with the timing slave) can be mounted below the slave to prevent electrical contact between the timing slave and the bottom of the chassis. The assembly can then be inserted into the front panel and secured with four additional mounting screws.

2. Display Assembly. Prior to installing the LCD Display boxes, the proper time & date display format must be specified using dip-switches inside the display boxes. Unscrew both front and rear display box covers to access these switches. After setting the switches, the displays can be mounted into the front panel using the front covers.

   Date Display. SW1-1 low, SW1-2 high (date display); SW2-11 high (European date format).

   Time Display. SW1-1 low, SW1-2 low (time display); SW2-10 low (24-hour time display).

   Both Displays. SW2-12 high (disable the Real Time Clock (RTC); this causes the display to show dashes unless a timing signal is actively being received). [6]

3. Panel Assembly. Screw the panel onto the chassis.

2.3 Rear Panel Assembly

1. Rear PCB (A). Solder a power supply connector onto one of the IRIG-B Rear PCBs, then insert it into slot (A) on the rear panel.

2. Rear PCBs (B) & (C). Insert the two other Rear PCBs into the (B) and (C) slots on the rear panel. Secure each BNC connector with washer and bolt, and secure each PCB with two mounting screws. Secure the boards to each other with four pairs of 0.875" standoffs.

3. Panel Assembly. Screw the panel onto the chassis.

2.4 Cable Connections

1. Display/Daughter Connection. Using a T-connector and two short BNC cables, connect the BNC output on the daughter board to the BNC inputs on the display units.

2. Display Power. The LCD Displays are powered from cables cut off from cheaply available wall-plug power supplies. To make the kludge cables, cut off the AC/DC converter box, strip the wires, and insert the cable into the two screw terminals on the lower Rear PCB (A). Plug the other end into the display boxes.

3. Rear PCB/Daughter Connection. Use three 40-pin cables, matching up the ground pin on both ends of each connector as shown in Fig. 1.

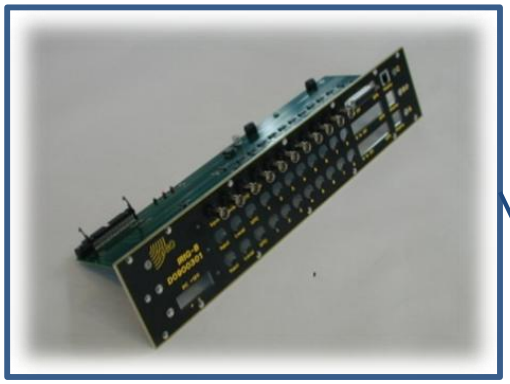
2.5 Power-up & Programming

1. Power Supply. The IRIG-B module requires +12V DC supply and draws about 10W. Give it power.

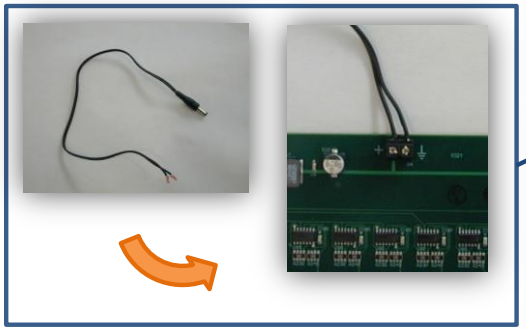
[5] For exact specifications & model numbers of fiber optic cables and transceivers supported by the Timing System, see Appendix A of LIGO-E080541-v3 (Ref. [2]).

[6] For detailed documentation of the TCD-200, go here: http://www.masterclock.com/data_files/tcd200_um.pdf.

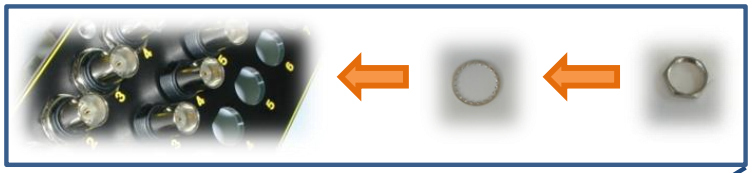
Figure 1. IRIG-B Module Assembly Guide



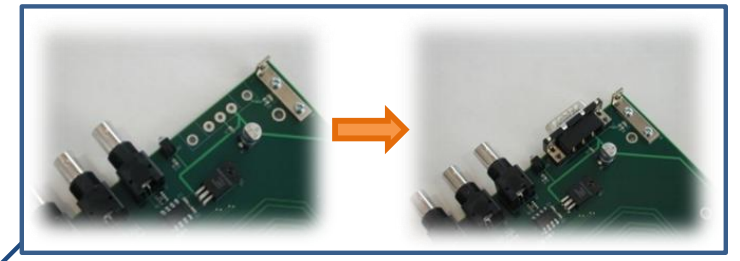
(2.2.2) The Rear IRIG-B PCBs mount into the rear panel as shown. The boards are supported by four pairs of 7/8” standoffs mounted between the PCBs.



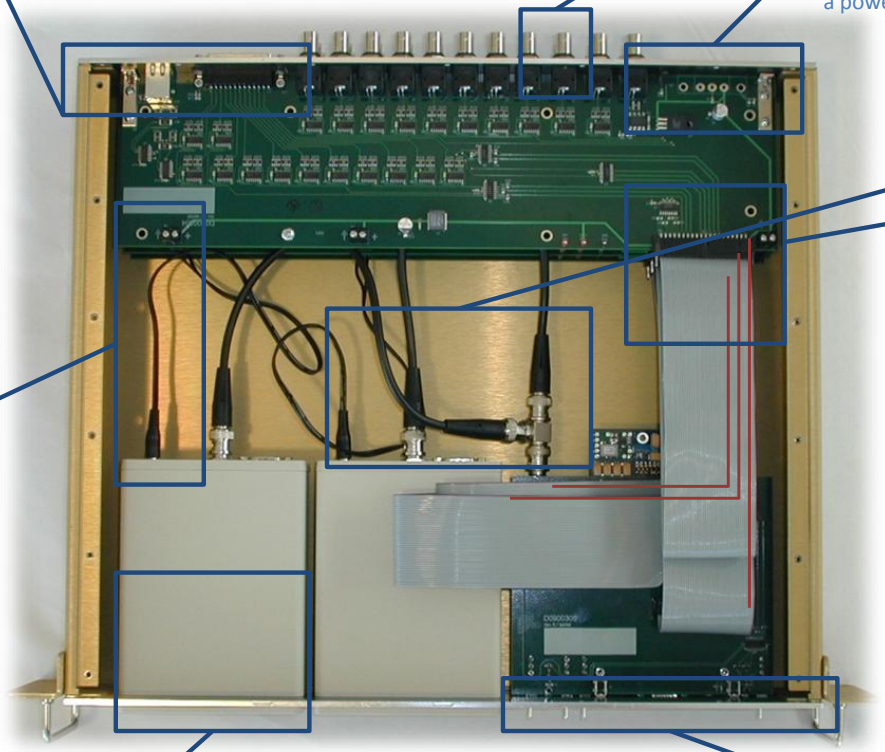
(2.3.2) The LCD Displays are powered from makeshift cables cut off from wall-plug power supplies. To make these cables, strip the ends of the power cord and mount it to the screw terminals on Rear IRIG-B PCB A.



(2.2.3) A washer and locknut secure each BNC port on the Rear IRIG-B PCBs. Two screws also hold each board in place, and standoffs ensure the boards remain well-separated.

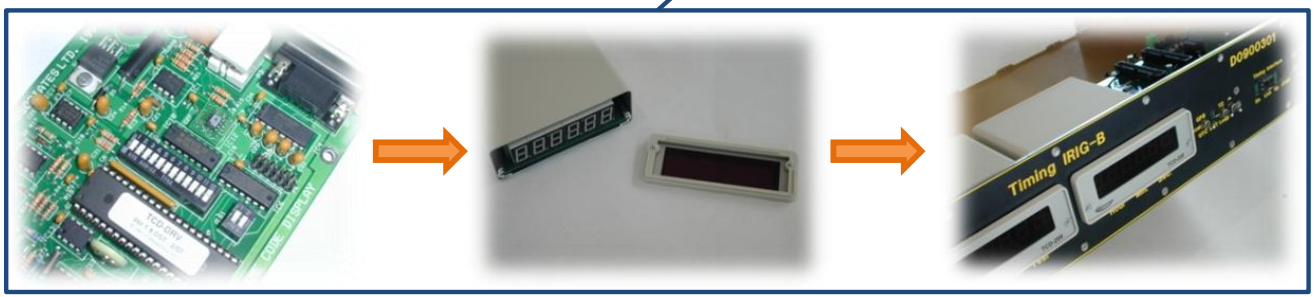


(2.2.1) The Rear IRIG-B PCB A supplies power to the IRIG-B module through a power supply connector, which must be sautered to the PCB.

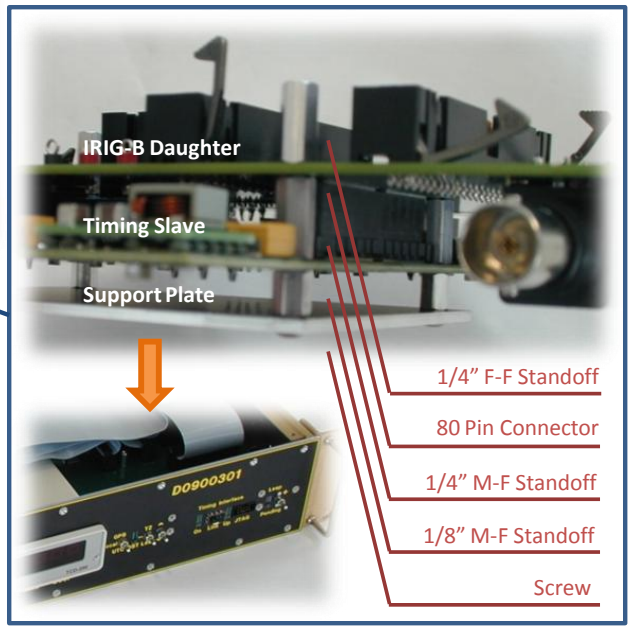


(2.3.1) Two short BNC cables and a T-connector send an IRIG-B signal from the IRIG-B Daughter to the LCD Displays.

(2.3.3) Three 40 pin ribbon cables interface between the Rear IRIG-B PCBs and the IRIG-B Daughter. The ground wire on each cable is attached as shown by the red lines at left.



(2.1.2) The two LCD Displays must first be set to display either time or date. These settings can be adjusted via dipswitches inside the Display box. Unscrew both front and rear Display box covers to access these switches. Date display: set SW1 -1 low and SW1-2 high for date display; set SW2-11 high for European display format. Time display: set SW1-1 low and SW1-2 low for time display; set SW2-10 low for 24-hour time display. For both Displays set SW2-12 high to disable RTC (this causes the Display to show dashes unless a timing signal is being actively received). The Displays mount into the front panel using the front covers, as shown.



(2.1.1) The IRIG-B Daughter connects to the Timing Slave through two 80 pin connectors and is secured with a standoff assembly, as shown above. A support plate helps hold the assembly up when it is mounted into the front panel.

2. JTAG Programming. Use a JTAG-USB adapter to connect the IRIG-B box to a desktop workstation with a fresh copy of Altium Designer installed. Load the IRIG-B program into the FPGA chip. Watch the lights come on.

3. Fiber Optic Up-link to the MFO. Insert a fiber optic transceiver into the IRIG-B Module and the upstream Timing Master Fanout (MFO). Connect the two boxes with a fiber optic cable. The timing slave will automatically synchronize to the upstream MFO [7].

3 Testing the IRIG-B Module

Here we describe procedures for testing the Timing IRIG-B Module. For most of these tests, we use Digital I/O devices pre-programmed into the IRIG-B FPGA code. These enable easy testing of the IRIG-B box. Failed tests most likely indicate failed hardware. Fried components can often be found using an oscilloscope and/or cleverness with the VHDL code. Of course, software glitches are always possible. For more details on hardware functionality, see the User's Guide.

3.1 Hardware Tests: Power Up & Programming

1. Power-up Lights. Upon power-up, do the 3 rear panel LEDs shine blue?

   Rear PCB A: Rear PCB B: Rear PCB C:

2. Test Points.

   IRIG-B Daughter PCB:

   TP2. Nominal: 3.3 ± 0.5V Measured:

   TP3. Nominal: 2.5 ± 0.5V Measured:

   IRIG-B Rear PCB:

   TP1. Nominal: 5.0 ± 0.5V Measured:

   TP2. Nominal: 12 ± 0.5V Measured:

   Multimeter

   Model Number:

   Manufacturer:

3. FPGA Programming. Connect the JTAG-USB adapter from the IRIG-B Module to the desktop workstation & load the IRIG-B FPGA program into the chip via Altium Designer.

   Was the FPGA chip programmed successfully?

4. Synchronization. Connect the IRIG-B Module to the MFO via fiber optic cable.

[7] For detailed information on synchronization & MFO setup, consult LIGO-E080541-v3 (Ref. [2]).

Does the Timing Slave "On" LED shine steady green?

Does the Timing Slave "Up-link" LED exhibit a 1/2 Hz blink (indicating synchronization with the MFO) within 3 minutes?

3.2 IRIG-B Front Panel Switches & Built-in LCD Display

The front panel switches and LCD Displays enable the user to chose a display time, set a time zone offset, add UTC leap seconds, and program in pending leap seconds. We test this functionality using the FRONT_PANEL_MON Digital I/O.

Digital I/O Reference: Front_Panel_Mon

Inputs

TZ_MON: The time zone offset, shown in minutes as a decimal number.
TZ_MON_SIGN: The sign of the time zone offset (1 represents a negative offset).
LEAP_MON: The number of UTC leap seconds, shown in seconds.
REAL_GPS: The true GPS time, in seconds.
INPUT_GPS: The time actually being used by the IRIG-B Module, whether real or user-injected.

Outputs

INJECT_GPS: Tells the IRIG-B Module to use actual GPS time (low) or a fake GPS time (high).
FAKE_GPS: A user-defined GPS time, in seconds.
RST_GPS: Injects the user-defined time (high) or lets the clock tick (low).
DELAY_OUT_ONLY: Injects the delayed time only into the hijacked IRIG-B output (see 3.4).

Test Procedure

1. IRIG-B Displays. Ensure that the IRIG-B box has been programmed and linked to the MFO via a fiber optic cable. The LCD Displays should then show a time; dashes indicate that a timing IRIG-B signal is not being properly received.

   Do the LCD Displays show a time?

   Disconnect the fiber optic. Do the LCD Displays show dashes?

2. Time Zone Offset. To adjust the time zone, hold the TZ/Leap Switch down and push up or down on the adjacent Add/Subtract Switch. Read out the time zone in the TZ_MON register on the Digital I/O.

   With the Time Zone Switch held, push the Add/Subtract Switch up, say, three times. Does the TZ_MON register show +3?

   With the Time Zone Switch held, push the Add/Subtract Switch down, say, seven times. Does the TZ_MON register show −4?

3. UTC Leap Seconds. To adjust the number of leap seconds, hold the TZ/Leap Switch down and push up or down on the adjacent Add/Subtract Switch. Read out the number of leap seconds in the LEAP_MON register on the Digital I/O.

   With the Leap Second Switch held, push the Add/Subtract Switch up, say, thirteen times. Does the LEAP_MON register show 13?

   With the Leap Second Switch held, push the Add/Subtract Switch down, say, five times. Does the LEAP_MON register show 8?

4. GPS/UTC/Local Switch. To toggle between different time displays, flip the GPS/UTC/Local Switch.

   Add some leap seconds. When the switch is flipped to UTC, does the displayed time lag the GPS time by the number of leap seconds shown in LEAP_MON?

   Add some time zone offset. When the switch is flipped to local, does the displayed time lag/lead the UTC time by the number of hours shown in TZ_MON?

5. Pending Leap Second LED. The Pending Leap Second switch allows users to program in leap seconds as they are announced.

   Press up on the Pending Leap Second Switch. Does the LED shine green?

   Press down on the Pending Leap Second Switch. Does the LED turn off?

   Press down again. Does the LED shine red?

6. Daylight Savings Time (DST). This switch toggles DST on the local time output.

   Push up on the Add/Subtract Switch. Does the DST LED turn on?

   Has the local time increased by one hour?

   Push down on the Add/Subtract Switch. Does the DST LED turn off?

   Has the local time decreased by one hour?

7. Pending Leap Second. Pending leap seconds are only added at specific times of year, as predefined in the international UTC standard. After a leap second is announced by the International Earth Rotation & Reference Systems Service, it is added at midnight of the last day of should only be added at specific UTC times. Input the following settings:

   - Add a positive pending leap second (Leap LED shines green) or a negative pending leap second (Leap LED shines red).
   - Set INJECT_GPS to '1', to set the system to use fake user-injected GPS time.
   - Set FAKE_GPS time to 10 seconds before each one of the GPS times in the table below.
   - Set RES_GPS to '1' to inject the new time and then back to '0' to the let clock tick.

   Record the results in the table below:

Leap	Date GPS Seconds	Clock shows 12:59:60? Clock skips 12:59:59?	LEAP_MON Register Value
+1	31 March, 2008 890956814		
	30 June, 2011 993427215		
	30 September, 2015 1127606415		
	31 December, 2016 1135555215		
−1	31 March, 2008 890956814		
	30 June, 2011 993427215		
	30 September, 2015 1127606415		
	31 December, 2016 1135555215		

3.3 IRIG-B Rear Panel BNC & DB-25 Connectors

The IRIG-B Module has 66 rear-panel IRIG-B signal outputs: 60 GPS time outputs, 3 UTC time outputs, and 3 local time outputs. We test these outputs by rerouting each of the rear panel outputs into the LCD Displays that are built into the IRIG-B box. This provides a quick and simple way to test the IRIG-B output signals without the need for excess hardware. To test the BNC output ports in this way requires a BNC cable; to test the DB-25 connectors requires a DB-25 breakout board and an electrical probe with BNC output.

Test Procedure

1. Program Timezone & Leap Seconds. Enter in an arbitrary time zone offset and an arbitrary number of leap seconds. Note the time zone offset & number of leap seconds in the FRONT_PANEL_MON Digital I/O.

2. Reroute LCD Displays. Unplug the IRIG-B LCD Display boxes from the daughter board output. Reconnect the boxes to each BNC output, one in turn.

3. BNC GPS/UTC/Local Time Outputs. Open up the REF_TIME Digital I/O. For each BNC output, compare the time shown on the LCD Displays with the corresponding time shown in the REF_TIME Digital I/O. Do the times match?

4. GPS DB-25 Outputs. Plug in the breakout board and use the BNC probe to connect the IRIG-B Display to each pair of output pins (see Fig. 2b for DB-25 pin-out). Check the display time against the GPS time displayed in REF_TIME. Do the times match?

Does it work?

	GPS1	GPS2	GPS3	GPS4	GPS5	GPS6	GPS7	GPS8	GPS9	GPS10	GPS11
A											
B											
C											

	GPS12	GPS13	GPS14	GPS15	GPS16	GPS17	GPS18	GPS19	GPS20	UTC	Local
A											
B											
C											

3.4 IRIG-B Input

The IRIG-B Module can receive up to three IRIG-B time signal inputs. The IRIG-B box outputs the time difference between the input time signal and the master timing signal, calculating the difference in the time & date information stored in the signals and in the arrival time of the IRIG-B pulses themselves.

Digital I/O Reference: Delayed_Input_Test

Inputs

TIME_DIFF: The difference between the internal GPS time & the delayed input IRIG-B time.
(Note: this is the difference in the times encoded by the IRIG-B signal.)
TIME_DELAY: The additional time difference in clock cycles between the IRIG-B second pulses.
(Note: this is the difference in the arrival time of the IRIG-B signals themselves.)

Outputs

HIJACK_OUT: When high, the IRIG-B Module outputs a user-adjusted IRIG-B time stamp.
TIME_DELAY: Input time delay, in clock cycles.
BASELINE_TIME_DELAY: Measured delay, in clock cycles, when TIME_DELAY is set to 0.

Test Procedure

1. Input Port. Using a BNC cable, connect a rear panel output port to any of the input ports.
2. Hijack BNC Output. Set HIJACK_OUT to '1'.
3. Baseline Time Delay. Note the time delay with 0 in the TIME_DELAY register.

   Baseline Time Delay. Nominal: 128 clock cycles. Measured:

4. Set Baseline Delay: Input the baseline time delay measurement into the BASELINE_TIME_DELAY register. This value will be automatically subtracted from the TIME_DELAY output register.

5. Add Arbitrary Time Delay. Set the time delay to an arbitrary large number of clock cycles (try on the order of 10E6). Record the output values. (Note: the timing clock has frequency 2^{26}Hz.)

   What was the input time delay (in clock cycles)?

   What was the measured time delay (in seconds + some remainder number of clock cycles)?

   Convert time delay back into clock cycles. How many clock cycles?

   Do the two clock cycle values agree?

6. Enable Negative Time Delay. To test an input time which leads the Timing System time, set the DELAY_OUT_ONLY to '1' in the FRONT_PANEL_MON Digital I/O.

7. Set Negative Time Delay. The user-defined GPS clock now controls the hijacked IRIG-B output. Input a past GPS time into the FAKE_GPS register. Reset the fake clock by switching RST_GPS high and then switching it back to low. Record the output values.

   What was the input time delay (in clock cycles)?

   What was the measured time delay (in seconds + some remainder number of clock cycles)?

   Convert time delay back into clock cycles. How many clock cycles?

   Do the two clock cycle values agree?

3.5 External Display

The IRIG-B box supports display output through an RJ12 6-pin jack carrying an RS422/RS485 serial signal to an external LED display (MasterClock: ALD118). This display shows GPS time in seconds, the current time zone, the number of UTC leap seconds, or input IRIG-B timing signal information.

External Display Test Procedure

1. Display Setup. Give the display power & interface it to the IRIG-B Module with the 6-pin RJ12 jack cable.
2. GPS Time. Shortly after powering up, does the display begin to show GPS time in seconds?
3. Time Zone. Push up the TZ/Leap Switch. Does the external display indicate the current time zone?
4. Leap Seconds. Push down the TZ/Leap Switch. Does the external display indicate the number of UTC leap seconds?

Does it work?

	GPS Time	Time Zone	Leap Seconds
A			
B			
C			

Figure 2a. IRIG-B Module Front Panel

LCD Time/Date Displays

(4.2.4) The two built-in LCD displays output the current time. The displays can output GPS, UTC, or local time, depending on the position of the selector switch to the right of the displays. Dashes indicate the display is not actively receiving a timing signal from the upstream MFO.

GPS/UTC/Local Switch

(4.2.4) Determines whether GPS, UTC, or local time will be output by the LCD displays.

Timing Slave Interface

(4.1.2) A fiberoptic cable connected via the Uplink port synchronizes the IRIG-B Module to the upstream MFO. The JTAG port allows the FPGA chip to be programmed. See references for complete timing slave documentation.

Pending Leap LED

(4.2.5) Green when a positive leap second is pending; red when a negative leap second is pending; otherwise off.

Pending Leap Switch

(4.2.5) Push up to add a pending leap second; down to subtract a leap second.

Daylight Savings Time (DST) LED

(4.2.3) On when DST is enabled; otherwise off.

Time Zone (TZ) / Leap Switch

(4.2.1-3) When the TZ/Leap Switch is pushed up, the Add/Subtract Switch adjusts the time zone; when pushed down, it adjusts the number of UTC leap seconds; when left alone, the Add/Subtract Switch toggles DST time.

Add/Subtract Switch

(4.2.1-3) Adjusts TZ, Leap, or DST depending on whether the TZ/Leap Switch is pushed up, down, or left alone.

Figure 2b. IRIG-B Module Rear Panel

IRIG-B Input

(4.3.5) The three BNC input channels require an IRIG-B encoded signal. When an input signal is received, the IRIG-B Module outputs the time difference between the IRIG-B signal & and the Timing System time.

IRIG-B Local Time

(4.3.1) Three BNC ports output the local time in the IRIG-B encoding, with DST, TZ offset, and leap seconds as set via the front panel interface.

GPS Time

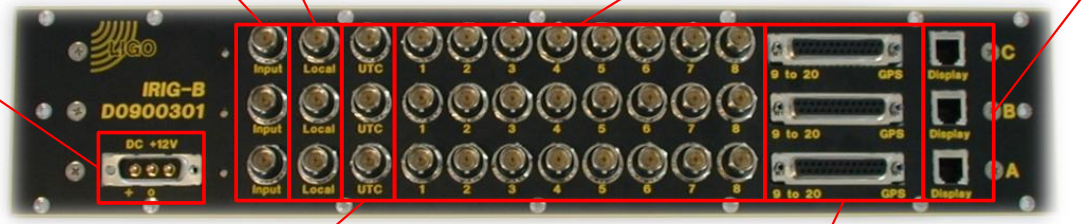
(4.3.3) Twenty-four BNC ports output the GPS time, received directly from the MFO.

LED Display

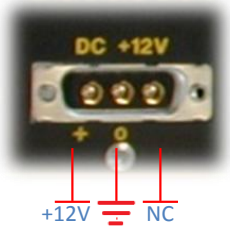
(4.1.4) An external LED display can be connected via 6-pin RJ12 connectors operating on the RS422 & RS485 signaling standards. The display shows (1) TZ offset when the TZ/Leap Switch is up, (2) UTC leap seconds when that switch is down, (3) the time difference between an input IRIG-B signal and the master clock, or otherwise (4) the current GPS time in seconds.

Power Supply

(4.1.1) The IRIG-B Module draws approximately 10W of power at +12V DC.



Power Connector Pin-out



UTC Time

(4.3.2) Three BNC ports output the UTC time in IRIG-B encoding, with leap seconds as set via the front panel interface.

More GPS Time

(4.3.4) Three DB-25 connectors output the GPS time, received directly from the MFO. The connector pin-out is as shown at right.

DB-25 Connector Pin-out

4 IRIG-B User's Guide

The IRIG-B box converts the internal Timing System signal into an IRIG-B encoded signal for use in synchronizing commercial computers. Here we describe start-up and configuration steps for the Timing IRIG-B Module.

4.1 Power Up & Synchronization

1. Power Up. The IRIG-B module requires +12V DC supply and draws about 10W. The rear panel has a 3-pin voltage connector (see Fig. 2b for pin-out). Give the box power.

2. Synchronize to MFO. Connect the IRIG-B to an upstream MFO with a fiber optic cable. After synchronization the Timing Interface "On" light will be always on and the "Up" light will exhibit a 1/2Hz blink.

3. Up-link to Desktop Computer. If the IRIG-B FPGA chip does not program itself (this will be apparent if the box, for instance, does not synchronize with the upstream MFO), then it will be necessary to reprogram the FPGA from a desktop workstation. To do this, connect the IRIG-B Module to a computer with a JTAG-USB adapter cable and program the chip through Altium Designer with Xilinx ISE.

4. (Optional) Connect External LED Display. Connect the external display (MasterClock: ALD118) to the IRIG-B box with a 6-pin RJ12 jack cable.

4.2 Initial Configuration

1. Setting UTC Leap Seconds. To input UTC leap seconds, hold down the TZ/Leap switch and add or subtract leap seconds with the Add/Subtract switch. When the TZ/Leap switch is held down, the external display will display the number of leap seconds programmed into the system.

2. Setting Local Time Zone. To set the local time zone, push up on the TZ/Leap switch and add or subtract 30-minute intervals to the time zone offset with the Add/Subtract switch. When the TZ/Leap switch is held down, the external display will display the current time zone.

3. Daylight Savings Time. To enable DST, push up on the Add/Subtract switch. To disable DST, push down on the Add/Subtract Switch. The DST LED will turn on when DST is enabled.

4. LCD Display Output. After synchronizing with the upstream MFO, the IRIG-B LCD displays will begin to display a time. The GPS/UTC/Local selector switch allows the user to choose between GPS, UTC, or local time display. Dashed lines on the LCD displays indicate that the IRIG-B Module is not actively receiving a timing signal from the upstream MFO.

5. Pending Leap Second. If a pending leap second is announced, the Pending Leap Switch can be used to program in a pending leap. This pending leap second that will then be added to the UTC clock at the end of the appropriate month. Push up on the Pending Leap Switch to add a positive pending leap second. Push down to add a negative pending leap second. If the Pending Leap LED is green, a positive leap second will be added; if red, a negative leap second will be added; if off, no leap seconds will be added.

4.3 Rear Panel I/O

1. Local Time BNC Output. The IRIG-B Module has 3 rear panel BNC outputs carrying IRIG-B encoded local time.

2. UTC Time BNC Output. The IRIG-B Module has 3 rear panel BNC outputs carrying IRIG-B encoded UTC time.

3. GPS Time BNC Output. The IRIG-B Module has 24 rear panel BNC outputs carrying IRIG-B encoded GPS time.

4. GPS Time DB-25 Output. In addition to the 24 GPS BNC output ports, the IRIG-B Module also has 3 rear panel DB-25 connectors, each of which carries 12 copies of the GPS IRIG-B signal (see Fig. 2b for pin-out). These can be used along with the GPS BNC ports to synchronize a total of 60 computers to the master timing clock with one IRIG-B box.

5. IRIG-B Input. The IRIG-B Module also has 3 rear panel BNC inputs, enabling the user to input an arbitrary IRIG-B signal. The IRIG-B box outputs the time difference between the input time signal and the master timing signal, calculating the difference in the time & date information stored in the signals and in the arrival time of the IRIG-B pulses themselves.

References

[1] The Advanced LIGO timing system. Bartos, Imre *et al.* Class. Quantum Grav. **27** (2010) 084025.

[2] Advanced LIGO Optical Timing Distribution System Quick Start Guide. Bartos, Imre *et al.* LIGO-E080541-v3 (2009).