LIGO LABORATORY
California Institute of Technology
1200 E. California Blvd.
Pasadena, CA 91125

Statement of Work
For Acquisition of 20 slot PCIe Expansion Backplanes for aLIGO

The following documents are incorporated into and made a part this purchase order. Click on the following LIGO Document Control Center (DCC) links to access these documents or go on line to the LIGO Public DCC at https://dcc.ligo.org/ to access the DCC#.

1.0 Terms:

DCC #	*Description*
C080185-v1	Laser Interferometer Gravitational Wave Observatory (LIGO) Commercial Items or Services Contract General Provisions California Institute of Technology "Institute", LIGO Rev 11/12/08
F0810001-v4	Technical Direction Memorandum.

2.0 End Item Data Package:

At the time of delivery of the parts, the Supplier shall also provide the following data, as a minimum:

- Any as-built modifications (with approval of the LIGO Contracting Officer) as mark-ups to the drawings
- Certificate or statement of compliance with all contract and drawing process restrictions.

3.0 Scope:

This RFQ is for the procurement of PICMG 1.3 compliant, 20-slot PCIe expansion backplanes per the minimum specifications listed below. Any specifications not met or exceeded by the product being proposed by the vendor shall be called out in the vendor response to this RFQ.

The backplanes shall meet the following minimum specifications:

- Support for 1 each System Host Board per the PICMG 1.3 specification
- The mounting hole pattern shall follow the PICMG 1.3 specification for 20 slot backplanes.
- The board size shall not exceed 12.9 inches x 16.4 inches.
- Support for a minimum of 18 x4 PCIe cards with x16 PCIe connectors. Each slot shall support a minimum of 75W of power as defined in revision 1.1 of the PCI Express Base Specification.
- Minimum of 1 each 24 pin ATX power connector for application of power.
- Additional terminal block connections for +12V, +5V and GND to be used by Caltech for external fan and indicator lamps. Minimum current to be supplied to each terminal block connection shall be 0.5A.
- Header connection for PS ON switch to be used by Caltech for connection of external power supply On/Off control.

4.0 Quantity Required:

PICMG 1.3 Compliant, 20-slot PCIe Expansion Backplane	total qty: 110

5.0 Delivery Requirements:

The deliveries are FOB at the destination listed below, i.e. the contractor has responsibility for shipping title and control of goods until they are delivered and the transportation has been completed. The contractor selects the carrier and is responsible for the risk of transportation and for filing claims for loss or damage.

Shipping Location:
These items will be shipped to:

California Institute Of Technology
Attention: Jay Heefner
1200 E. California, MS 18-34
Pasadena, CA 91125

Shipping Containers:
The contractor is responsible for providing shipping containers and transportation which protects these parts from damage from the transportation environment (weather, handling, accidents, etc.). Mating edges of parts should be especially protected from damage during shipping.

Delivery Schedule:

Delivery of first 10 units shall be 3 weeks or less, ARO.

Delivery of the remaining 100 units shall be completed within 8 weeks ARO.