aLIGO ISC Whitening Module Description
LIGO-T1000321-v5
R. Abbott
25 March 2014

1. **Overview** – A Whitening filter has been designed for general purpose signal whitening in the aLIGO ISC subsystem. The main goal of this filter is to ensure signals of interest are comfortably above the input referred noise of the General Standards 32 channel ADC chosen for aLIGO digitization. The required performance characteristics for this design are presented in Table 1. The design intended to fulfill these requirements is presented. All of the subcircuits are shamelessly taken from successful iLIGO designs to eliminate design uncertainty and time consuming prototypes. A goal of this write up is to establish this design as ready for production based on precedents set using similar circuits successfully deployed in LIGO.

2. **Requirements** – As shown in Table 1, the input referred noise requirements for the whitening filter are based on the output referred electronics noise of the preceding circuitry. This whitening filter is most commonly used to amplify signals from the aLIGO: RF demodulators, DC Quadrant position sensing amplifiers, and critical ISC DC photodiodes. The output dynamic range is designed to be compatible with the aLIGO Anti-aliasing function in conjunction with the standard aLIGO ADCs.

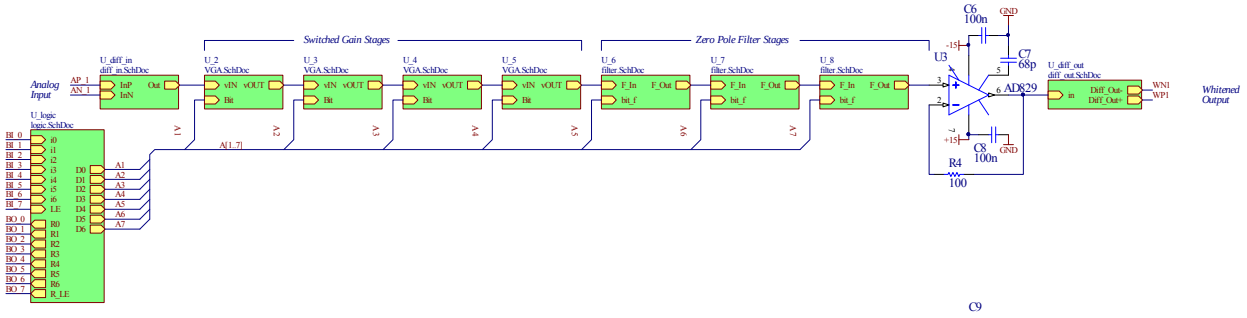
Table 1

Parameter	**Requirement**
Input structure	Analog differential receiver
DC power	+/- 18 VDC
Channels per PCB	4 channels
Input referred noise voltage	Less than 20nVrms/√Hz
Gain adjustability range	Greater than 40dB
Minimum gain step size	3dB
Total DC current per board	400mA per supply, required to control thermal problems in aLIGO racks
Output voltage dynamic range	+/- 20 volts p-p
Control interface	32 bit TTL parallel control with latch
Control readback	Every control bit is read back to control computer for integrity check
Analog filter function	3 stages of zero-pole filter, Fp/Fz ~10, each stage is independently switchable
Output structure	Balanced Differential Transmission
Input impedance	100kΩ
Slew rate	10 volts/μsec
-3dB Bandwidth	100 kHz
Mechanical	1U, 19 inch rack-mounted chassis

3. Circuit Solutions

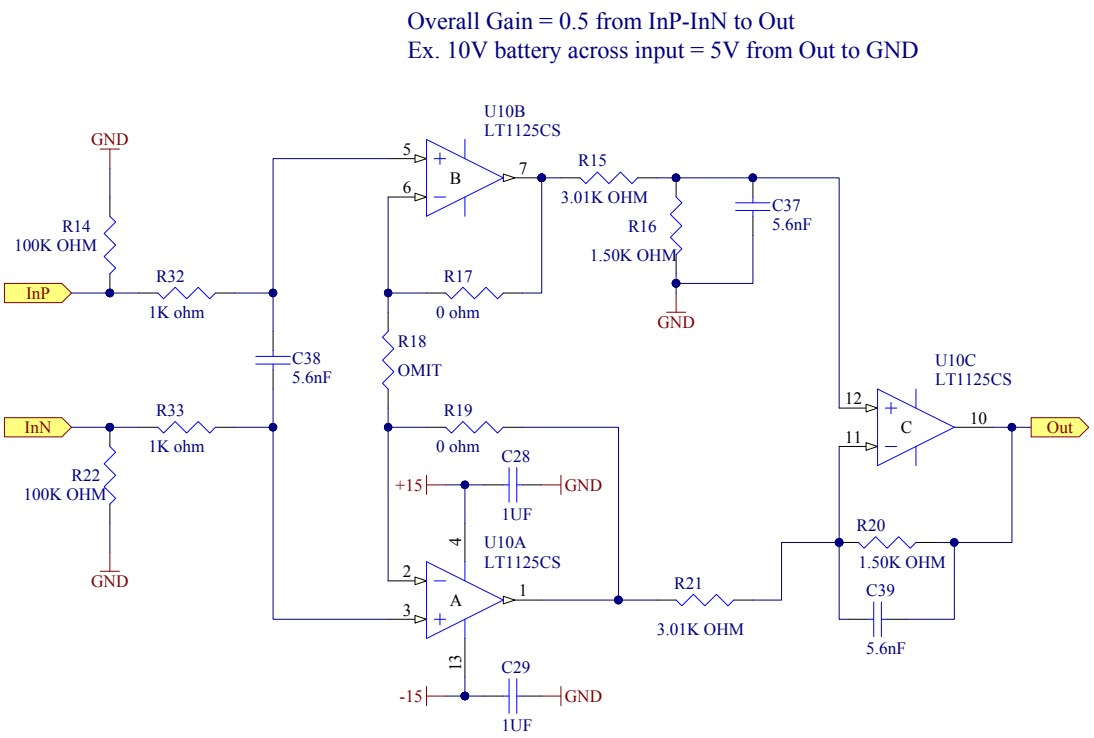
a. Block Diagram

Figure 1



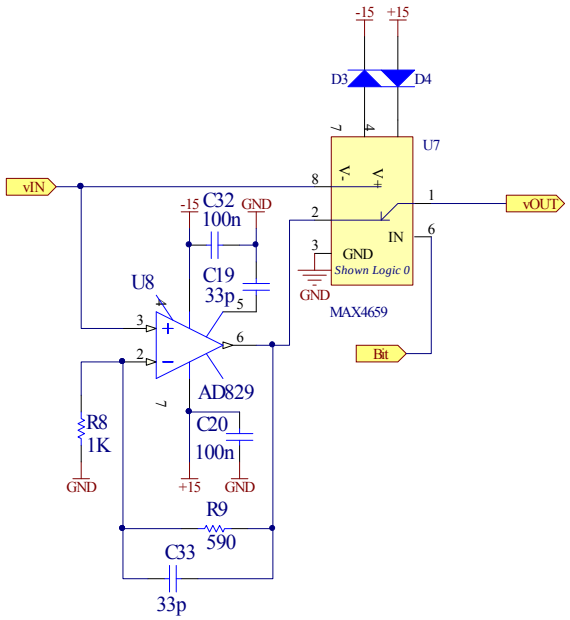
b. A fully differential, instrumentation amplifier front end is employed as shown in Figure 2.

Figure 2



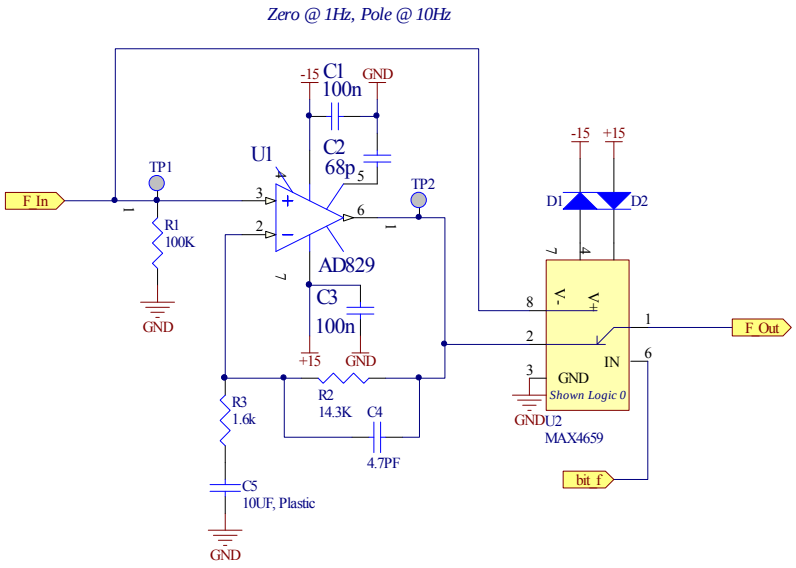
c. One of four switchable gain stages is shown in Figure 3(opamp is now OP27)

Figure 3, 4dB gain step circuit shown



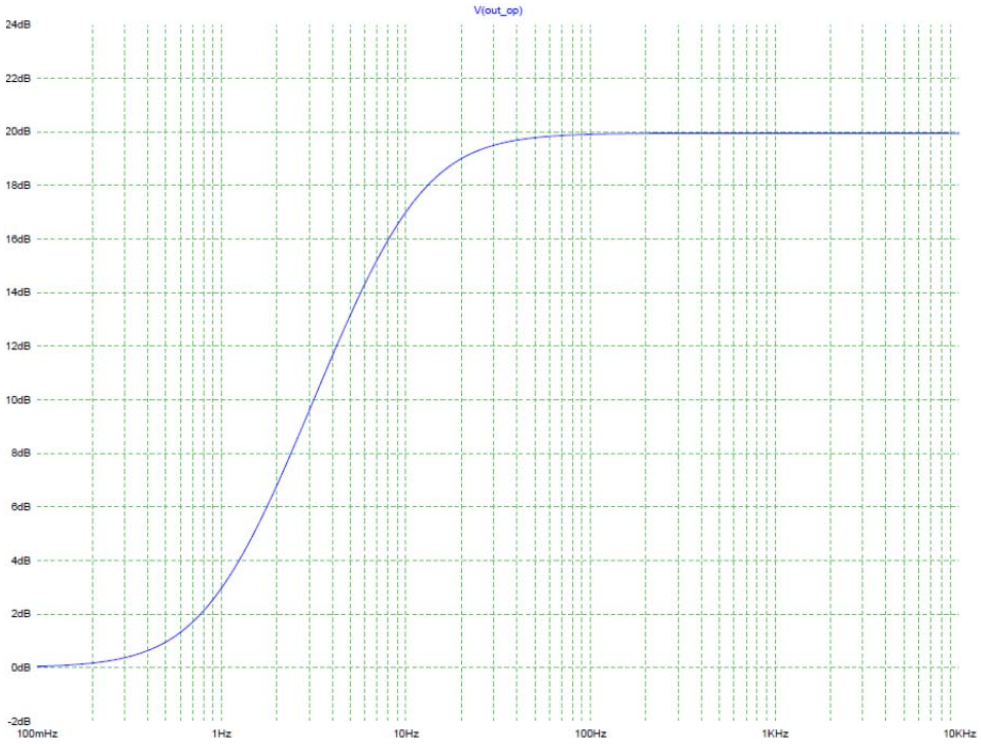
d. One of three switchable filter stages is shown in Figure 4 (opamp is now OP27)

Figure 4



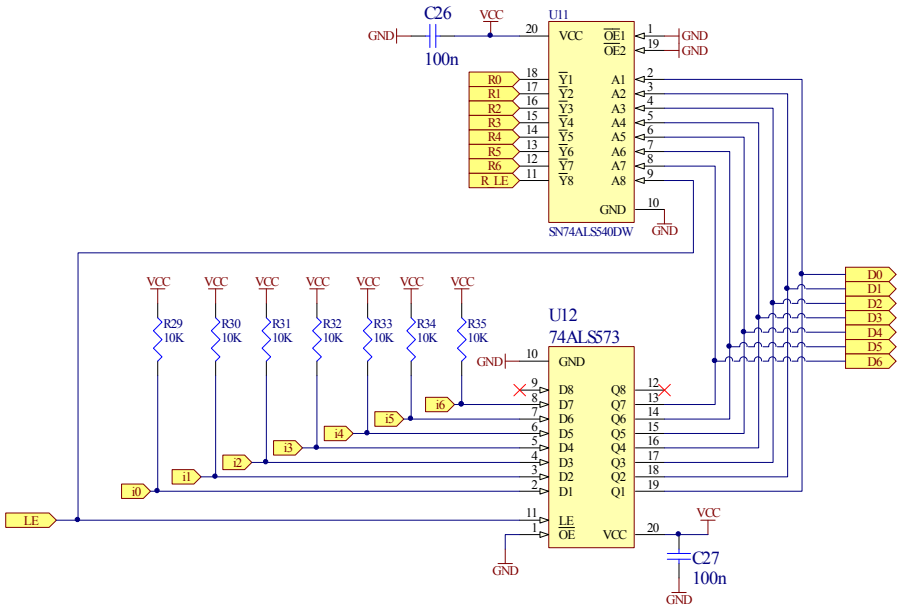
e. The transfer function of the filter stage is shown in Figure 5

Figure 5, impossible to read transfer function



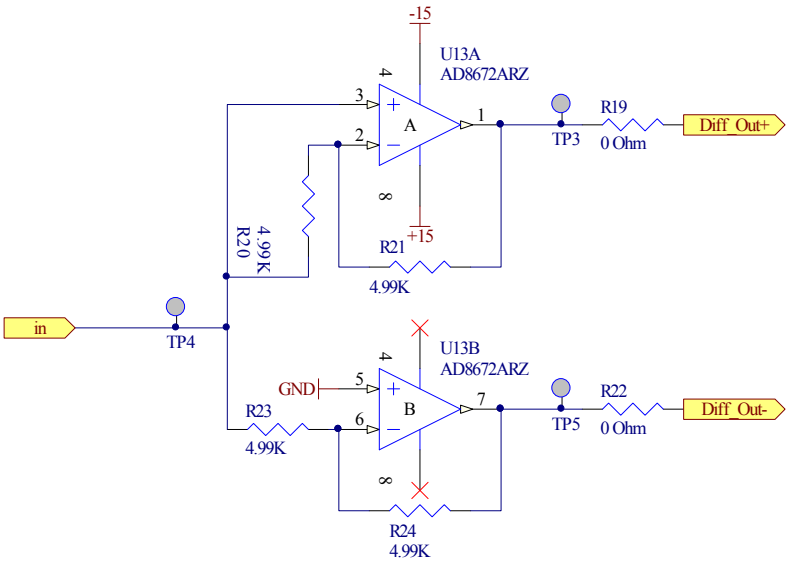
f. Gain and filter control logic is shown in Figure 6. The voltage level shown as VCC is 5VDC

Figure 6



g. The differential output drive circuit is shown in Figure 7

Figure 7



h. The product perspective for the ISC whitening board is shown in Figure 8. Two whitening boards will be mounted in a single 1U chassis such that a single whitening chassis serves a single RF demodulator chassis.

Figure 8