LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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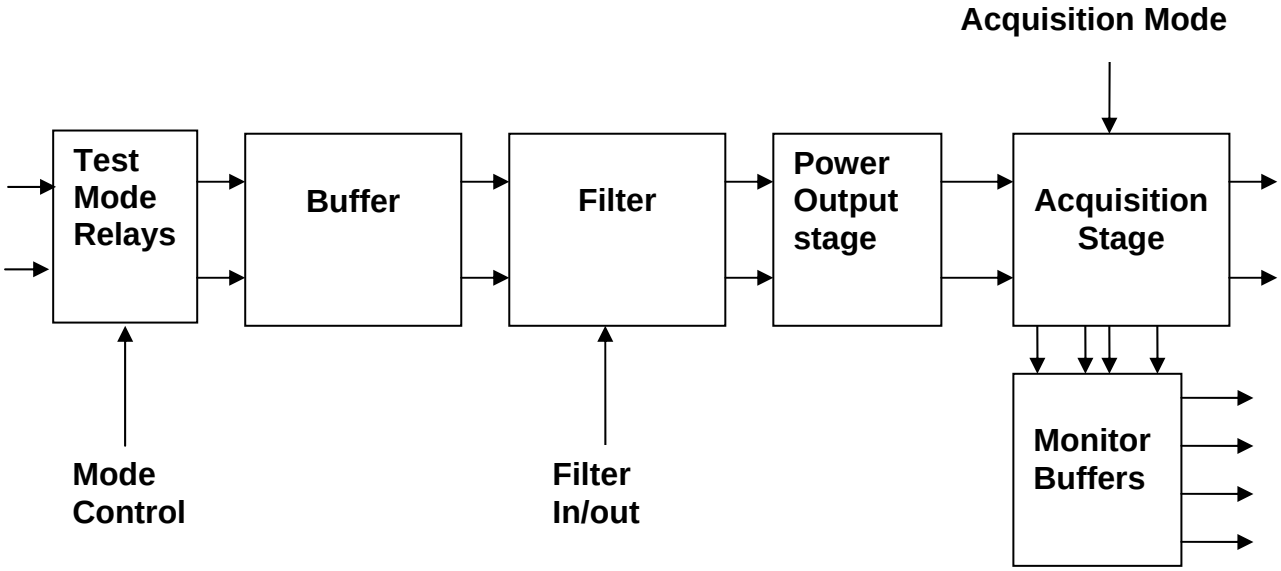
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……Serial No ……
Test Engineer ……
Date ……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number

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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	
2	PD2P	Photodiode B+	2	
3	PD3P	Photodiode C+	3	
4	PD4P	Photodiode D+	4	
5	0V			
6	PD1N	Photodiode A-	14	
7	PD2N	Photodiode B-	15	
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	

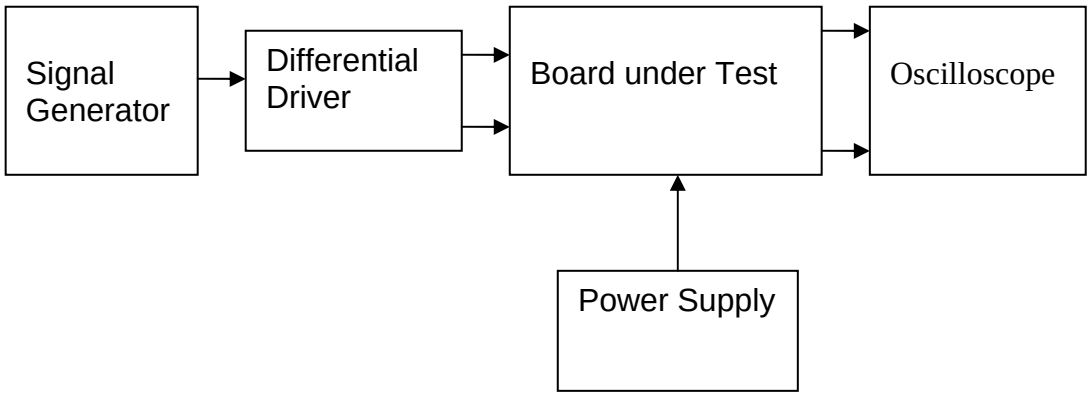
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	
2	Imon2P		6	
3	Imon3P		7	
4	Imon4P		8	
5	0V			
6	Imon1N		18	
7	Imon2N		19	
8	Imon3N		20	
9	Imon4N		21	

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	
10	V+ (TP1)	+17v Supply	
11	V- (TP2)	-17v Supply	
12	V- (TP2)	-17v Supply	
13	0V (TP3)		
22	0V (TP3)		
23	0V (TP3)		
24	0V (TP3)		
25	0V (TP3)		

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power
Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5			
+15v TP4			
-15v TP6			

All Outputs smooth DC, no oscillation?	

Record Power Supply Currents

Supply	**Current**
+16.5v	
-16.5v	

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1			
Ch2			
Ch3			
Ch4			

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1			
Ch2			
Ch3			
Ch4			

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1			
Ch2			
Ch3			
Ch4			

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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1		Pin 1 to Pin 2		
2		Pin 5 to Pin 6		
3		Pin 9 to Pin 10		
4		Pin 13 to Pin 14		

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1		Pin 3 to Pin 4		
2		Pin 7 to Pin 8		
3		Pin 11 to Pin 12		
4		Pin 15 to Pin 16		

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-40dB	-36dB	
Ch2		-40dB	-36dB	
Ch3		-40dB	-36dB	
Ch4		-40dB	-36dB	

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-42.5dB	-39.5dB	
Ch2		-42.5dB	-39.5dB	
Ch3		-42.5dB	-39.5dB	
Ch4		-42.5dB	-39.5dB	

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-53dB	-50dB	
Ch2		-53dB	-50dB	
Ch3		-53dB	-50dB	
Ch4		-53dB	-50dB	

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-30dB	-27dB	
Ch2		-30dB	-27dB	
Ch3		-30dB	-27dB	
Ch4		-30dB	-27dB	

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-21dB	-18dB	
Ch2		-21dB	-18dB	
Ch3		-21dB	-18dB	
Ch4		-21dB	-18dB	

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1		-21dB	-18dB	
Ch2		-21dB	-18dB	
Ch3		-21dB	-18dB	
Ch4		-21dB	-18dB	

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-36.5dB / 20mV	-33.5dB / 16mV	
Ch2		-36.5dB / 20mV	-33.5dB / 16mV	
Ch3		-36.5dB / 20mV	-33.5dB / 16mV	
Ch4		-36.5dB / 20mV	-33.5dB / 16mV	

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-20dB / 122mV	-17dB / 118mV	
Ch2		-20dB / 122mV	-17dB / 118mV	
Ch3		-20dB / 122mV	-17dB / 118mV	
Ch4		-20dB / 122mV	-17dB / 118mV	

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-6dB / 570mV	-4dB / 565mV	
Ch2		-6dB / 570mV	-4dB / 565mV	
Ch3		-6dB / 570mV	-4dB / 565mV	
Ch4		-6dB / 570mV	-4dB / 565mV	

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-4.5dB / 665 mV	-2.5dB / 672mV	
Ch2		-4.5dB / 665 mV	-2.5dB / 672mV	
Ch3		-4.5dB / 665 mV	-2.5dB / 672mV	
Ch4		-4.5dB / 665 mV	-2.5dB / 672mV	

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-4.5dB / 675mV	-2.5dB / 665mV	
Ch2		-4.5dB / 675mV	-2.5dB / 665mV	
Ch3		-4.5dB / 675mV	-2.5dB / 665mV	
Ch4		-4.5dB / 675mV	-2.5dB / 665mV	

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1		
Ch2		
Ch3		
Ch4		

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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v								
-1v								
0v								
1v								
5v								