LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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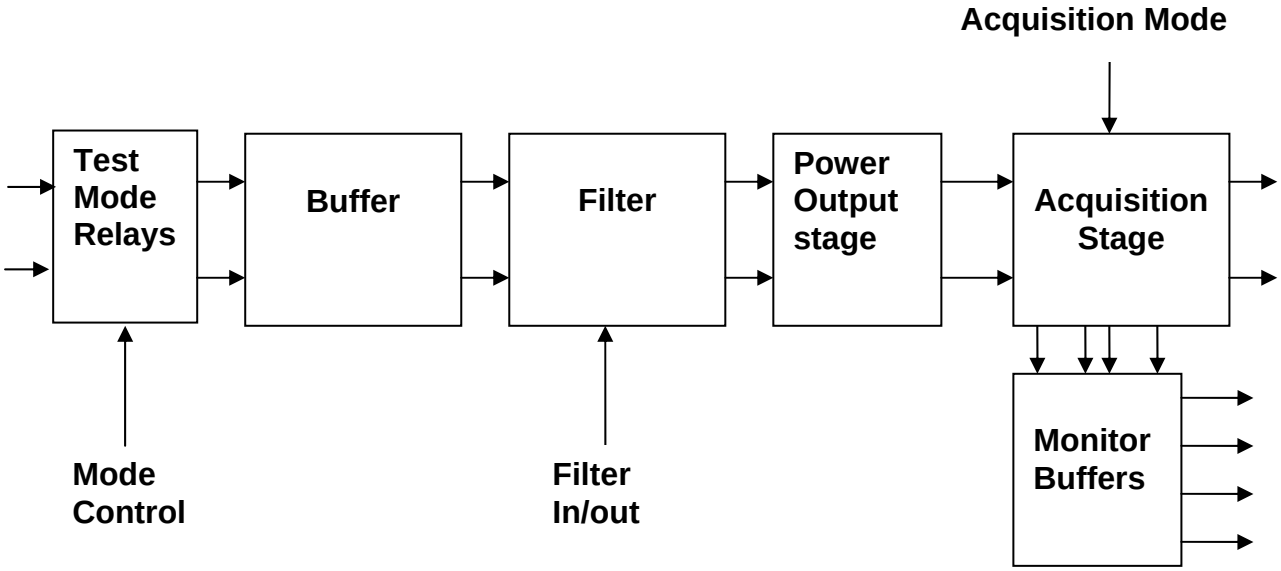
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

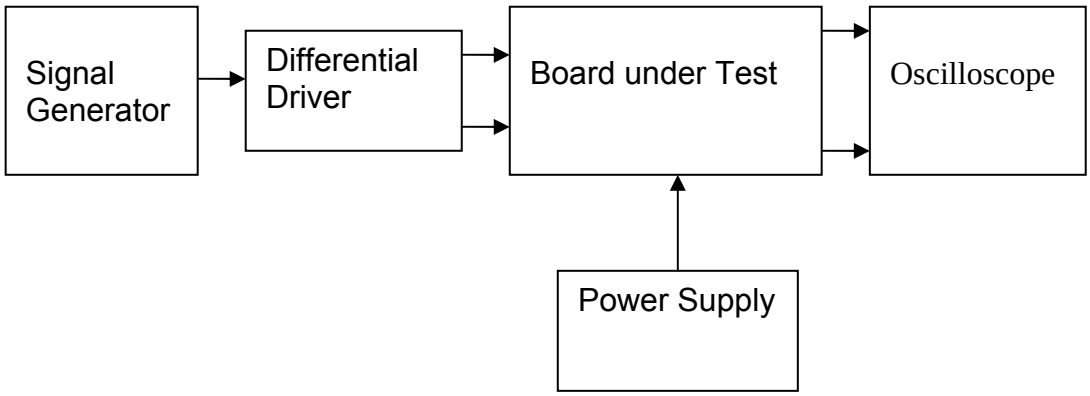
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.82V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.1	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-29.2	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P84….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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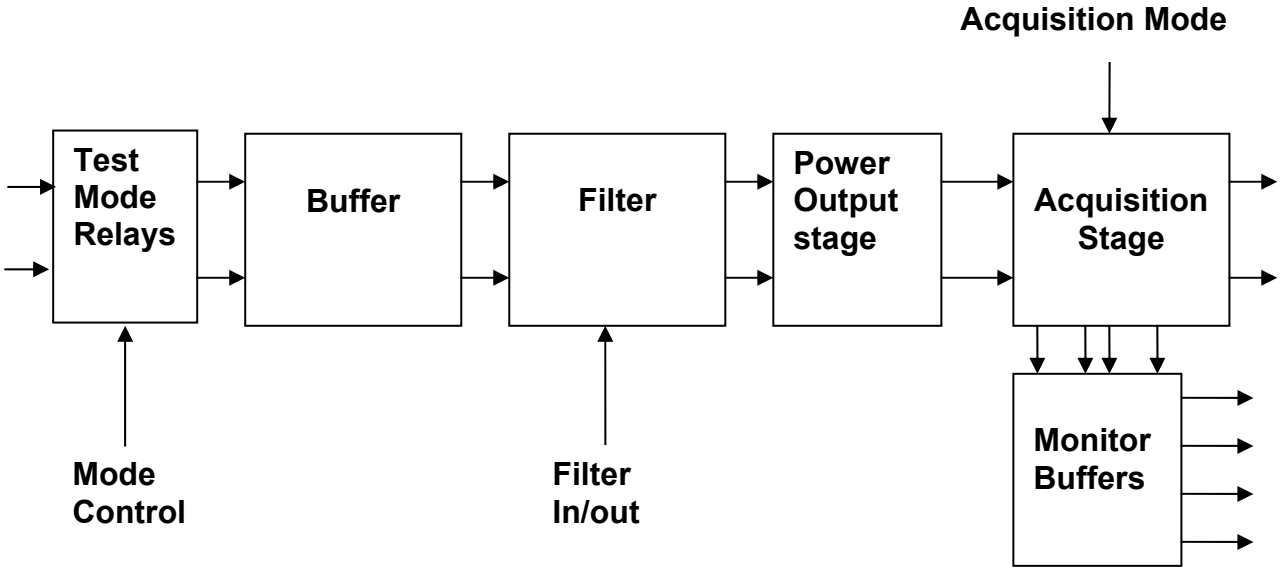
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/10/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/10/10……

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt/Xen……
Date …15/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

General alignment of SM components is not great.

Removed and replaced R11 on CH4 with the correct value of 3k3.

Removed and replaced R15 on CH4 with the correct value of 100k.

IC2 and IC8 on CH4 have been replaced and also IC8 on CH3.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

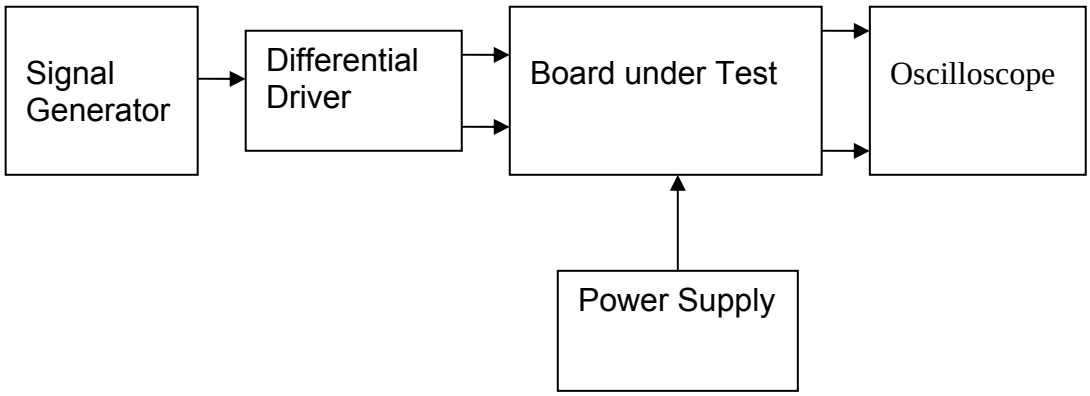
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.92V	√	1mV
-15v TP6	15.12V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.198V	Pin 1 to Pin 2	2.196V	√
2	2.197V	Pin 5 to Pin 6	2.196V	√
3	2.198V	Pin 9 to Pin 10	2.196V	√
4	2.197V	Pin 13 to Pin 14	2.196V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.283V	Pin 3 to Pin 4	0.283V	√
2	0.282V	Pin 7 to Pin 8	0.281V	√
3	0.284V	Pin 11 to Pin 12	0.284V	√
4	0.285V	Pin 15 to Pin 16	0.284V	√

Unit……T_ACQ_P1…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…1/4/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	27.0	-40dB/25mV	-36dB/28mV	√
Ch2	27.0	-40dB/25mV	-36dB/28mV	√
Ch3	27.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.4	-30dB	-27dB	√
Ch4	-28.4	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……T_ACQ_P1…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…5/10/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P1….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

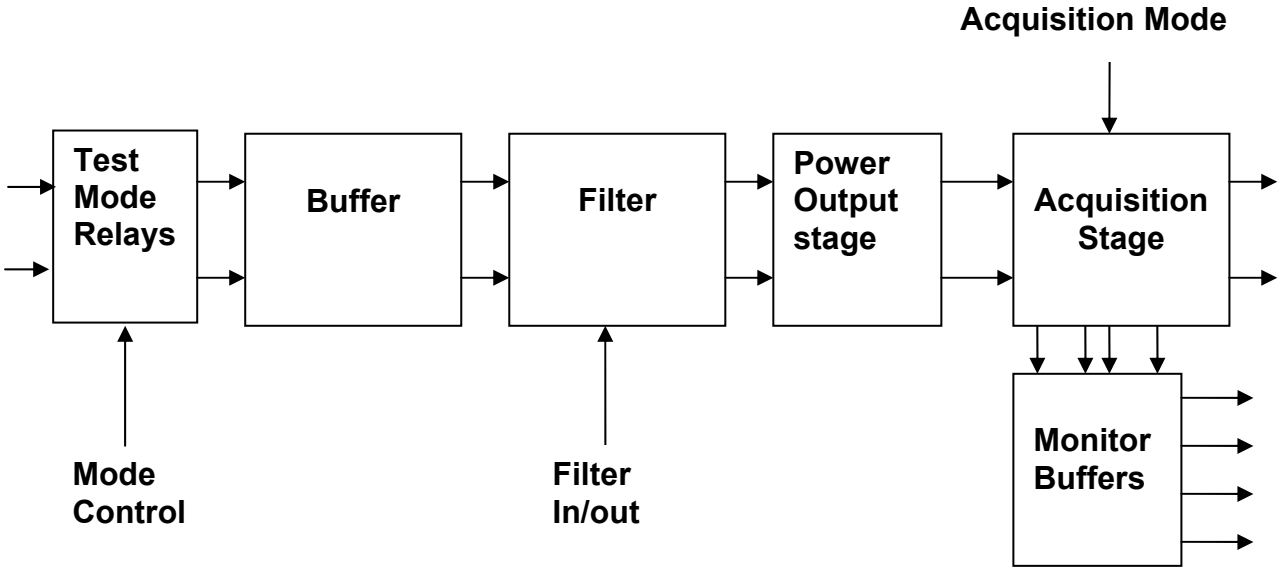
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

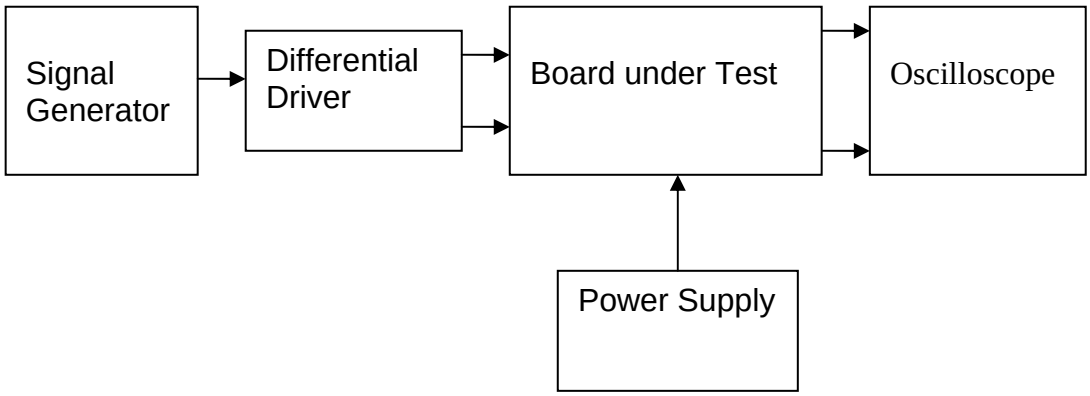
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.99V	√	1mV
-15v TP6	15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.282V	Pin 3 to Pin 4	0.282V	√
2	0.284V	Pin 7 to Pin 8	0.284V	√
3	0.284V	Pin 11 to Pin 12	0.283V	√
4	0.284V	Pin 15 to Pin 16	0.283V	√

Unit……T_ACQ_P2…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.0	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.3	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……T_ACQ_P2…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.8	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.2V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P2….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	4.5V	√	-4.5V	√	4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

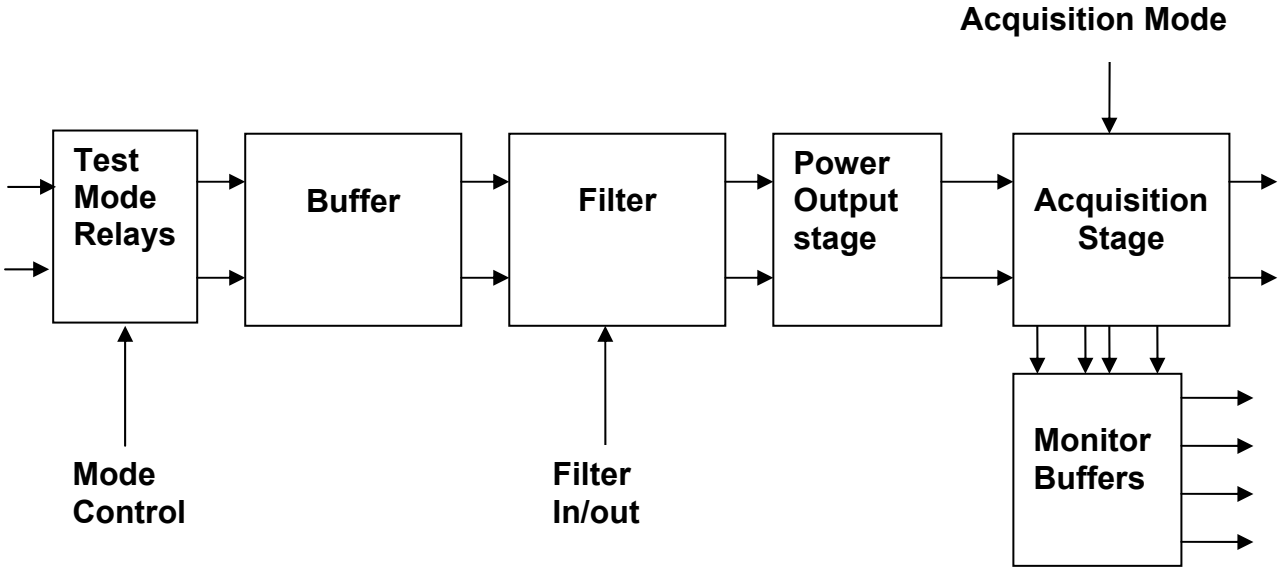
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

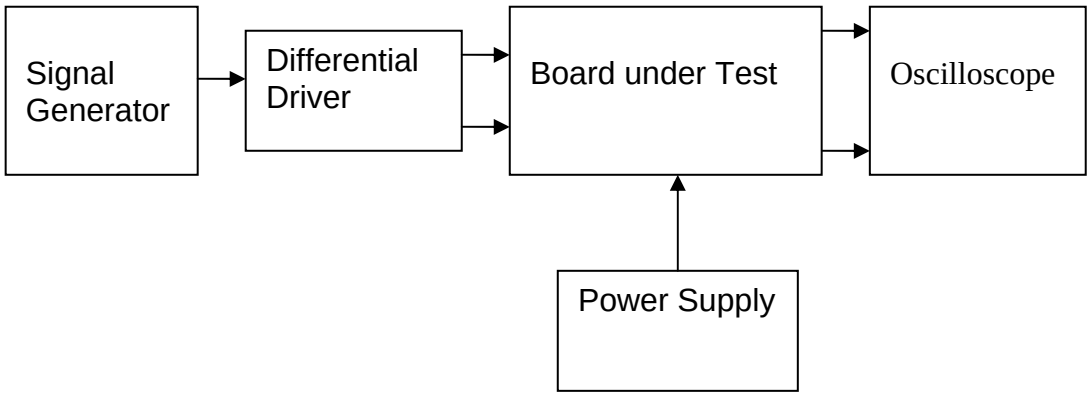
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P3…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.5	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P3…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.8	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P3….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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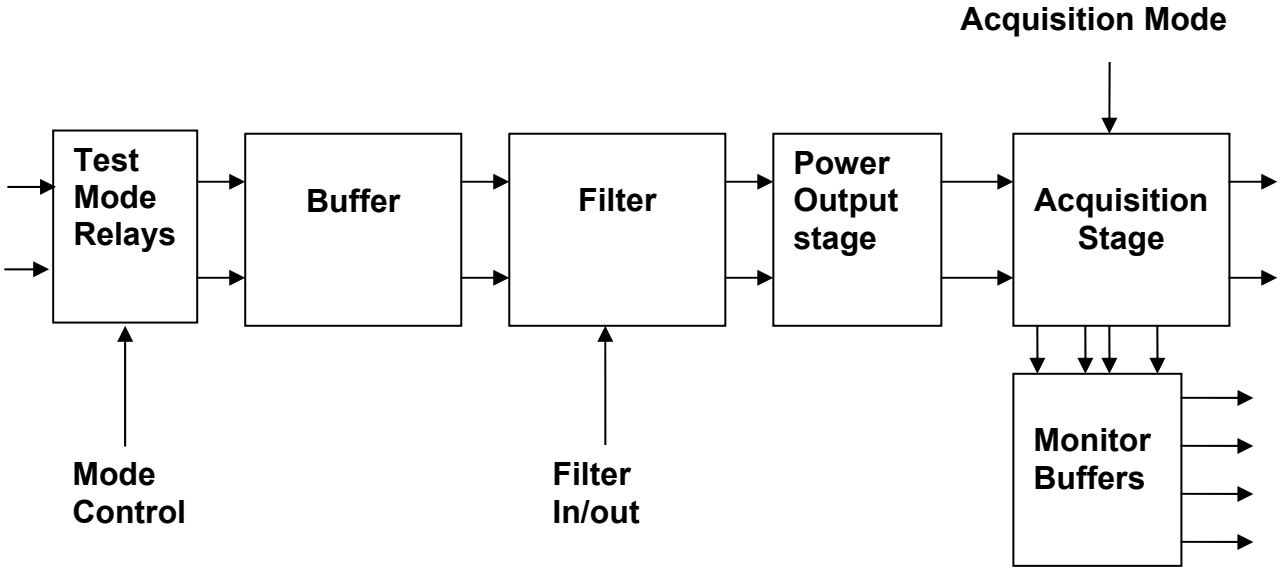
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Removed solder splashes on two mounting holes.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

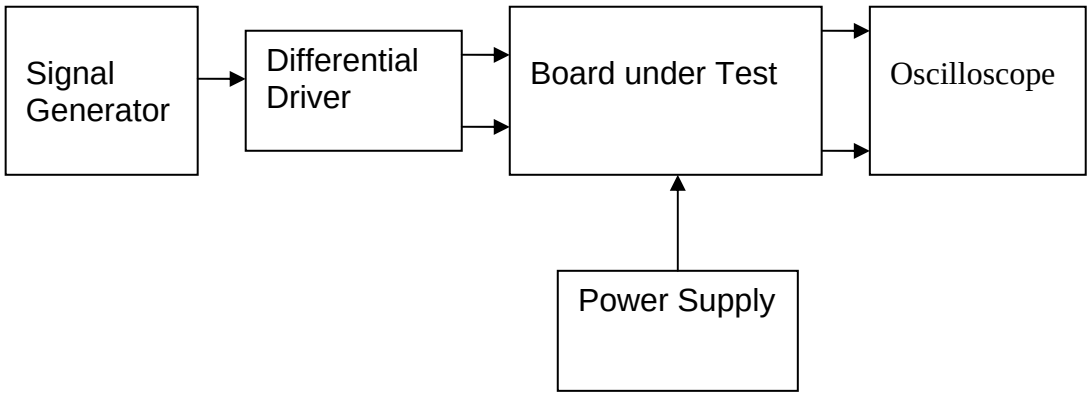
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	14.83V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P4…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.4	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P4…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…1/4/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P4….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

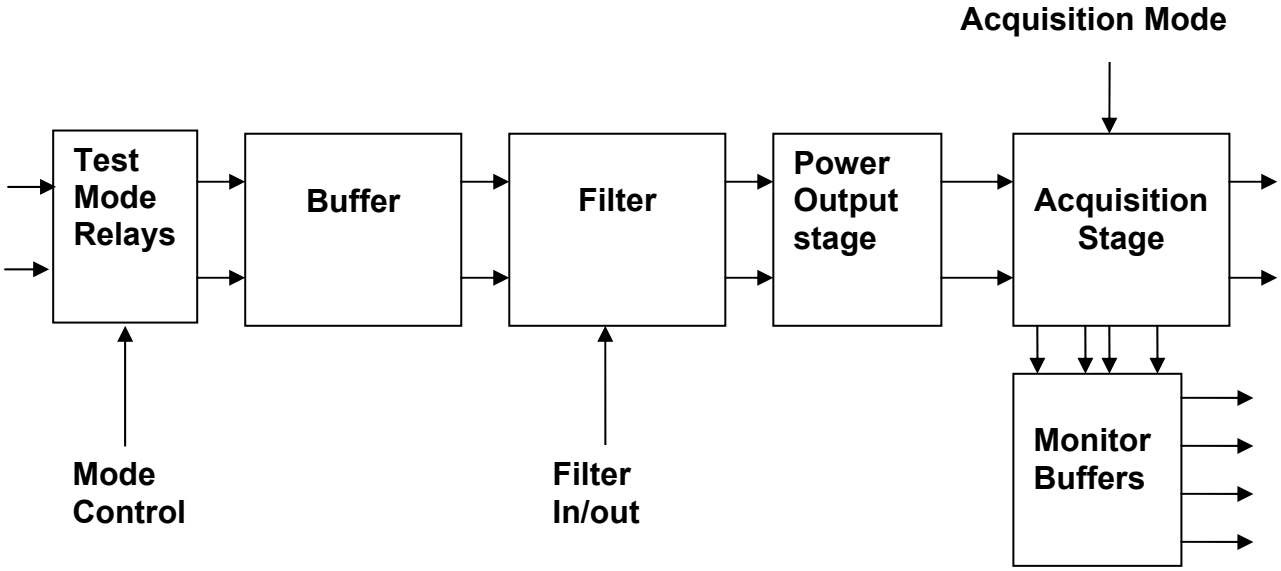
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

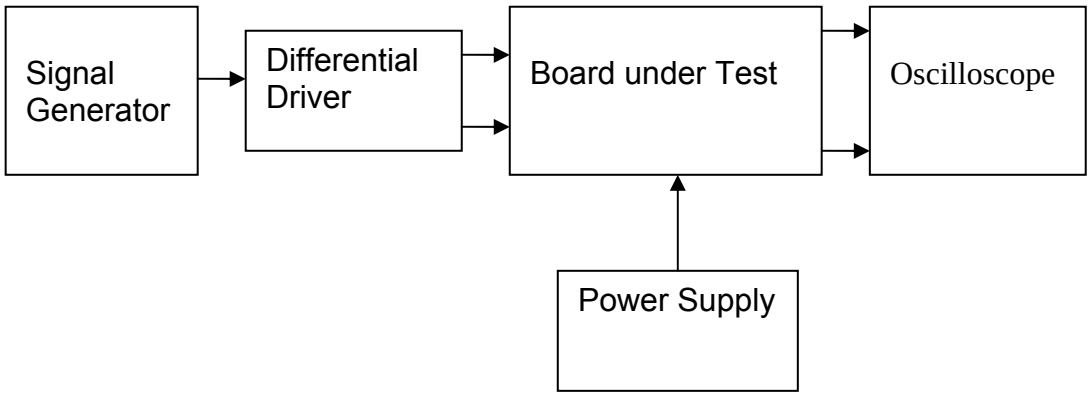
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.04V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.01V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.8	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P5….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

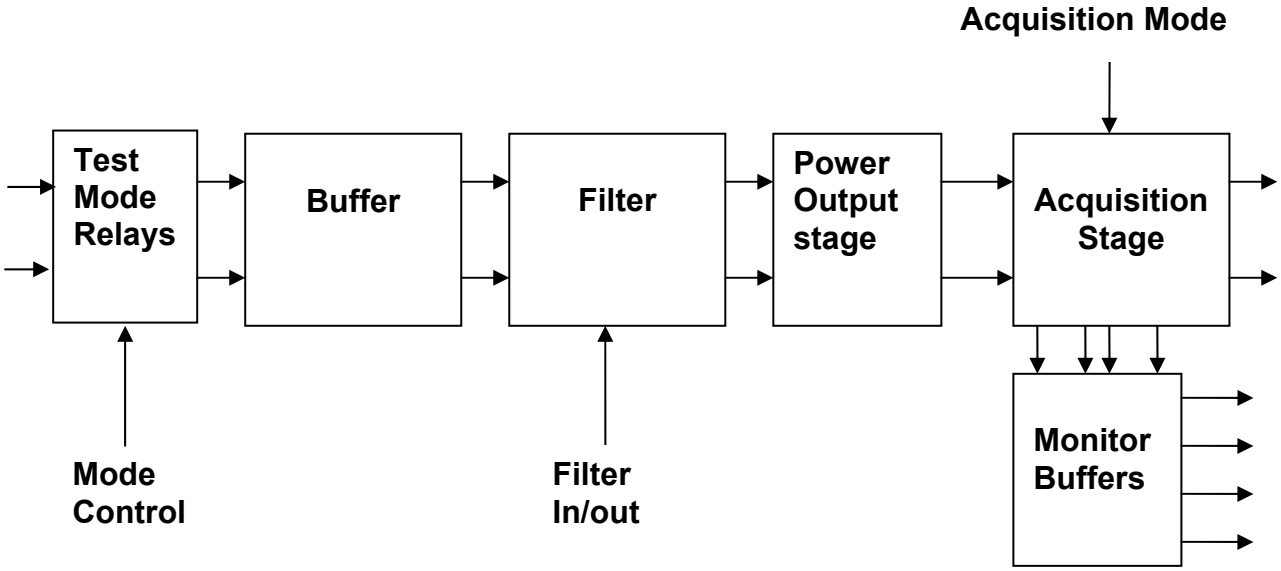
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

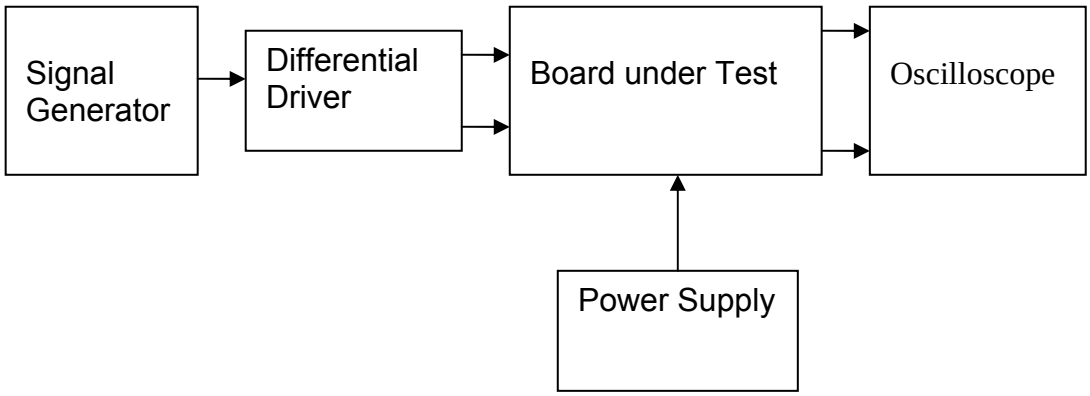
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.14V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.98V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-27	-40dB/25mV	-36dB/28mV	√
Ch2	-27	-40dB/25mV	-36dB/28mV	√
Ch3	-27	-40dB/25mV	-36dB/28mV	√
Ch4	-27	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-29	-30dB	-27dB	√
Ch4	-29	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P6….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/03/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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Unit…T_ACQ_P7….Serial No ……
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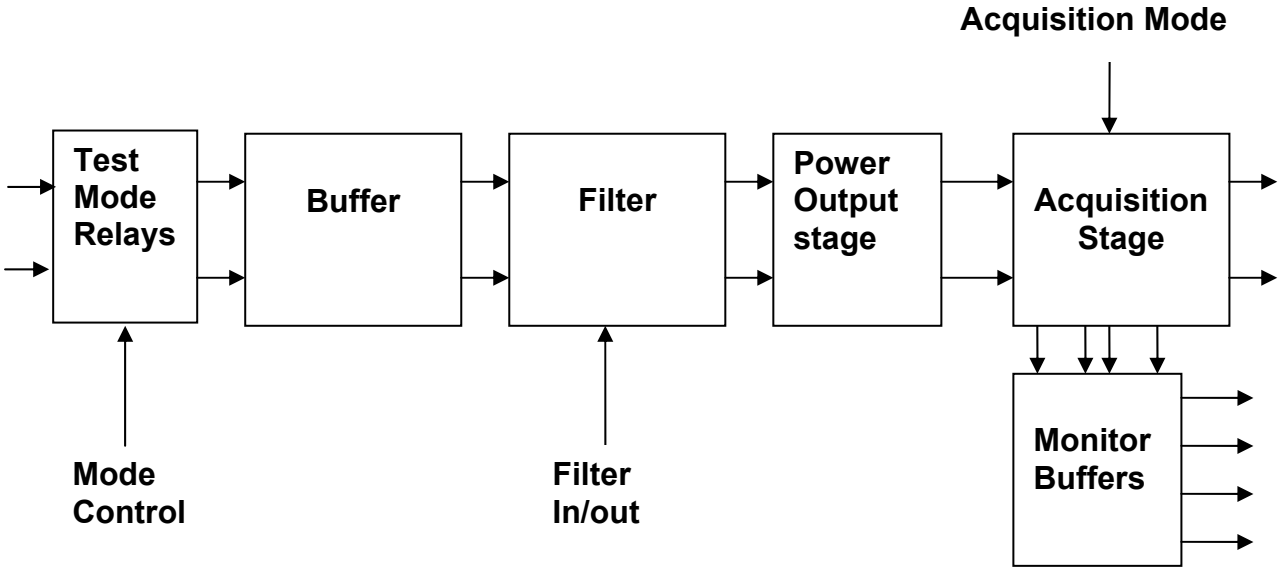
Date …17/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

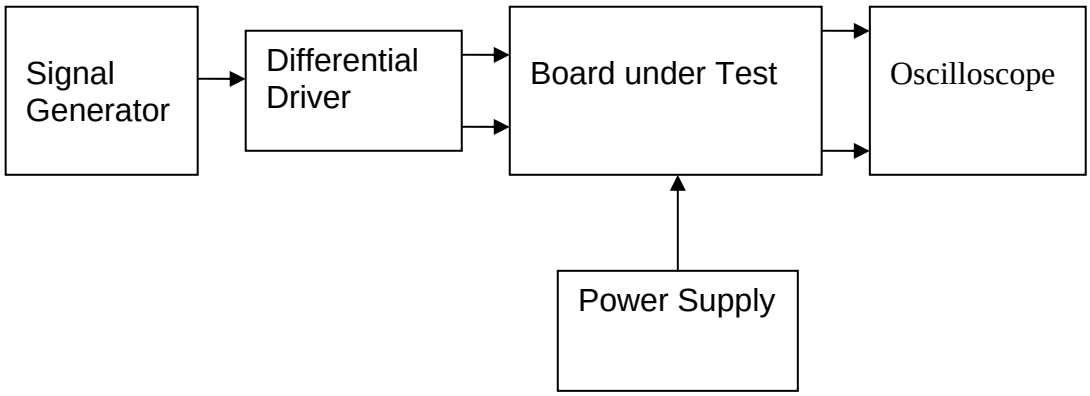
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P7….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.98V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P7….Serial No ……
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7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P7….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

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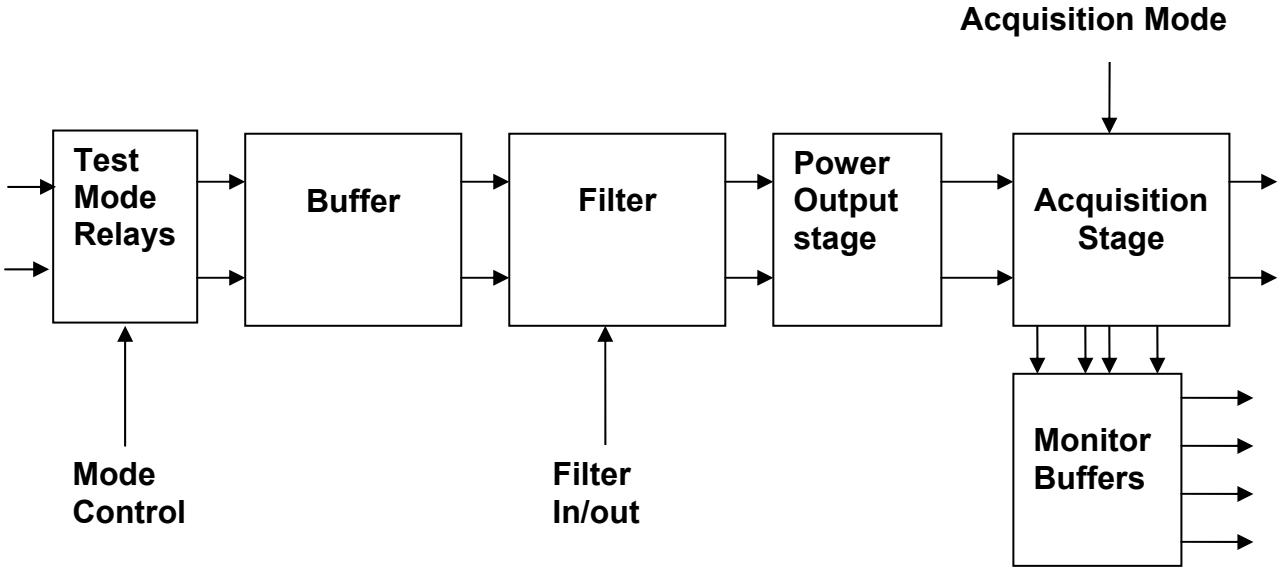
Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

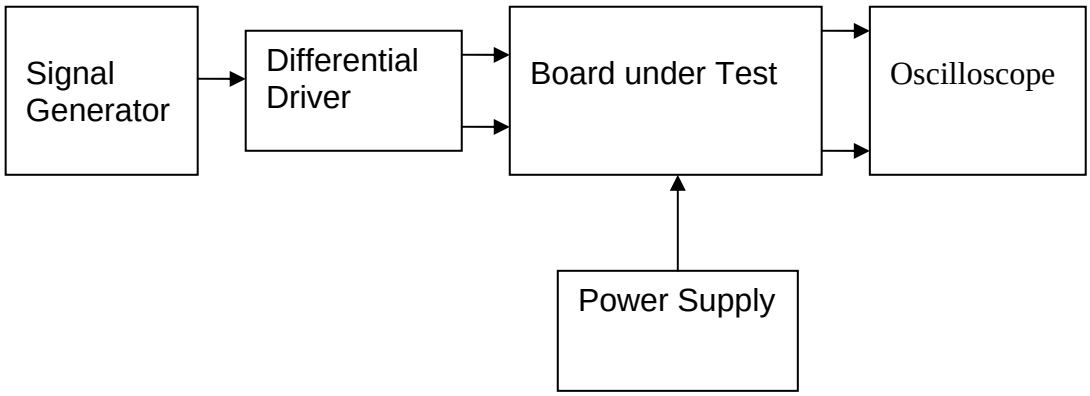
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.92V	√	1mV
-15v TP6	-14.98V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

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Test Engineer …Simon Pyatt……
Date …18/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P8…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P8…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.0	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P8….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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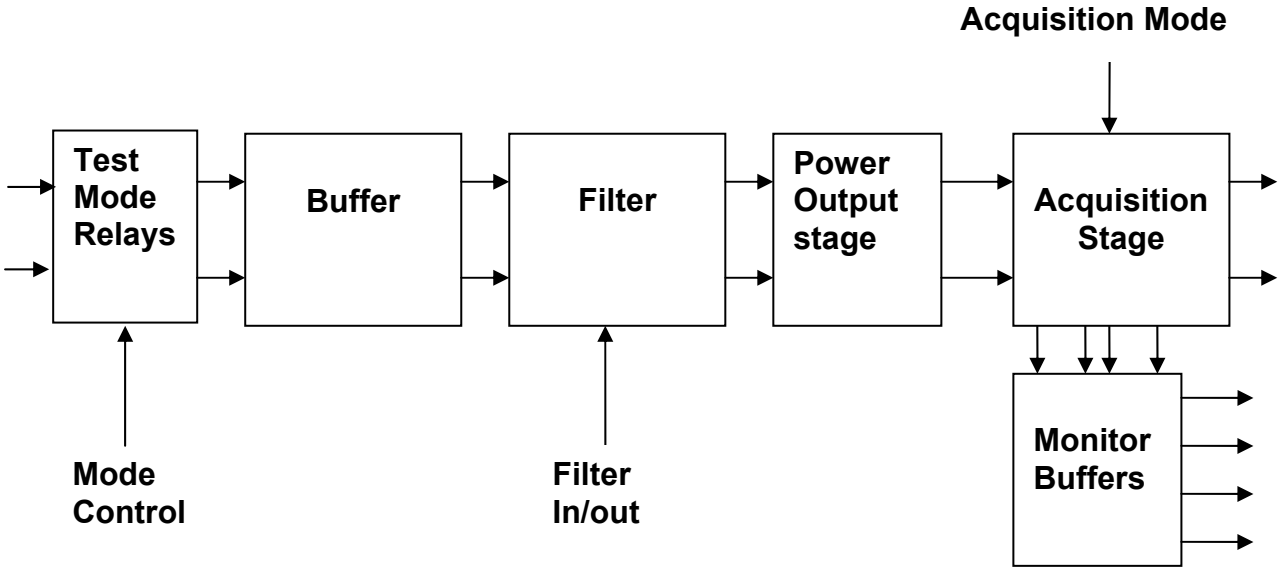
Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

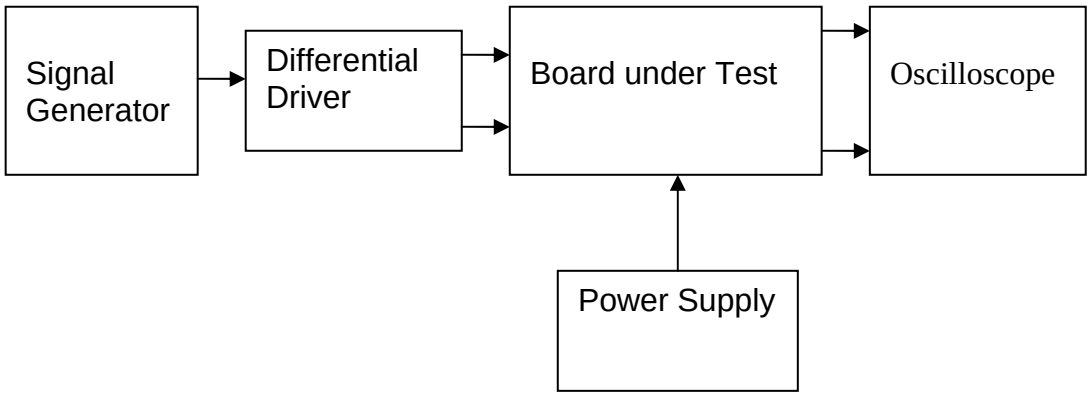
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.01V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P9…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	28.0	-40dB/25mV	-36dB/28mV	√
Ch2	27.0	-40dB/25mV	-36dB/28mV	√
Ch3	27.0	-40dB/25mV	-36dB/28mV	√
Ch4	27.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P9…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P9….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

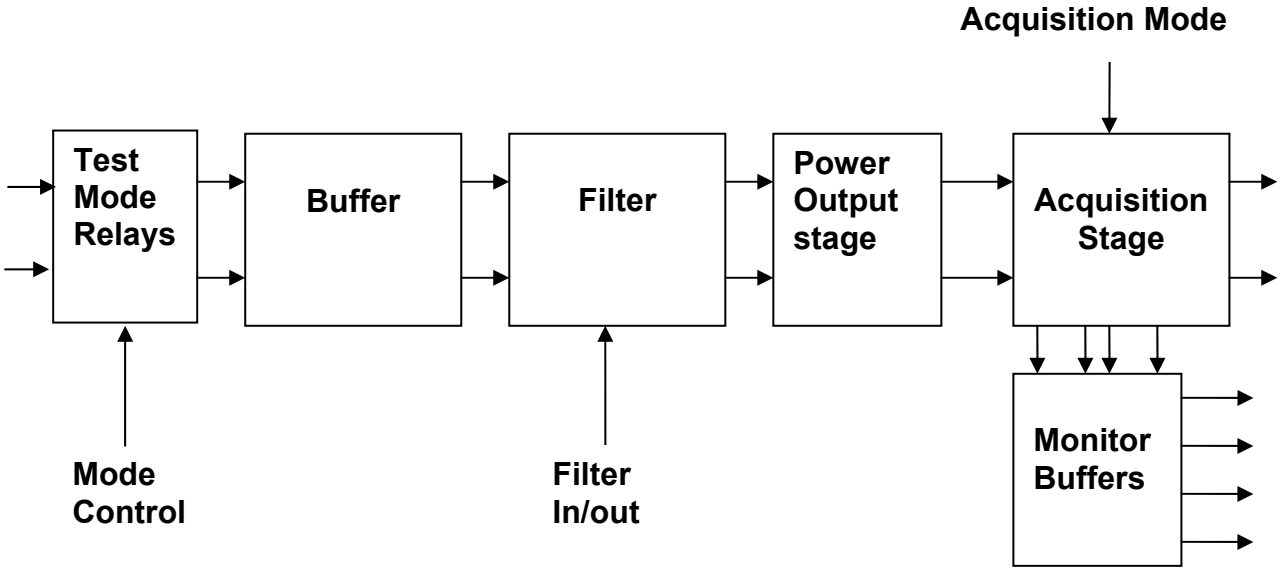
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

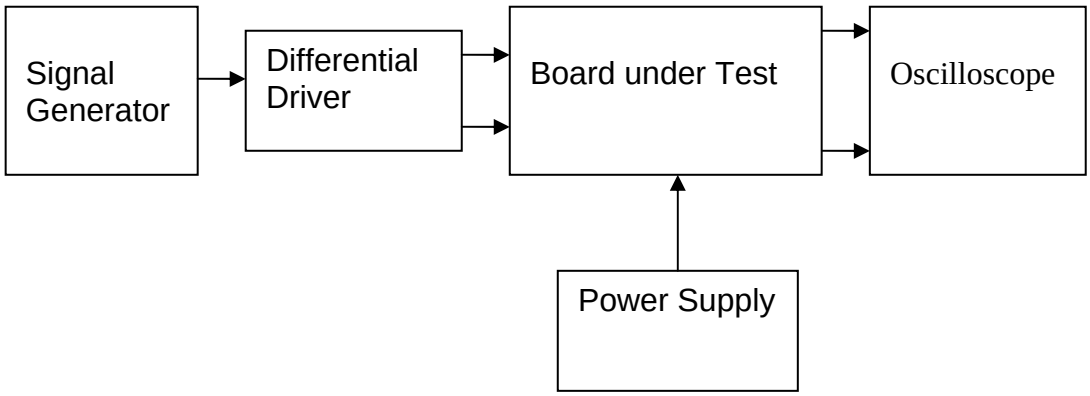
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.10V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P10…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.9	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.4	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……T_ACQ_P10…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P10….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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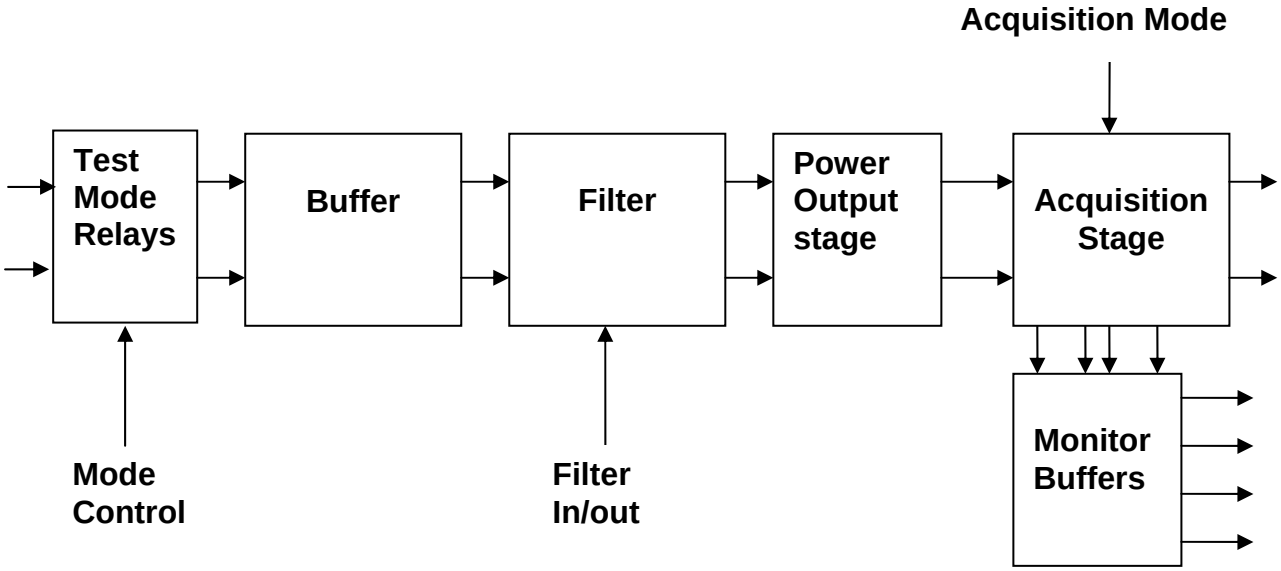
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	77 III	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
V/I calibrator	Time Electronics	1044	

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…25/3/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…19/3/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

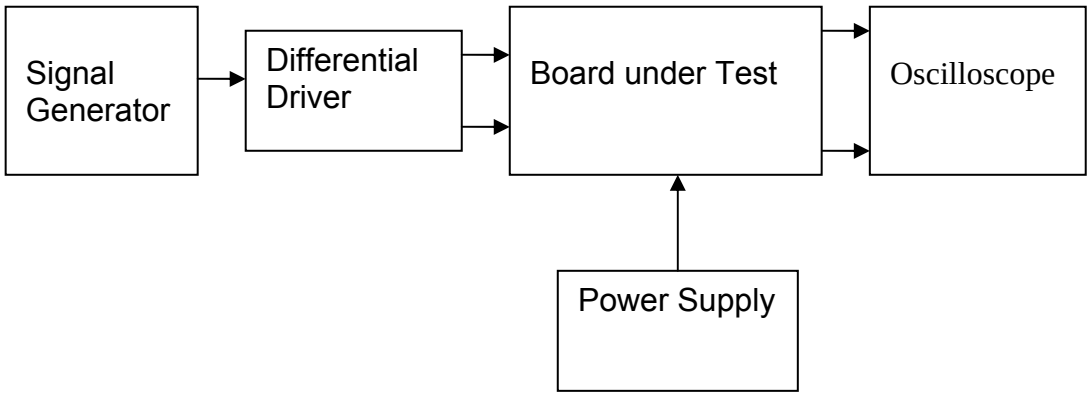
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04	√	1mV
+15v TP4	14.97	√	1mV
-15v TP6	-15.01	√	1mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	300mA
-16.5v	200mA

If the supplies are correct, proceed to the next test.

Unit……T_ACQ_P11…….. ….Serial No ……
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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…25/3/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.196	Pin 1 to Pin 2	2.195	√
2	2.196	Pin 5 to Pin 6	2.195	√
3	2.196	Pin 9 to Pin 10	2.195	√
4	2.196	Pin 13 to Pin 14	2.195	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.280	Pin 3 to Pin 4	0.280	√
2	0.278	Pin 7 to Pin 8	0.277	√
3	0.278	Pin 11 to Pin 12	0.278	√
4	0.281	Pin 15 to Pin 16	0.280	√

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-37.5	-40dB/25mV	-36dB/28mV	√
Ch2	-37.6	-40dB/25mV	-36dB/28mV	√
Ch3	-37.5	-40dB/25mV	-36dB/28mV	√
Ch4	-37.5	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.8	-42.5dB	-39.5dB	√
Ch3	-40.9	-42.5dB	-39.5dB	√
Ch4	-40.9	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.8	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……T_ACQ_P11…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…26/3/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22.0	√	-22.0	√	-22.0	√	-21.9	√
-1v	-4.5	√	-4.5	√	-4.5	√	-4.5	√
0v	0	√	0	√	0	√	0	√
1v	4.3	√	4.2	√	4.3	√	4.5	√
5v	21.9	√	21.8	√	21.9	√	22.0	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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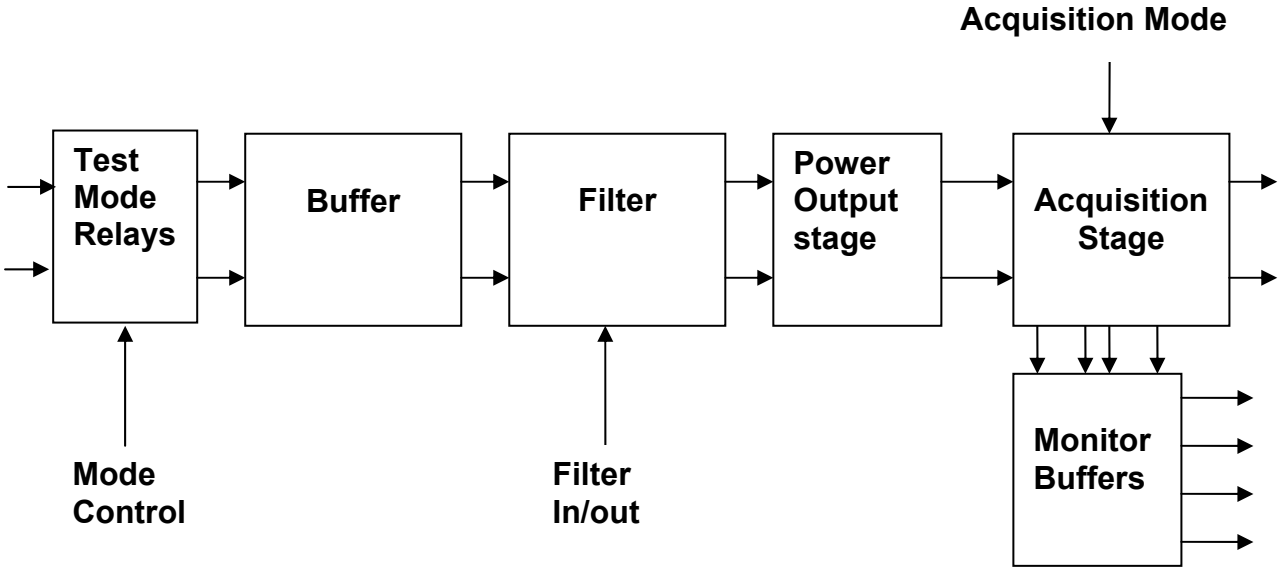
Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

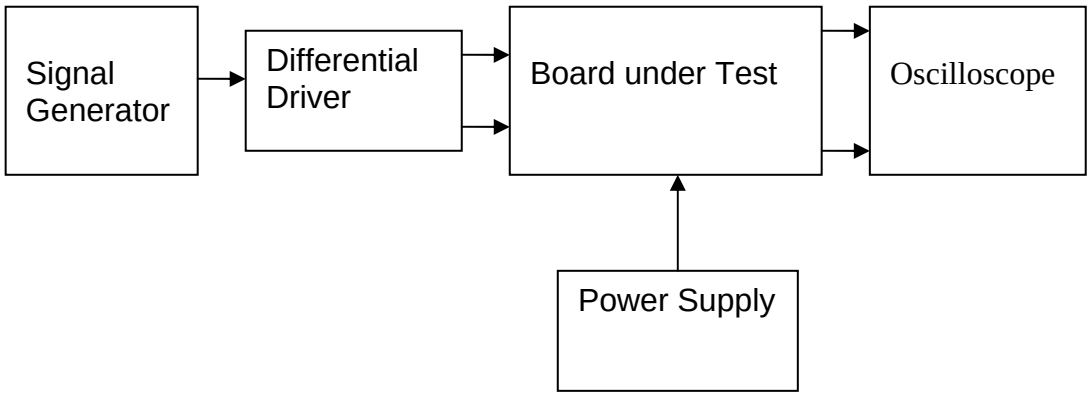
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P12…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.4	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P12…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…31/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P12….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

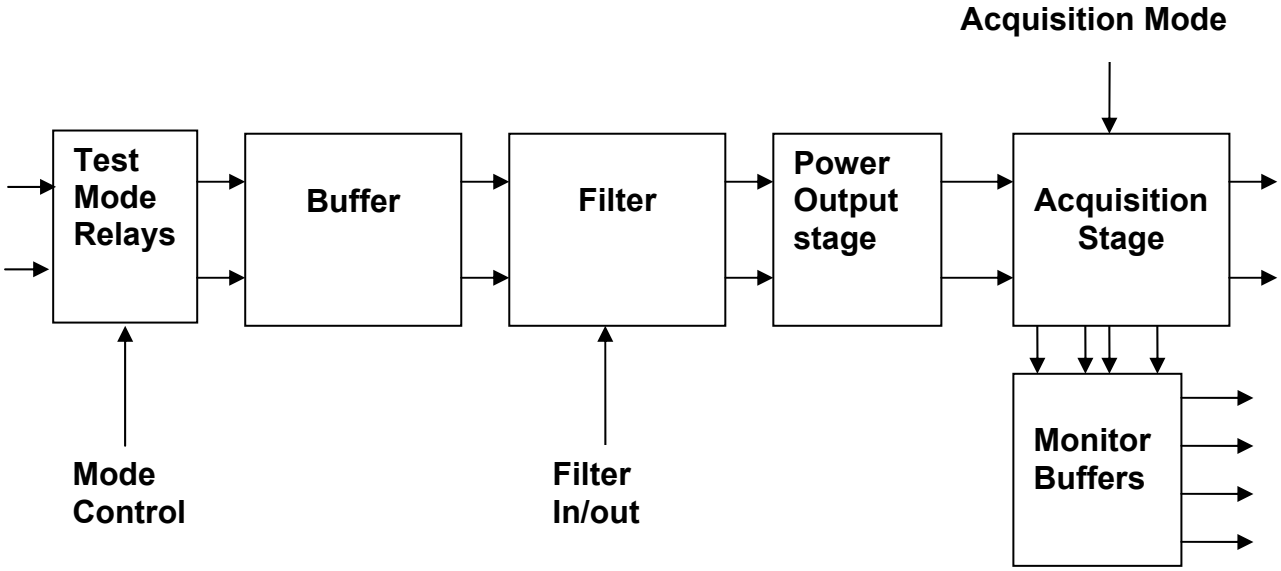
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

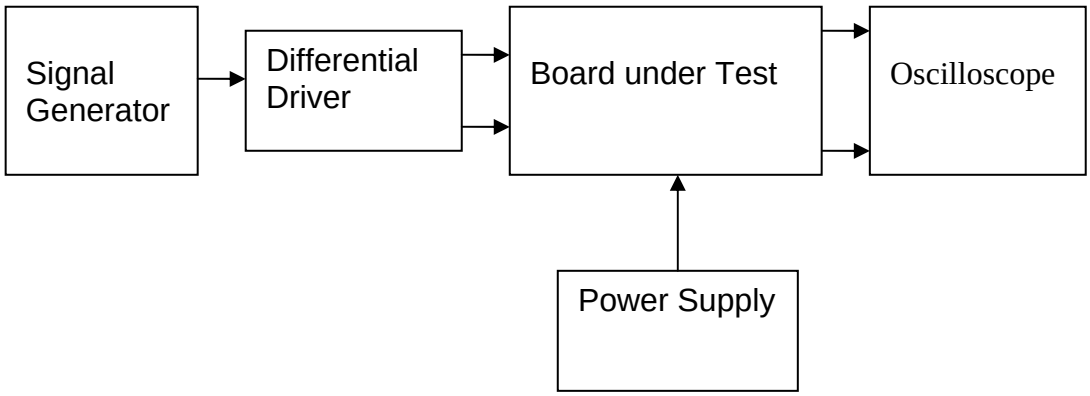
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.08V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10…….

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P13…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…30/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0mV	-40dB/25mV	-36dB/28mV	√
Ch2	26.0mV	-40dB/25mV	-36dB/28mV	√
Ch3	26.0mV	-40dB/25mV	-36dB/28mV	√
Ch4	26.0mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.8	-42.5dB	-39.5dB	√
Ch3	-40.8	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.4	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-29.0	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P13…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…30/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-17.9	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch3	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch2	-3.8	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.8	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.4V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P13….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

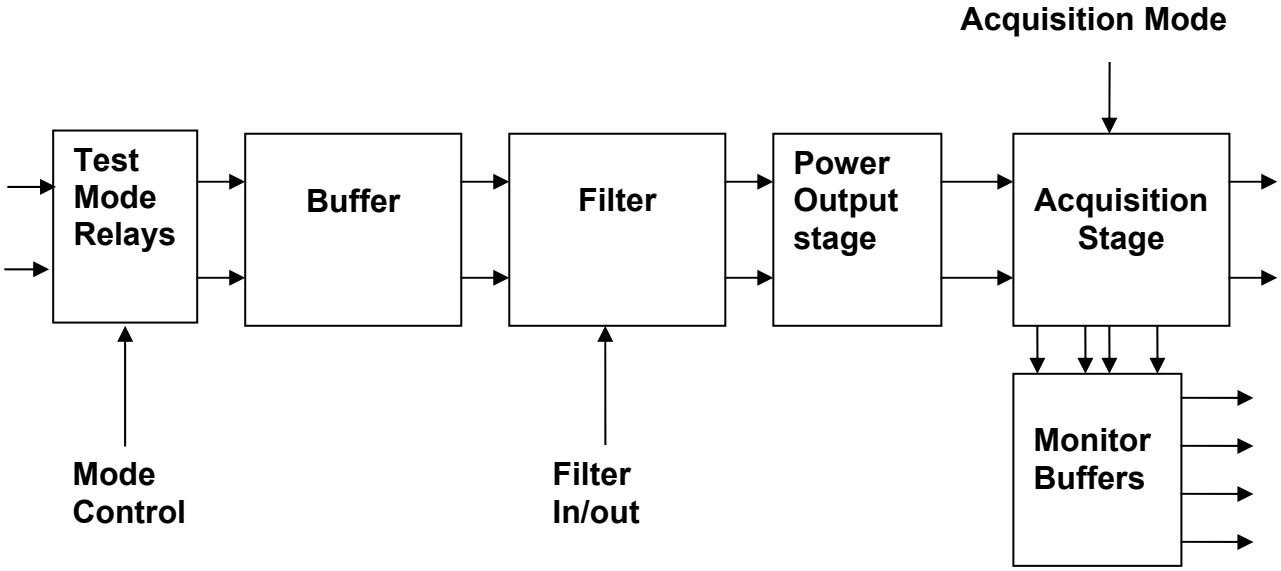
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

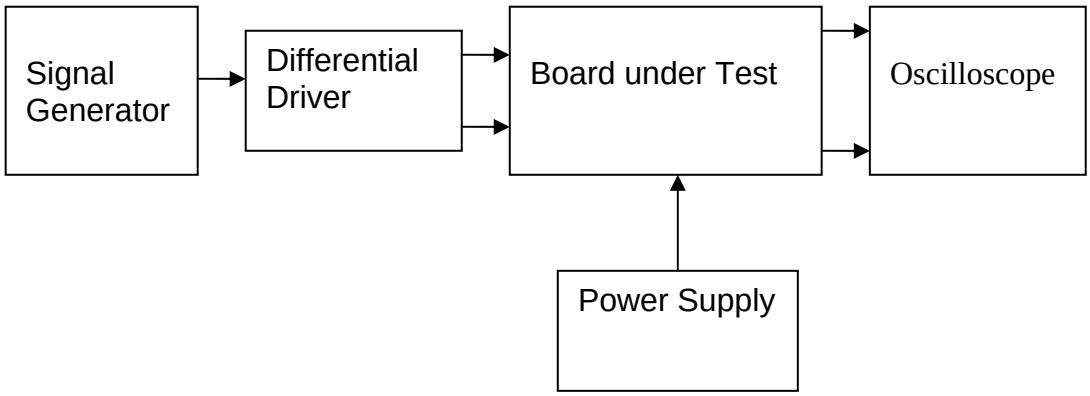
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P14….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	-15.05V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P14…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…30/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-29.0	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P14…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…30/3/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.8	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.8	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P14….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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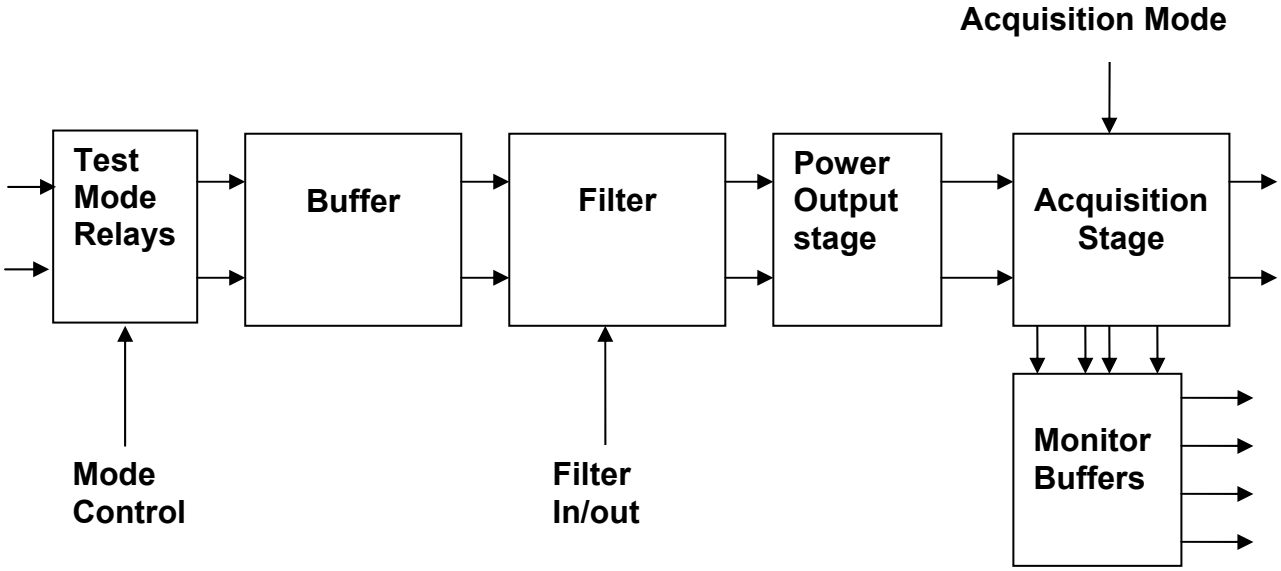
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

Contents

Block diagram



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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

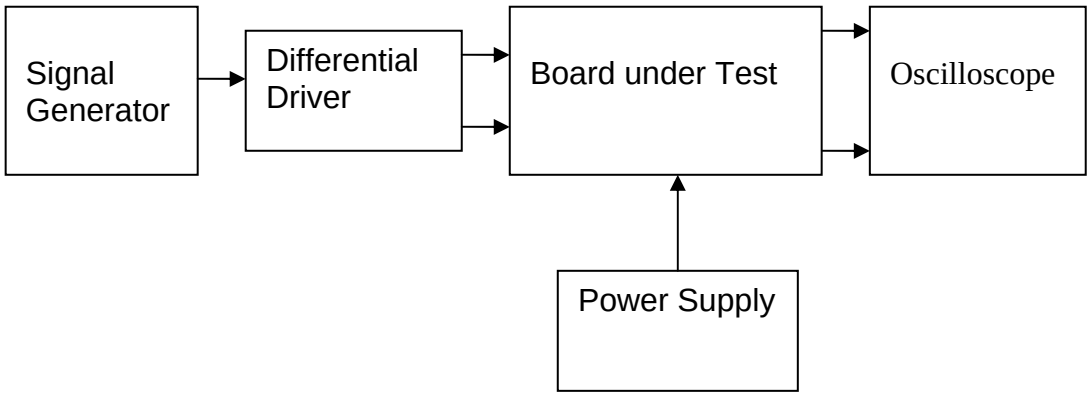
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_15P…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_15P…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P15….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

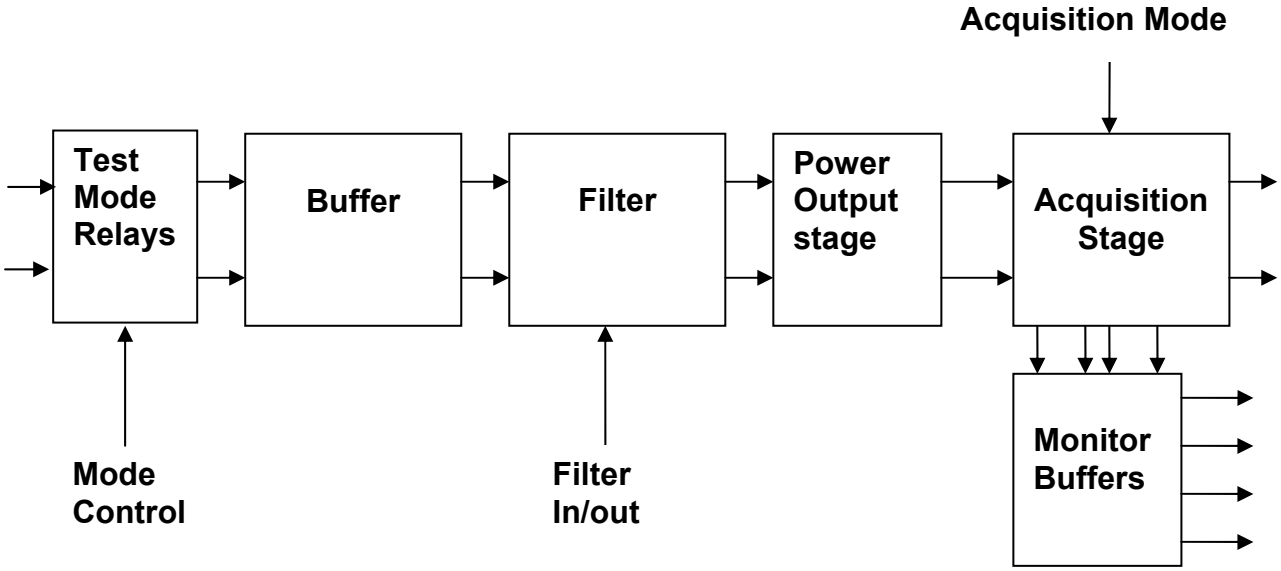
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Board slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

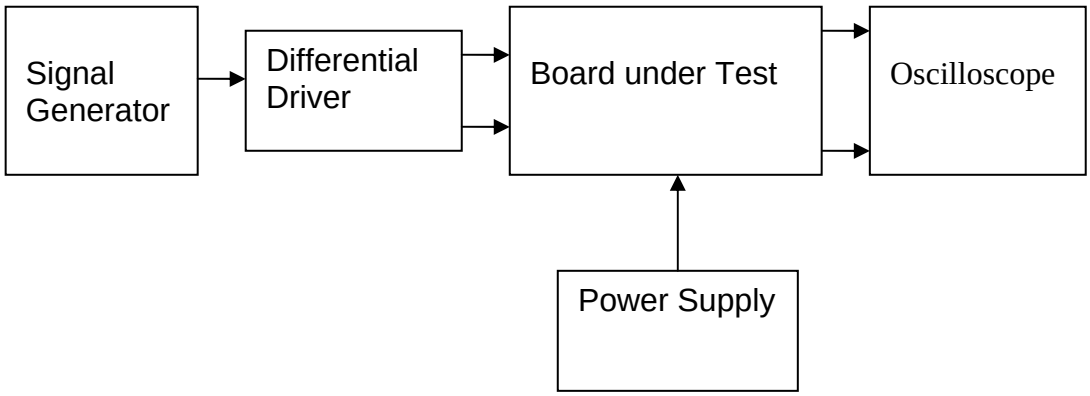
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-15.00V	√	1mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P16…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P16…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…30/3/10…….

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.1	-20dB / 122mV	-17dB / 118mV	
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P16….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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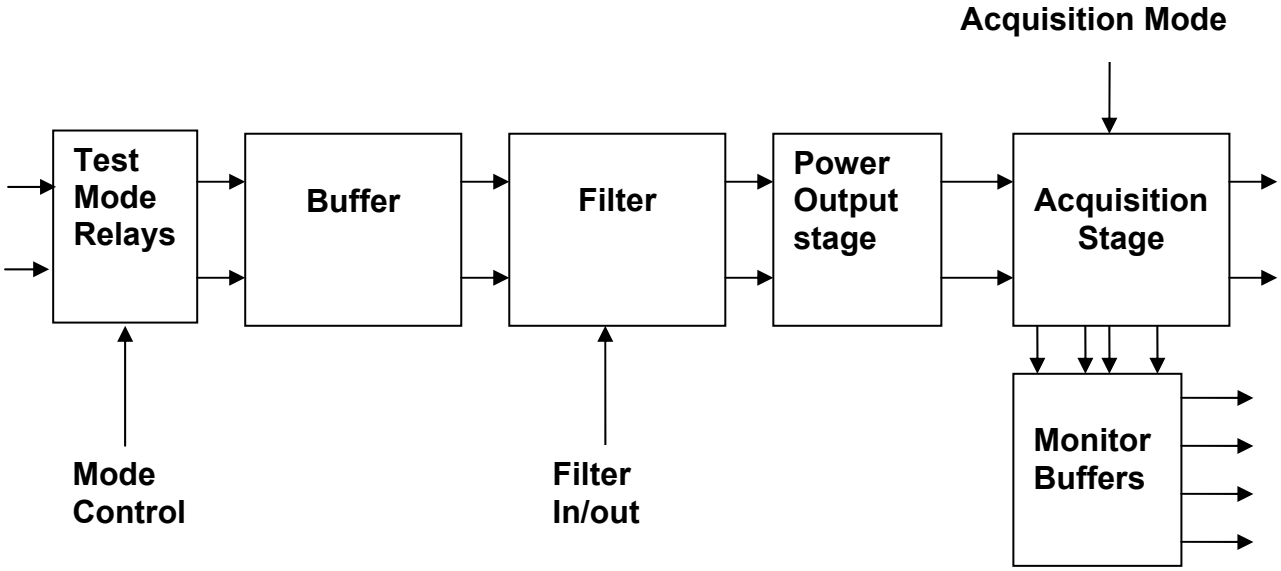
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

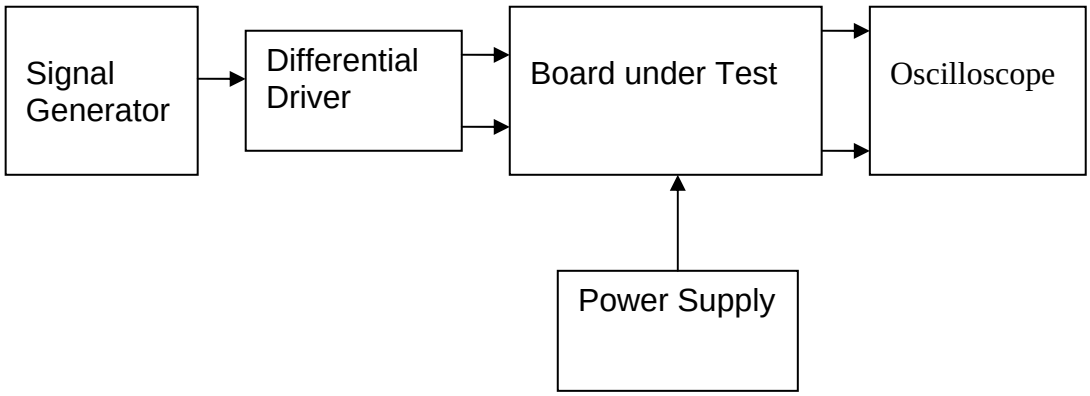
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.92V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_17P…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10…….

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.5	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_17P…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P17….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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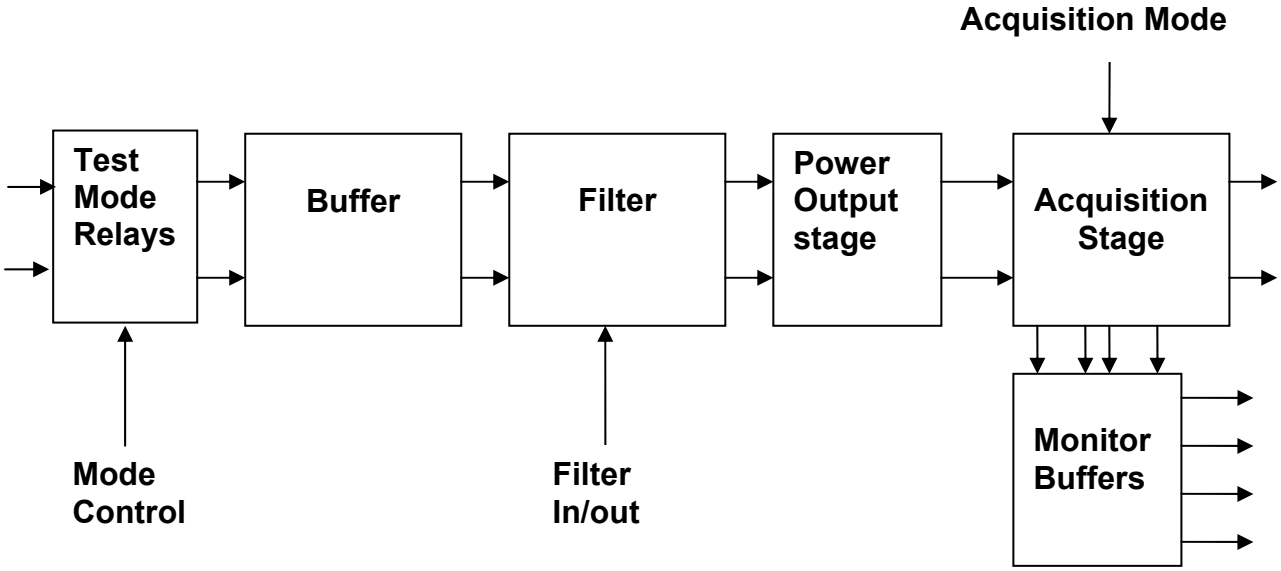
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

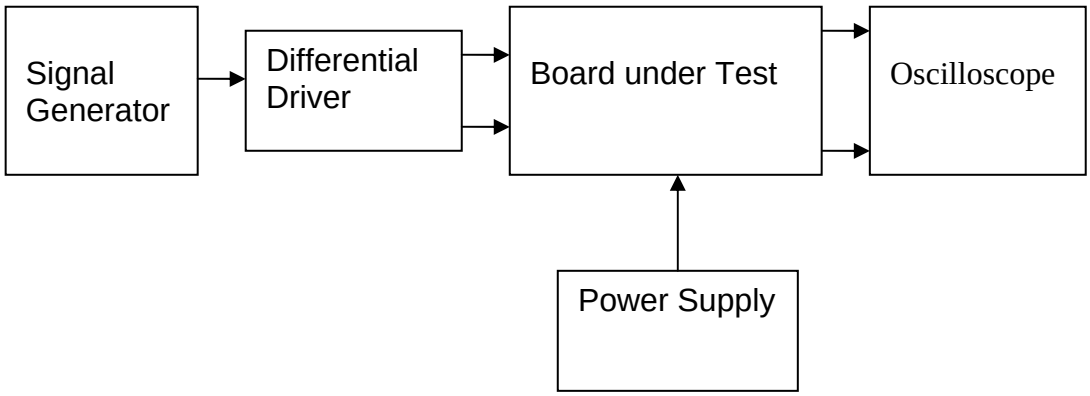
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P18…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.0	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.4	-30dB	-27dB	√
Ch2	-28.3	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.3	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P18…….. ….Serial No ……
Test Engineer…..Xen……
Date……..…29/3/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P18….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

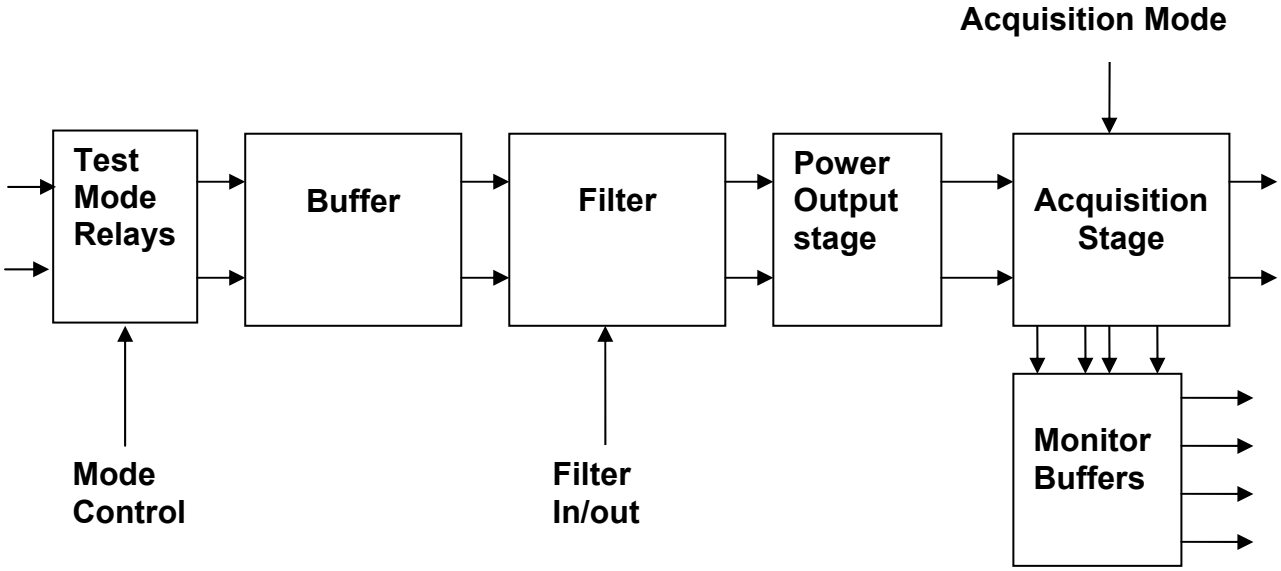
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

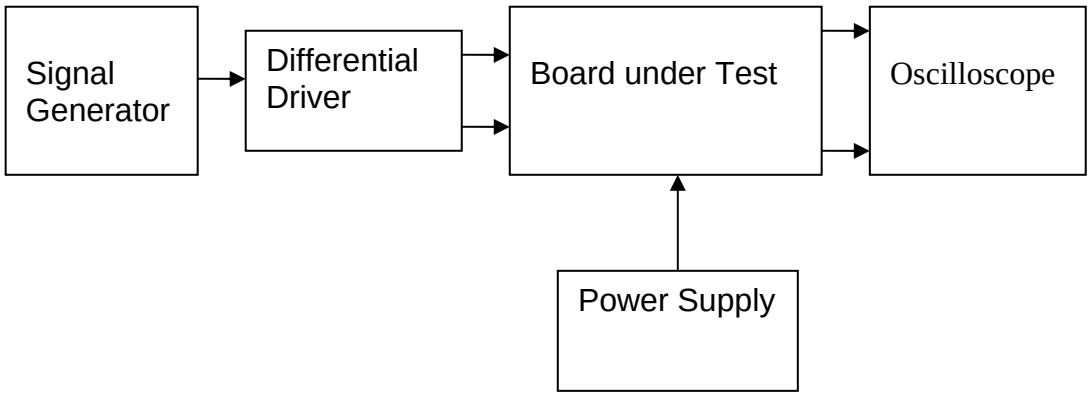
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P19……Serial No ……
Test Engineer …..Xen……
Date ……..26/3/10……..

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.9	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.5	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-29.0	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.6	-21dB	-18dB	√

Unit……T_ACQ_P19……Serial No ……
Test Engineer …..Xen……
Date ……..26/3/10……..

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.5	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P19….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

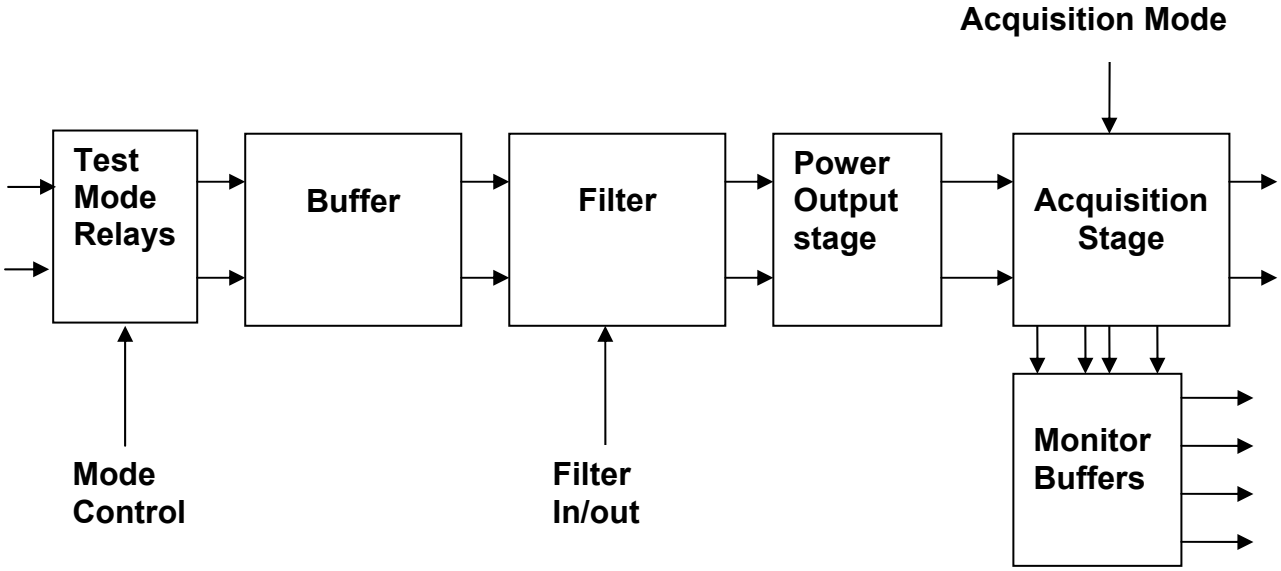
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

J4 slightly lifted off the board.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

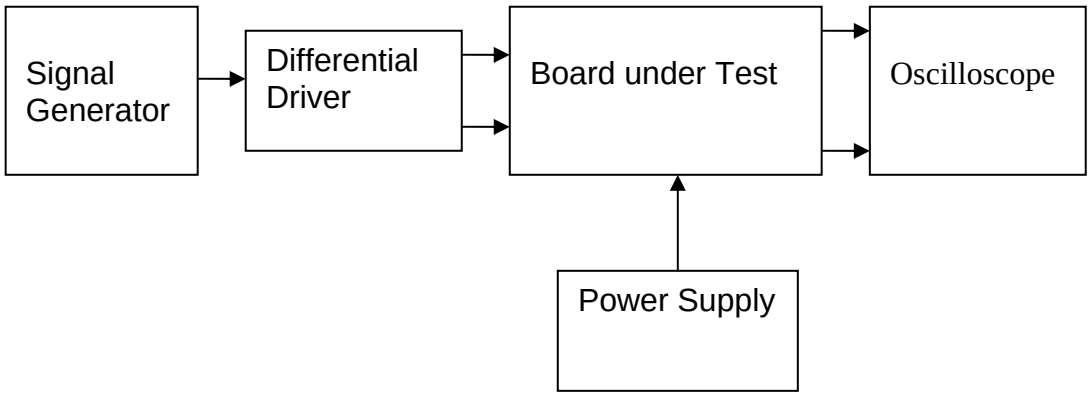
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-14.89V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit……T_ACQ_P20….Serial No ……
Test Engineer…Xen……
Date……29/3/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26.0	-40dB/25mV	-36dB/28mV	√
Ch2	26.0	-40dB/25mV	-36dB/28mV	√
Ch3	26.0	-40dB/25mV	-36dB/28mV	√
Ch4	26.0	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit……T_ACQ_P20….Serial No ……
Test Engineer…Xen……
Date……29/3/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2, or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P20….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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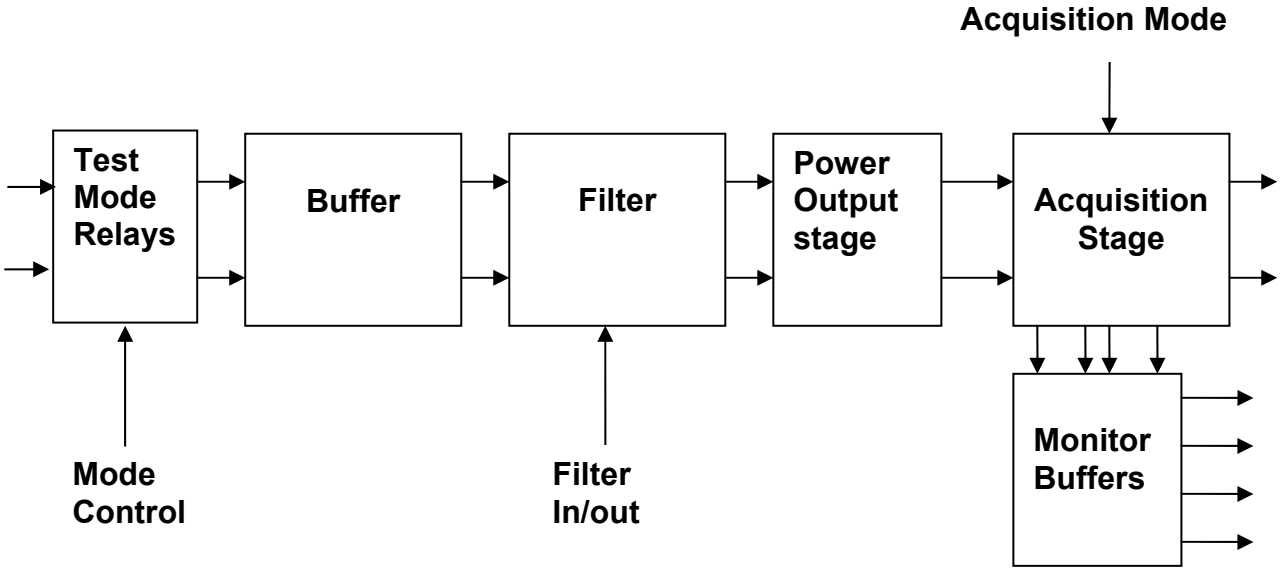
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

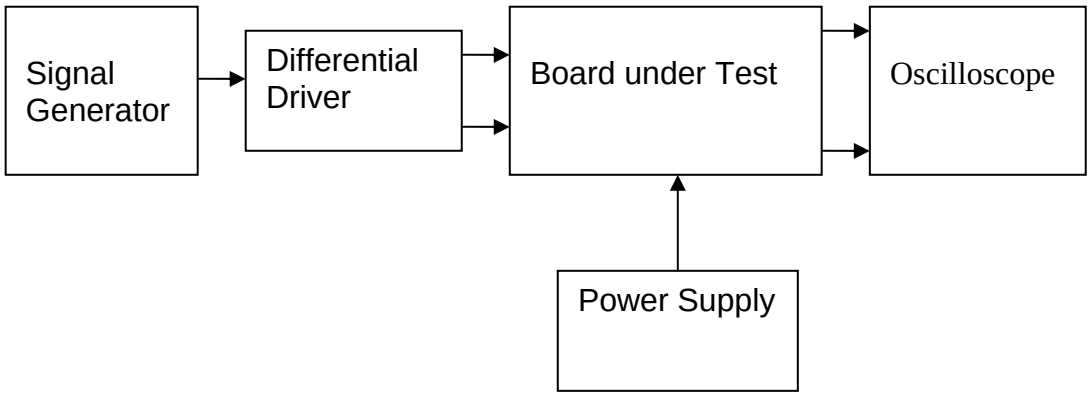
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	25mV	-40dB/25mV	-36dB/28mV	√
Ch2	25mV	-40dB/25mV	-36dB/28mV	√
Ch3	25mV	-40dB/25mV	-36dB/28mV	√
Ch4	25mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P21….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

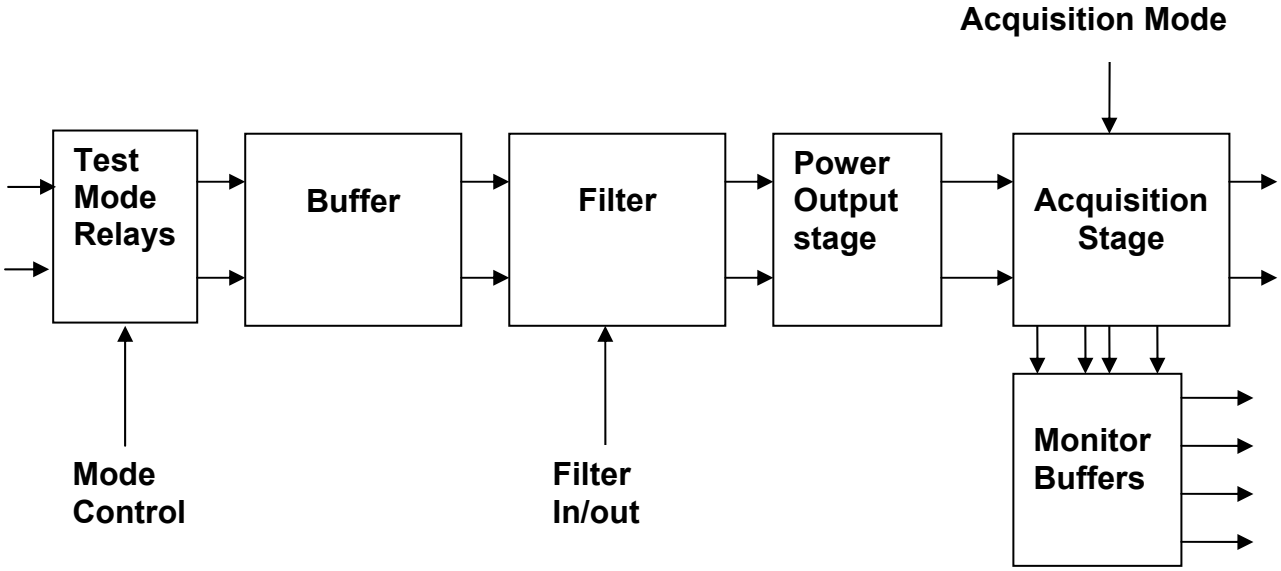
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Board is slightly bowed.

IC6 channel 1 alignment is poor.

IC6 and IC3 channel 3 alignment is poor.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

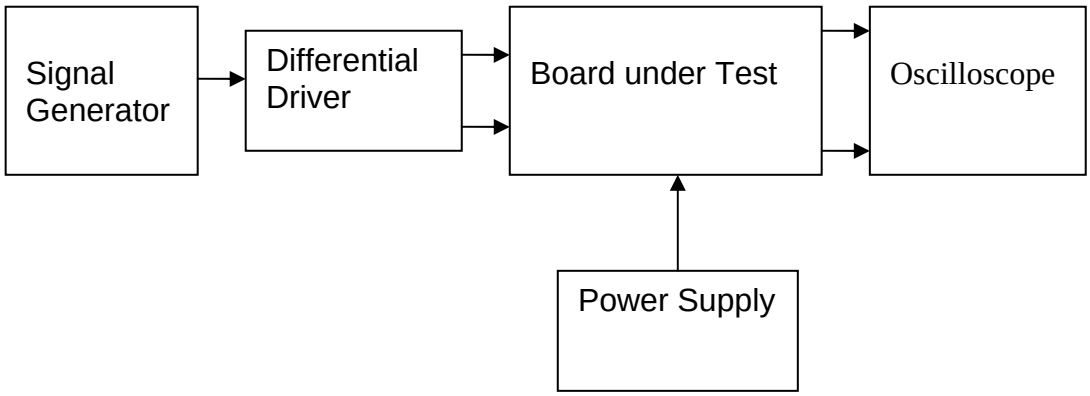
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	14.88V	√	1mV
-15v TP6	-15.04V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P22….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

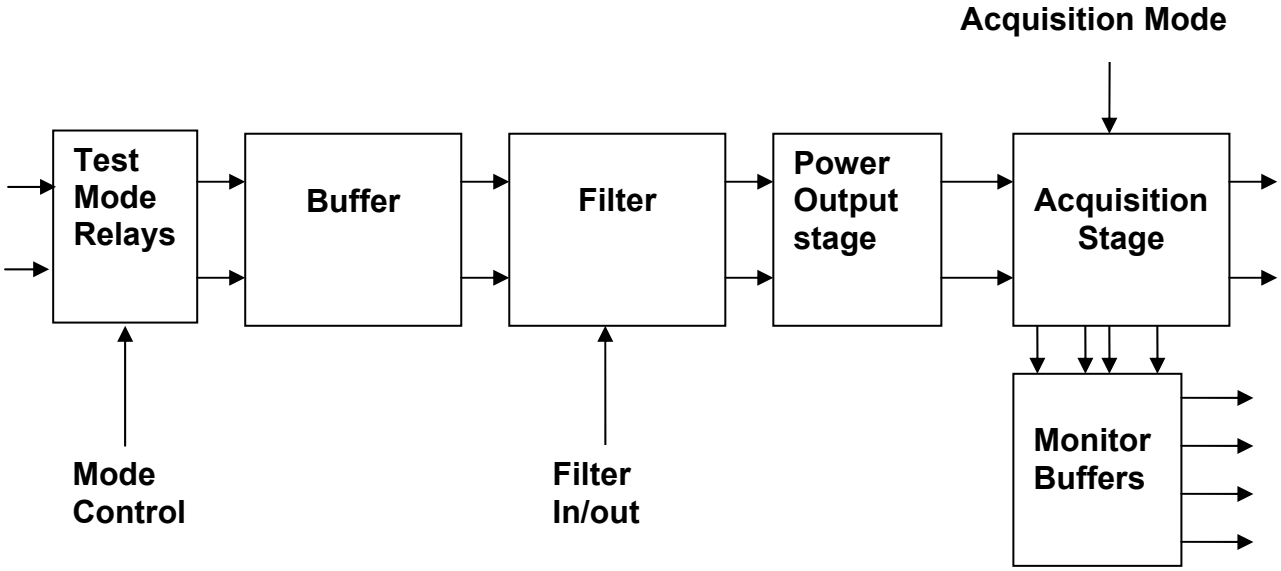
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

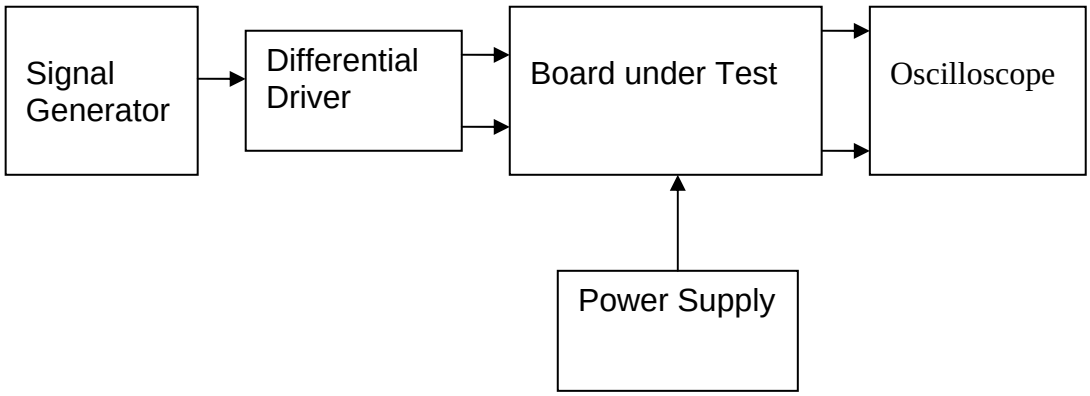
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.12V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	15.01V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P23….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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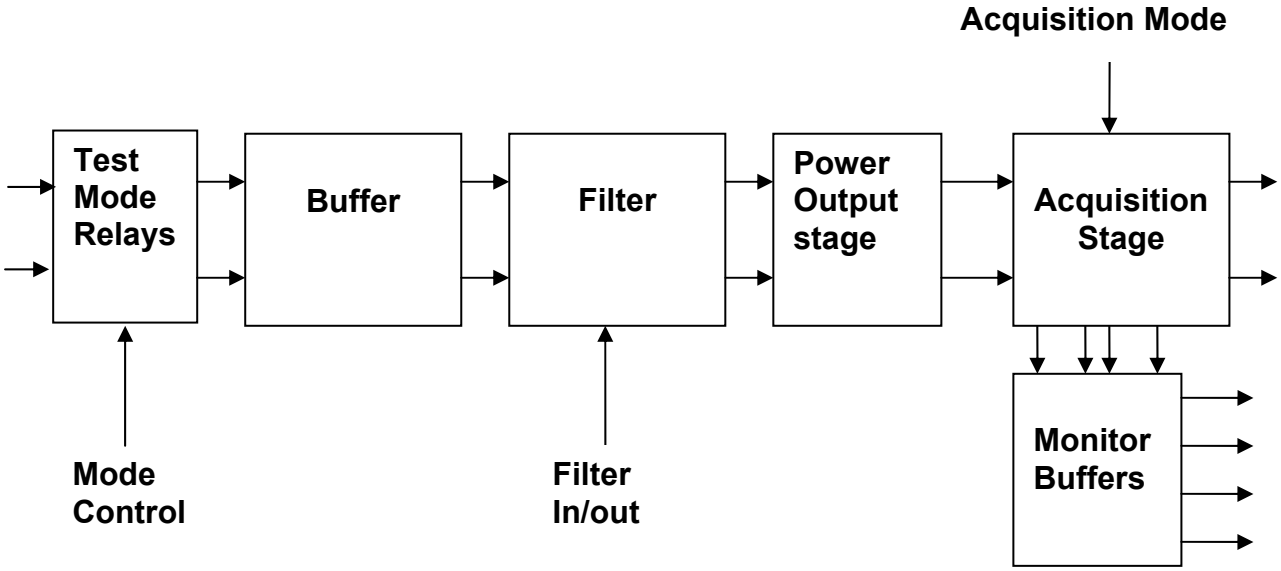
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

2. Test equipment
Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10…….

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

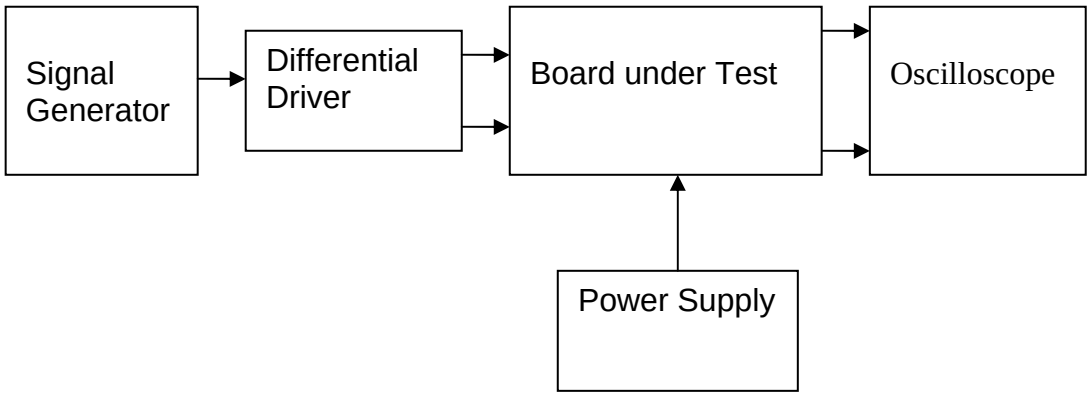
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	11.99V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.93V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

7. Relay Operation

Note: 37 way to 25 way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.

With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.

Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filters and test the response using the signal generator. Measure the frequency response of each channel using the dynamic signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-29.1	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 KHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …05/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on for each channel. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	

1 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	

5 KHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1KHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P24….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/03/10……..

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

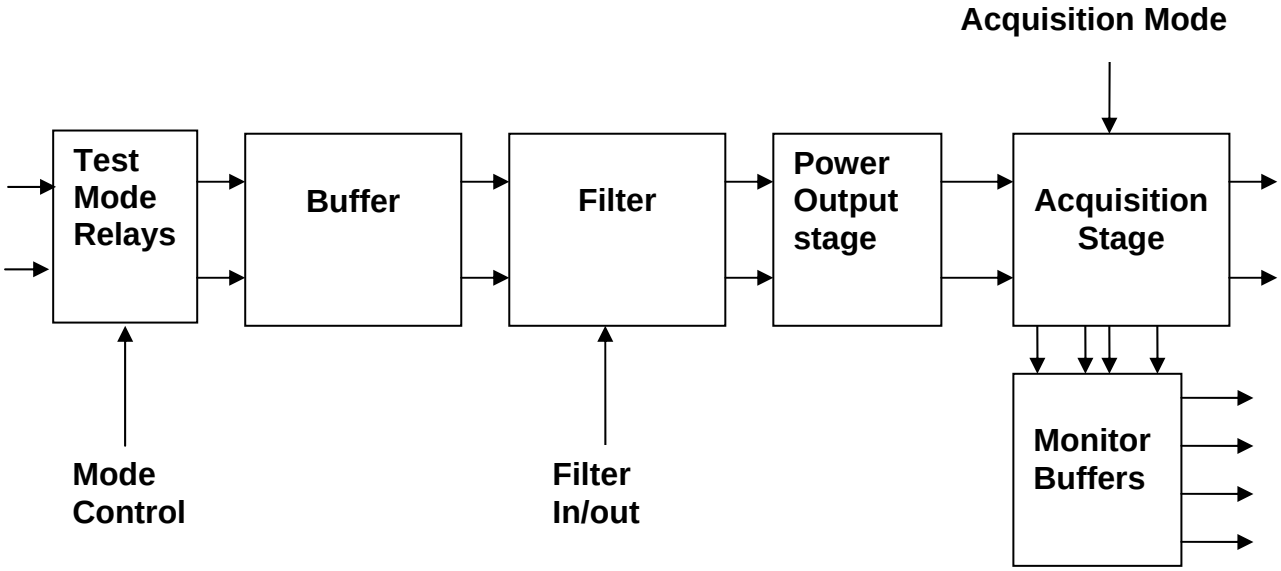
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

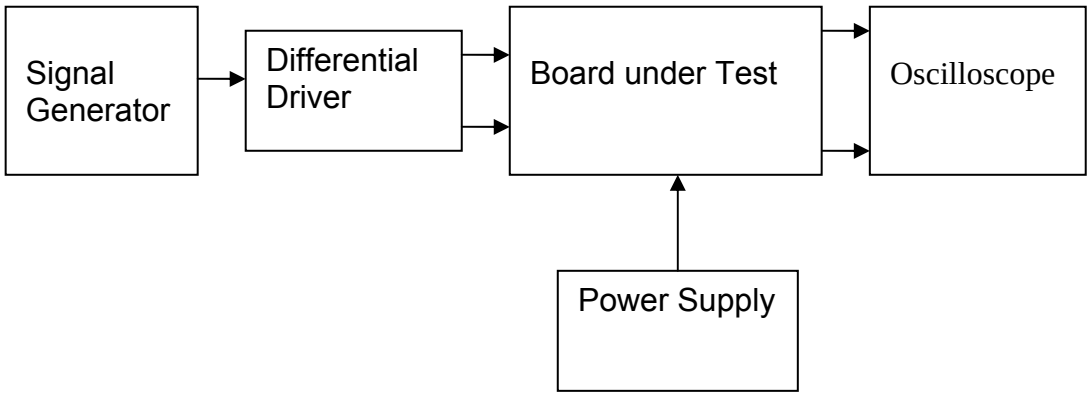
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.00V	√	1mV
+15v TP4	14.82V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.3	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-50.7	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-29.1	-30dB	-27dB	√
Ch3	-29.2	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P25….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

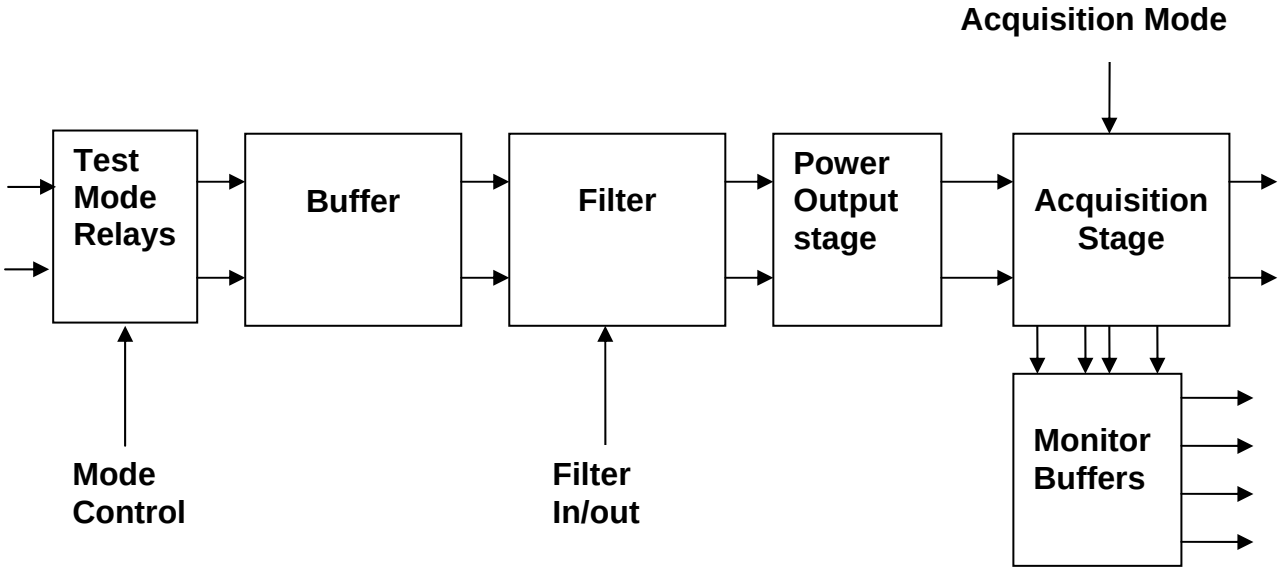
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

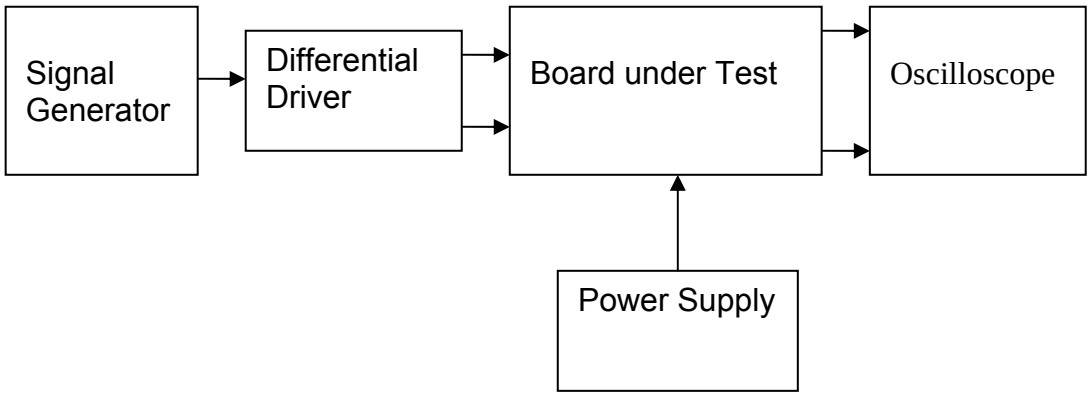
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P26….Serial No ……
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Date …12/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.95V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …12/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	25mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.4	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.4	-53dB	-50dB	√
Ch4	-50.9	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P26….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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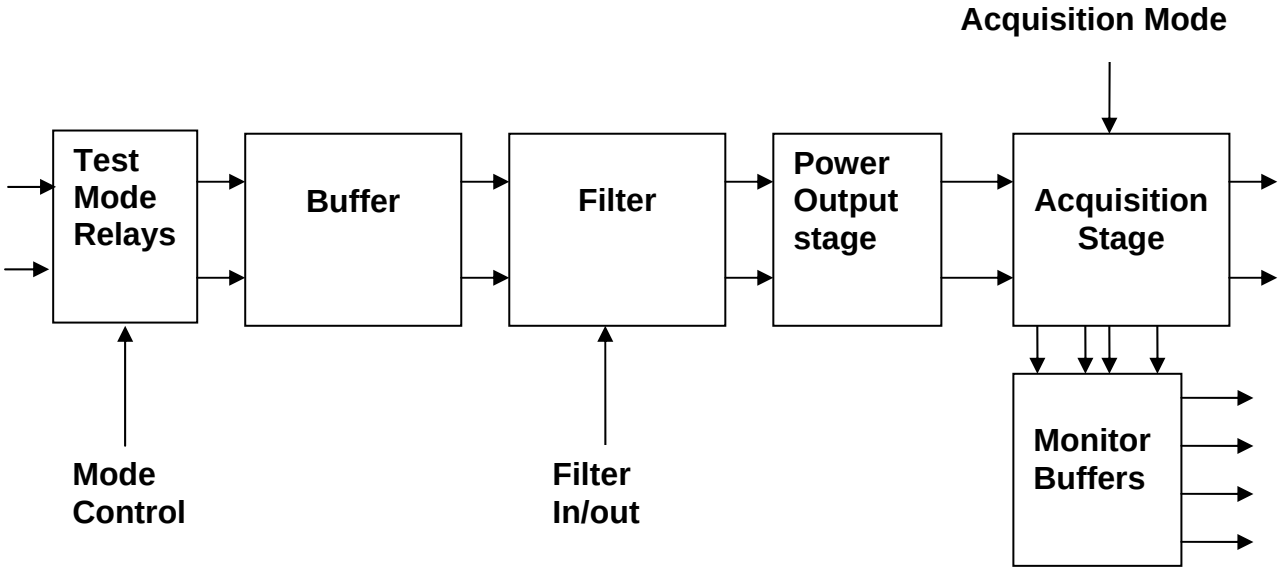
Block diagram



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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

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The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

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Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

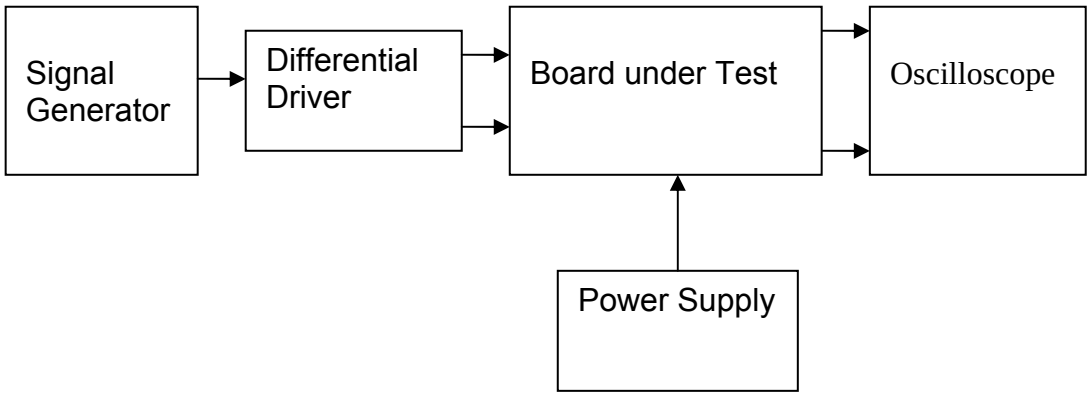
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.90V	√	1mV
-15v TP6	-14.95V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P27….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

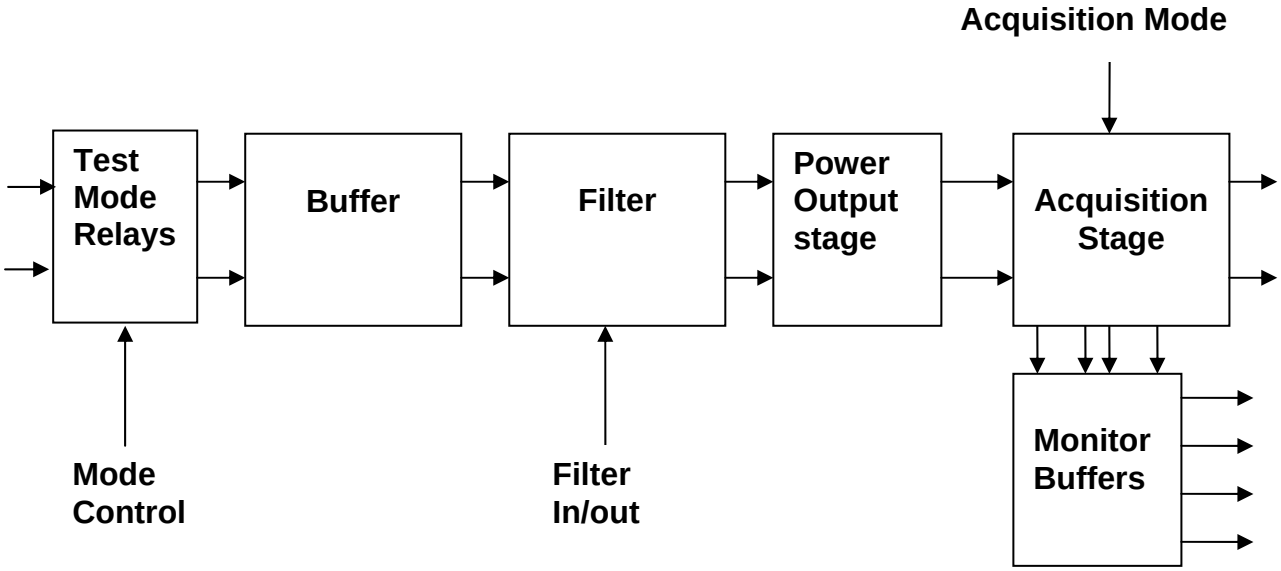
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……..T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……..…
Date …….6/10/10……..……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit……..T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……..…
Date …….6/10/10……..……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Replaced the relay K4 on CH4.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

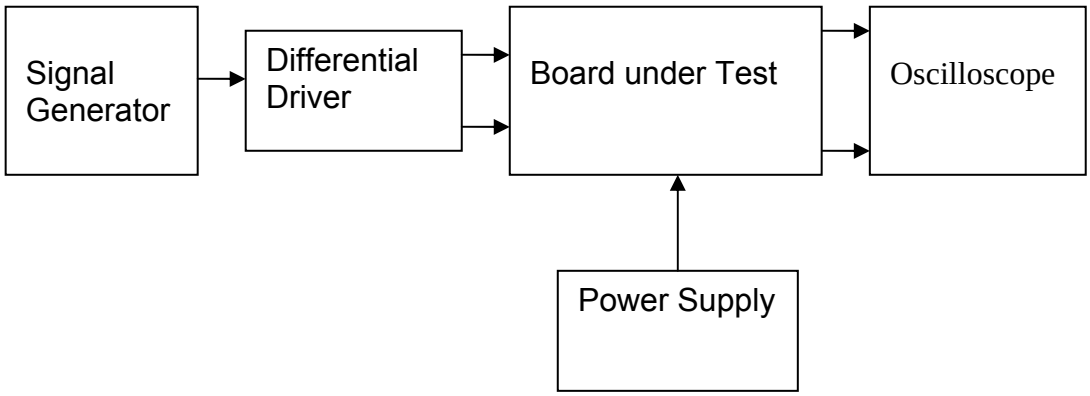
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.98V	√	1mV
-15v TP6	-14.94V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.20V	Pin 1 to Pin 2	2.20V	√
2	2.20V	Pin 5 to Pin 6	2.20V	√
3	2.20V	Pin 9 to Pin 10	2.20V	√
4	2.20V	Pin 13 to Pin 14	2.20V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……..T_ACQ_P28….Serial No ……
Test Engineer ……Xen……..……
Date ……6/10/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …13/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P28….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22.5V	√	-22.5V	√	-22.5V	√	-22.5V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	-22.5	√	22.5V	√	22.5V	√	22.5V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

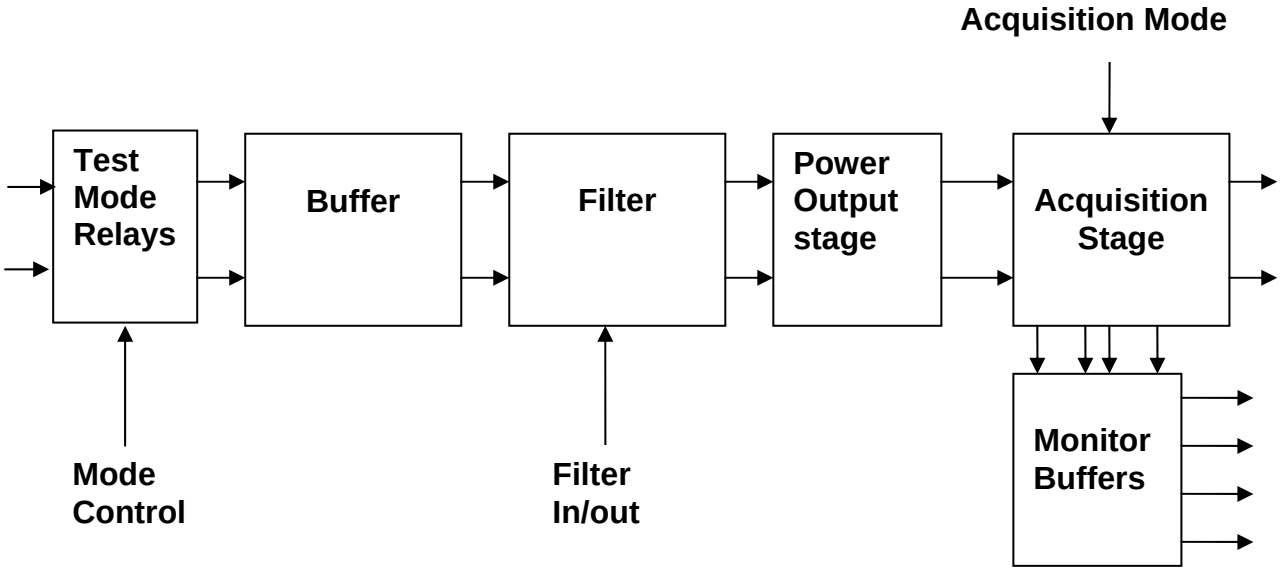
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

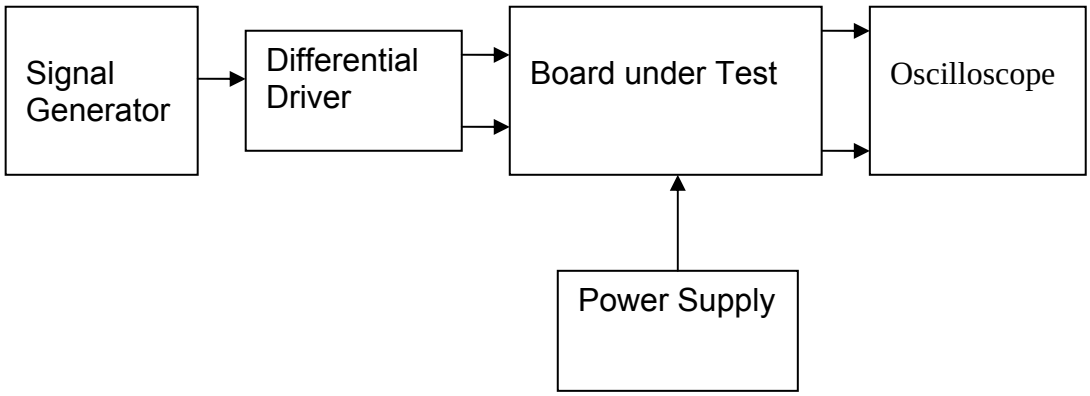
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.00V	√	1mV
+15v TP4	14.87V	√	1mV
-15v TP6	15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.0	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P29….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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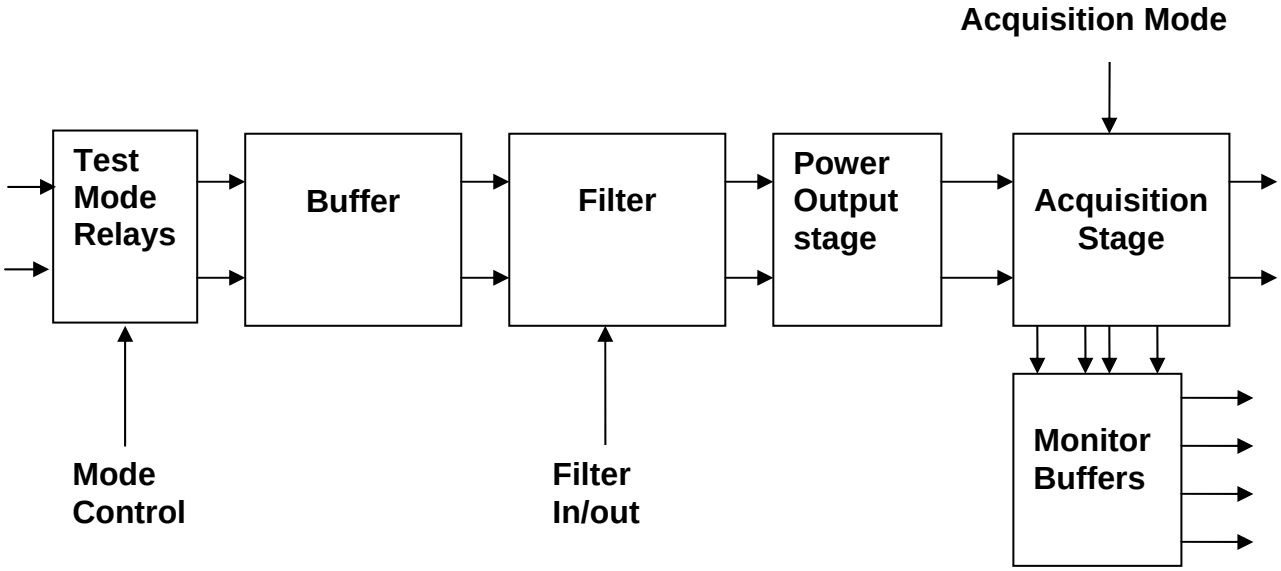
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
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Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

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Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

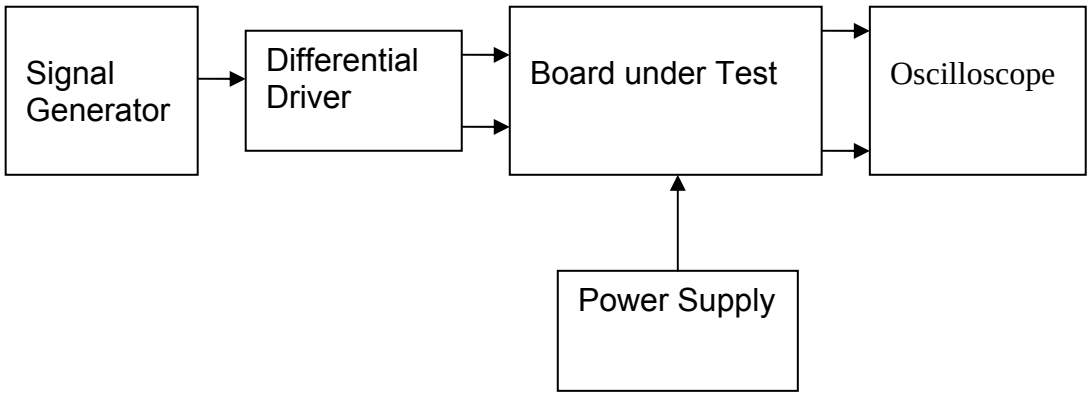
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.90V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.0	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …17/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P30….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

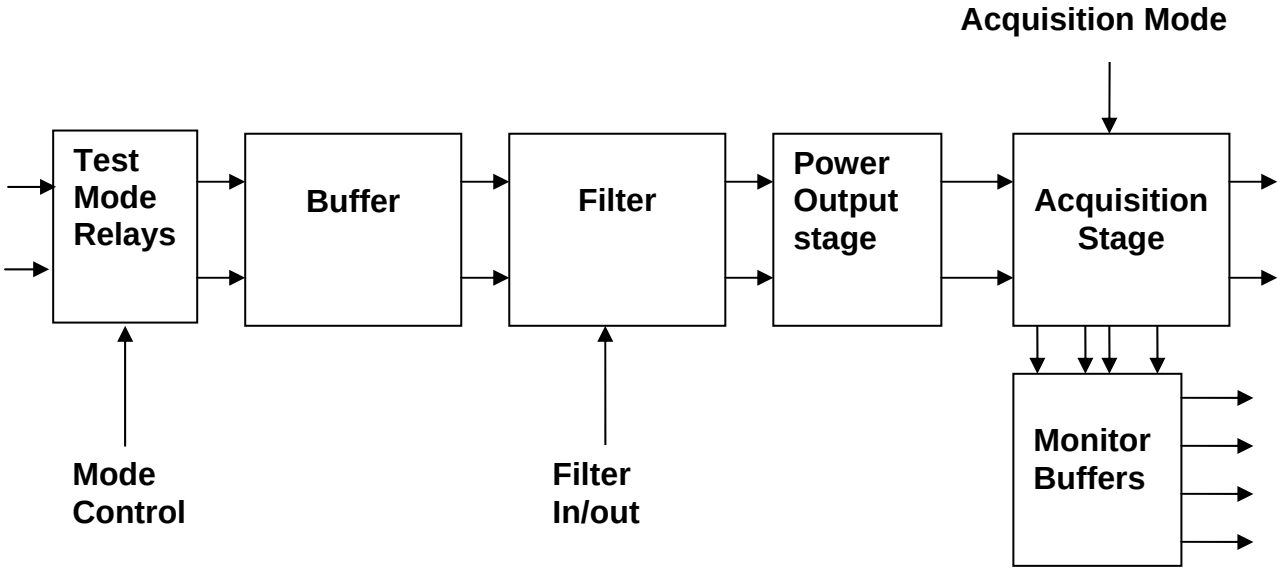
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P31….Serial No ……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

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Date …15/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

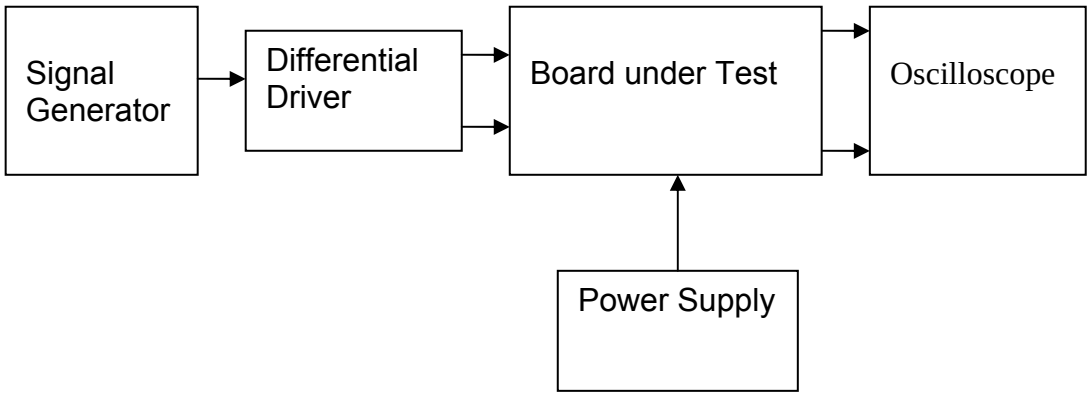
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P31….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.01V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.07V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-29.3	-30dB	-27dB	√
Ch3	-29.1	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P31….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

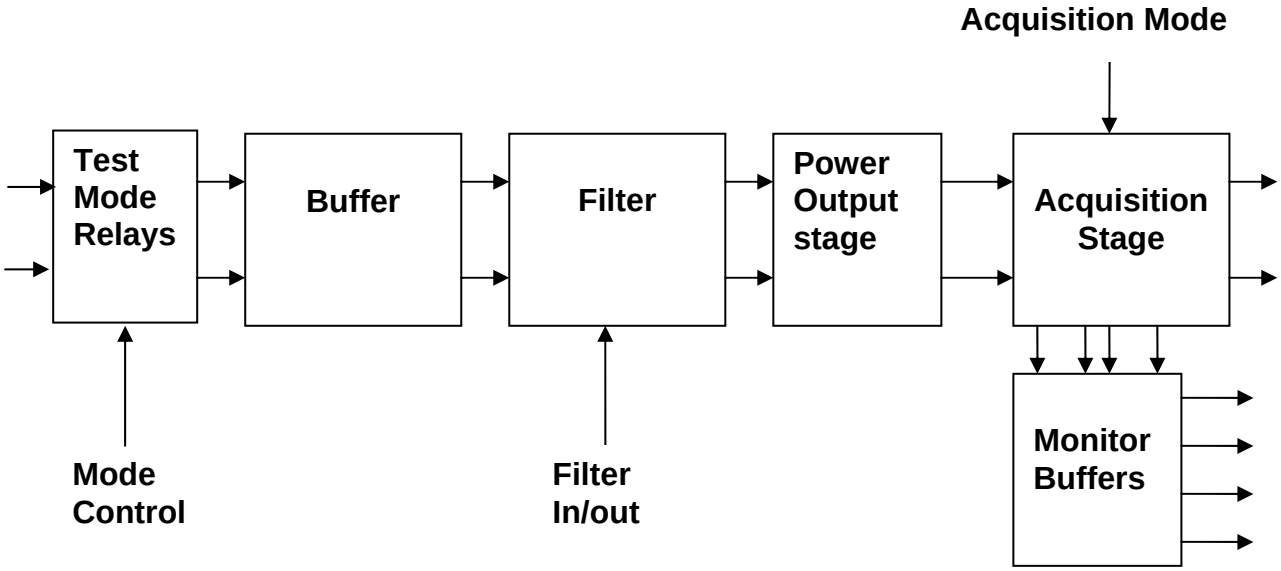
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

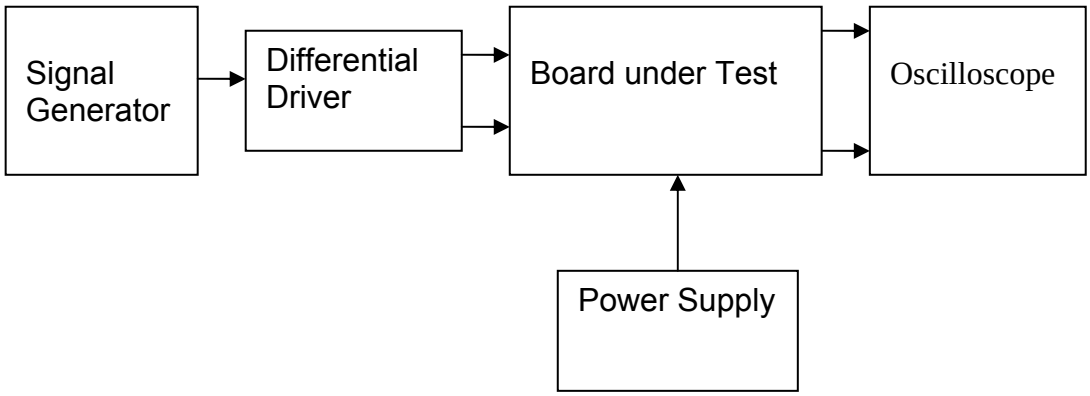
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-14.99V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P32….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P33….Serial No ……
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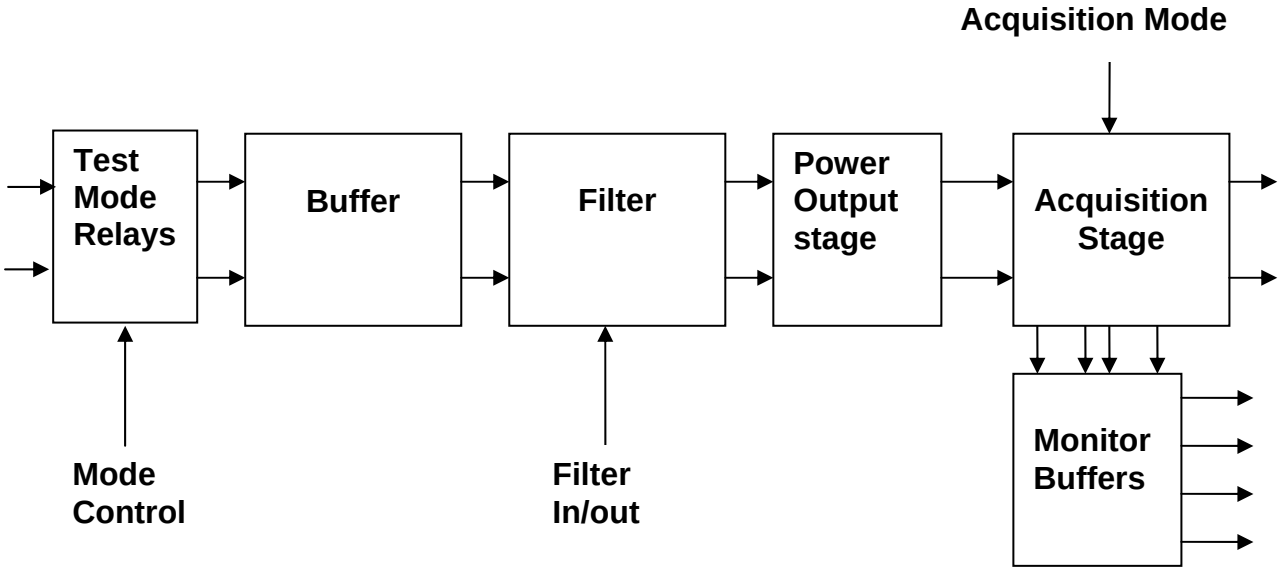
Block diagram



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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

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The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

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Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

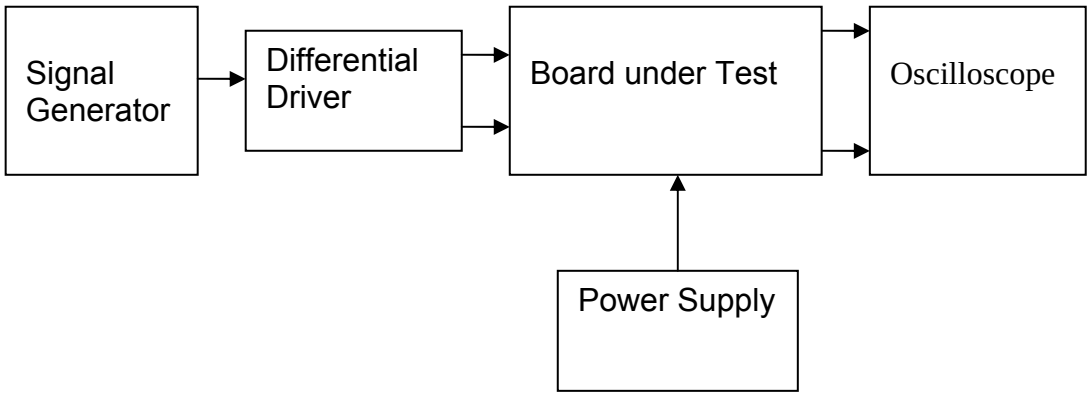
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-29.0	-30dB	-27dB	√
Ch3	-29.0	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P33….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

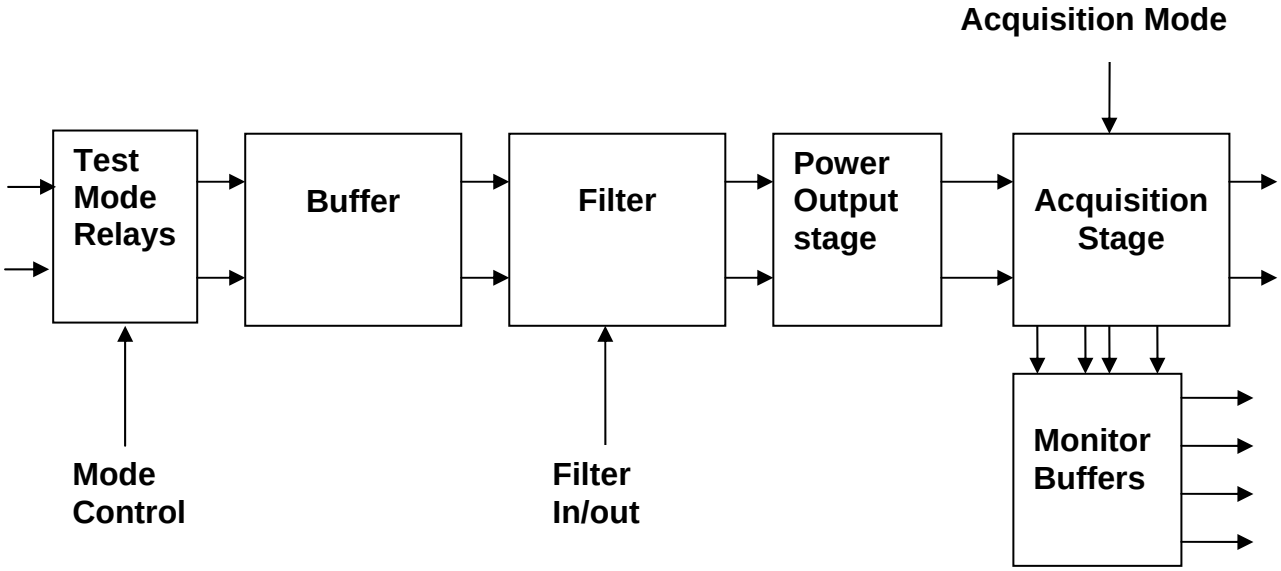
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Small scratches on board around Ch 3 area.

DS1 and DS2 positioning poor.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

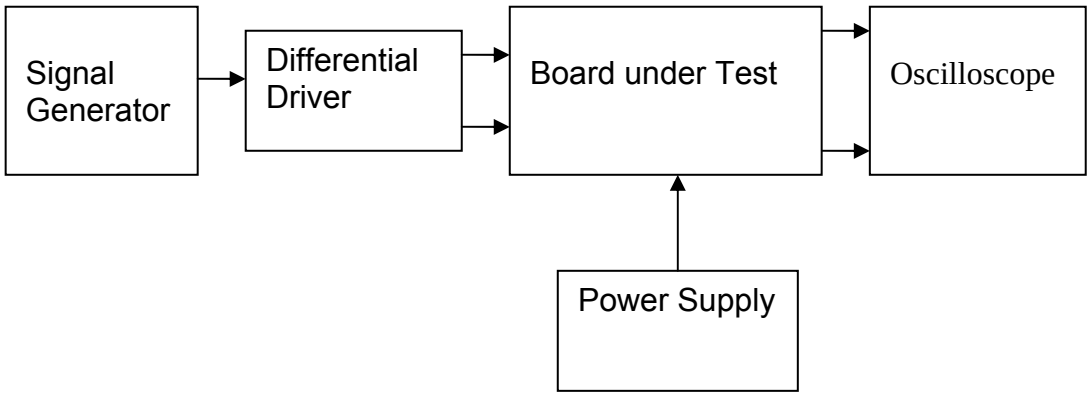
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.76V	√	1mV
-15v TP6	-15.00V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.2	-30dB	-27dB	√
Ch2	-29.2	-30dB	-27dB	√
Ch3	-29.4	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P34….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

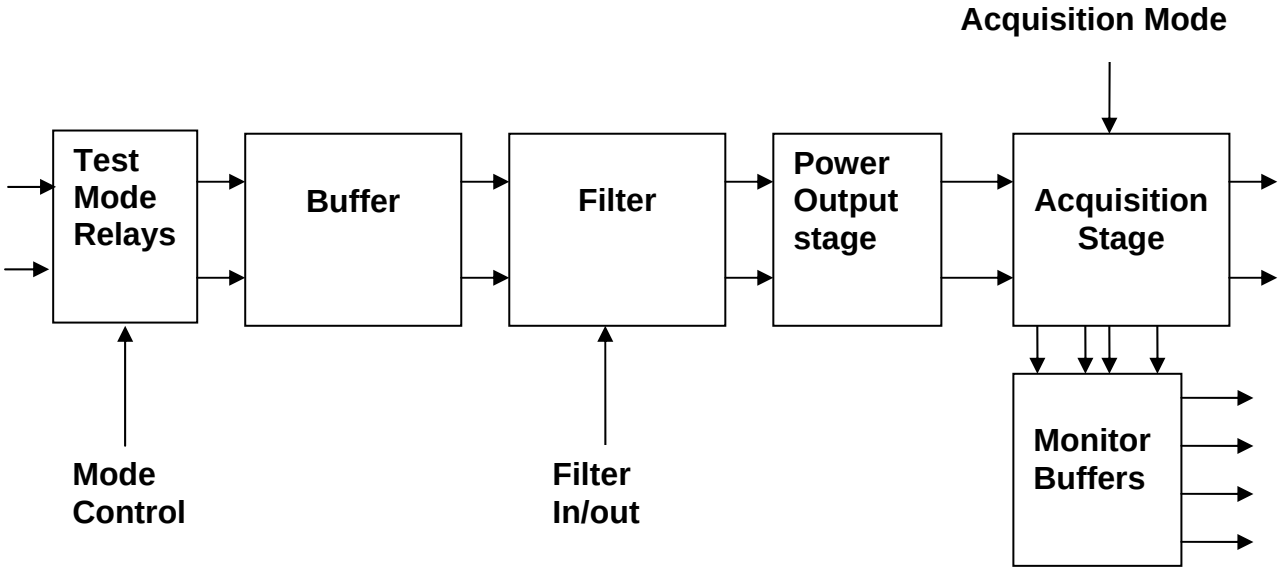
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is very bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

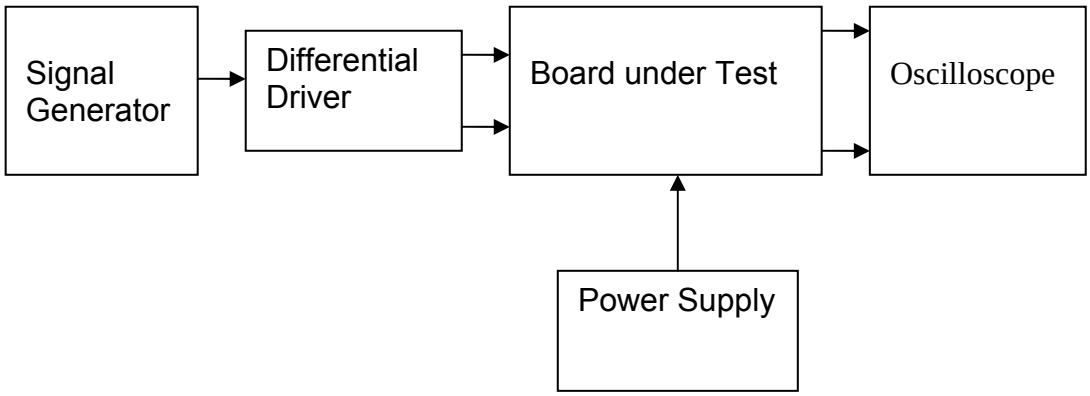
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.2	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P35….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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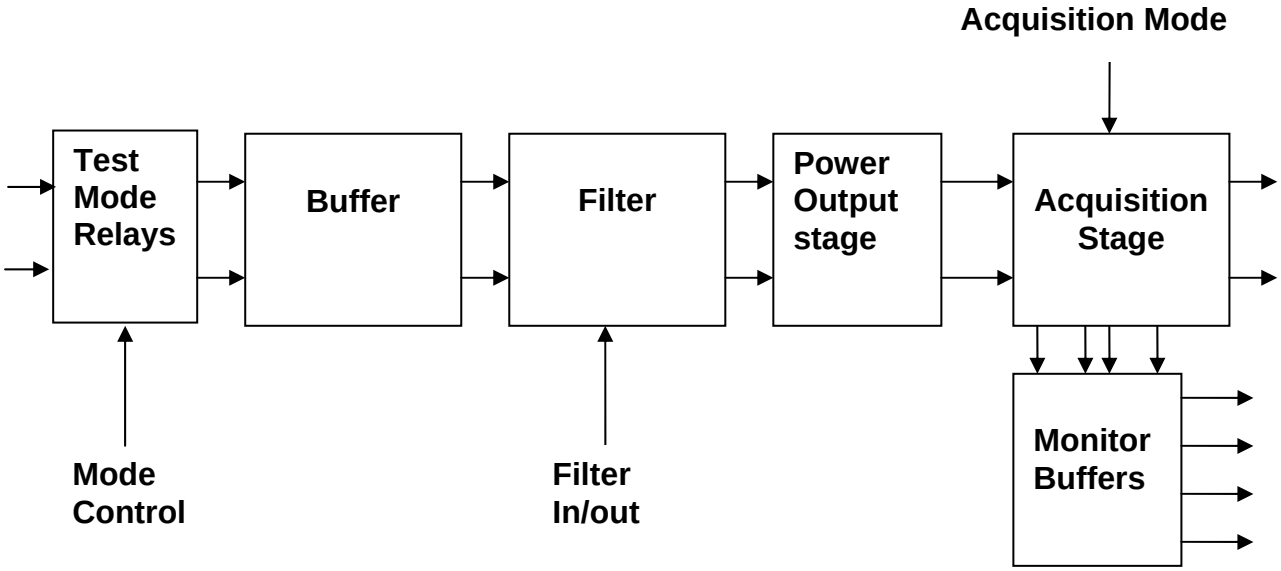
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

Contents

Block diagram



1. Description

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The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
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The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

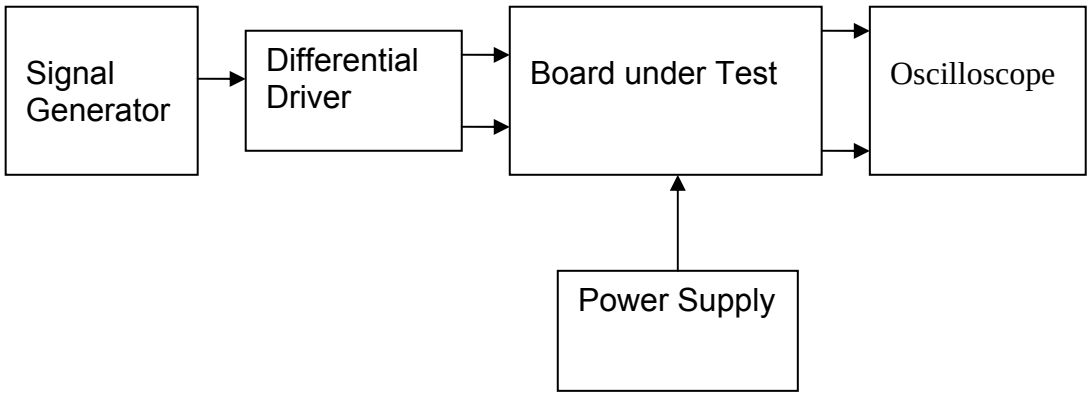
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

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Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	-15.09V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P36….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

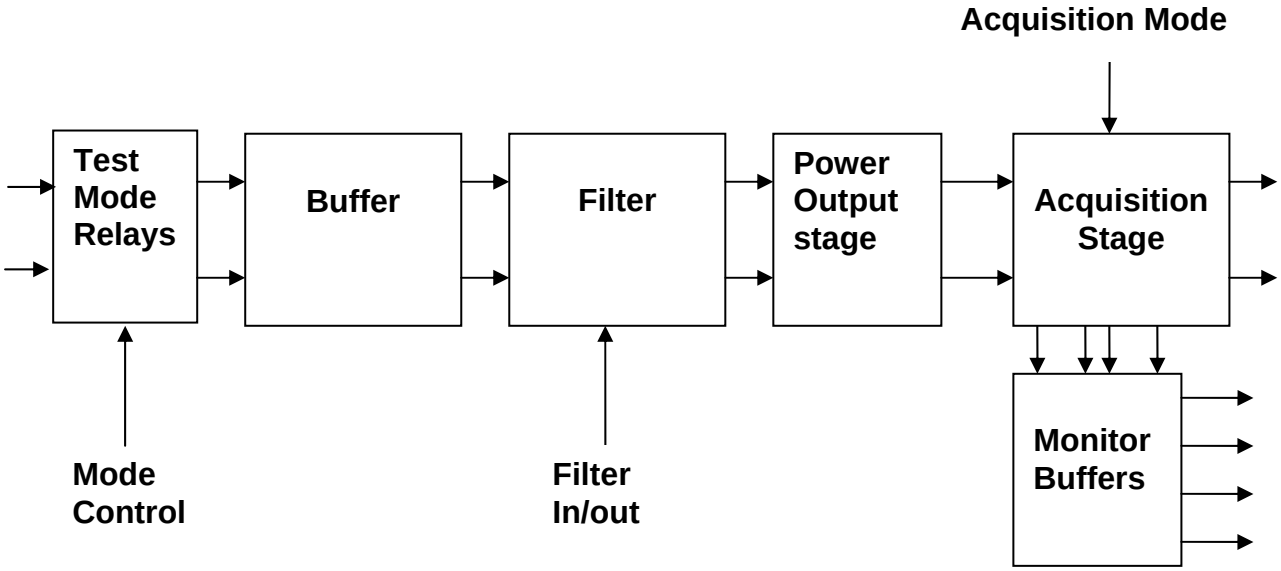
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

IC4 Channel 2 was replaced. Original was mounted upside down.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

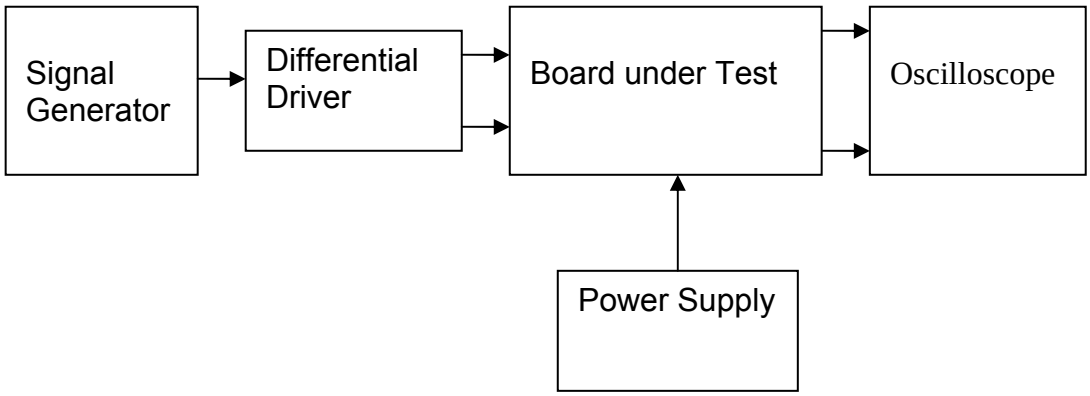
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.92V	√	1mV
-15v TP6	-14.95V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.0	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …18/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P37….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

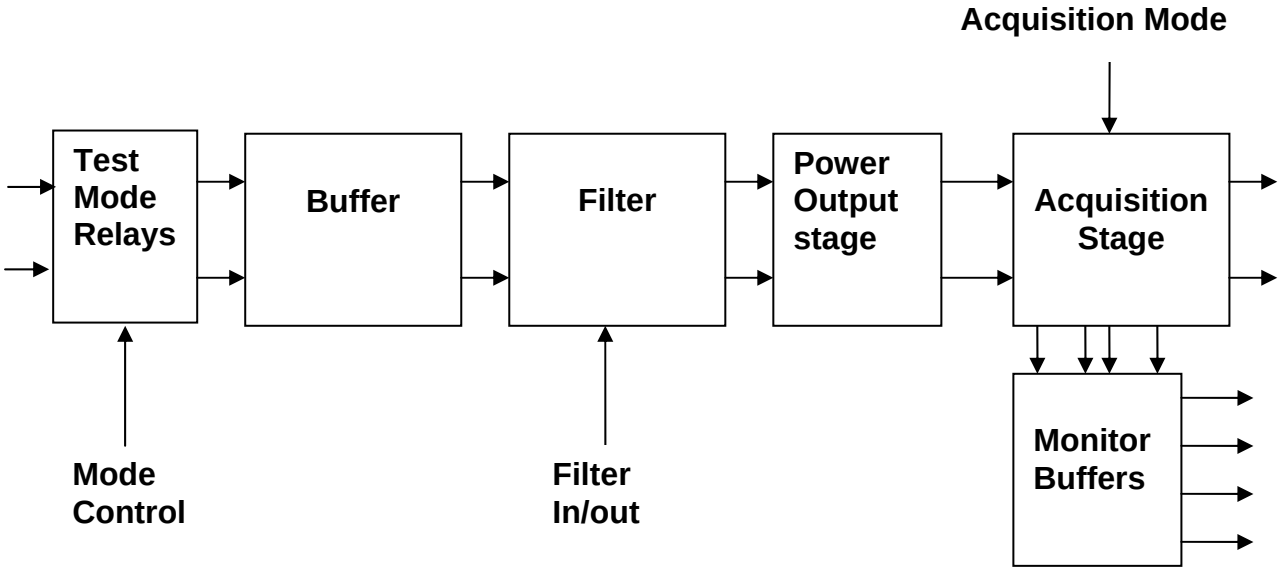
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

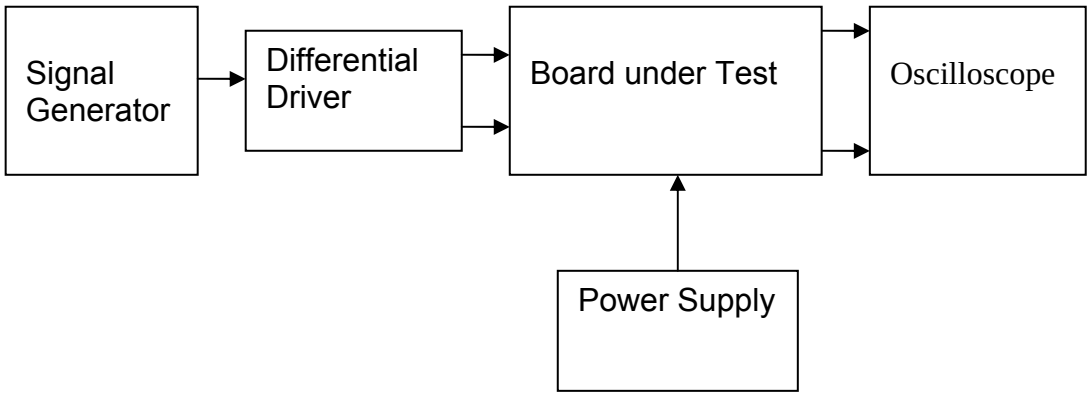
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	14.81V	√	1mV
-15v TP6	-15.08V	√	1mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P38….Serial No ……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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Date …18/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.2	-30dB	-27dB	√
Ch2	-29.2	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-29.2	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P38….Serial No ……
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Date …18/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P38….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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http://www.ligo.caltech.edu/

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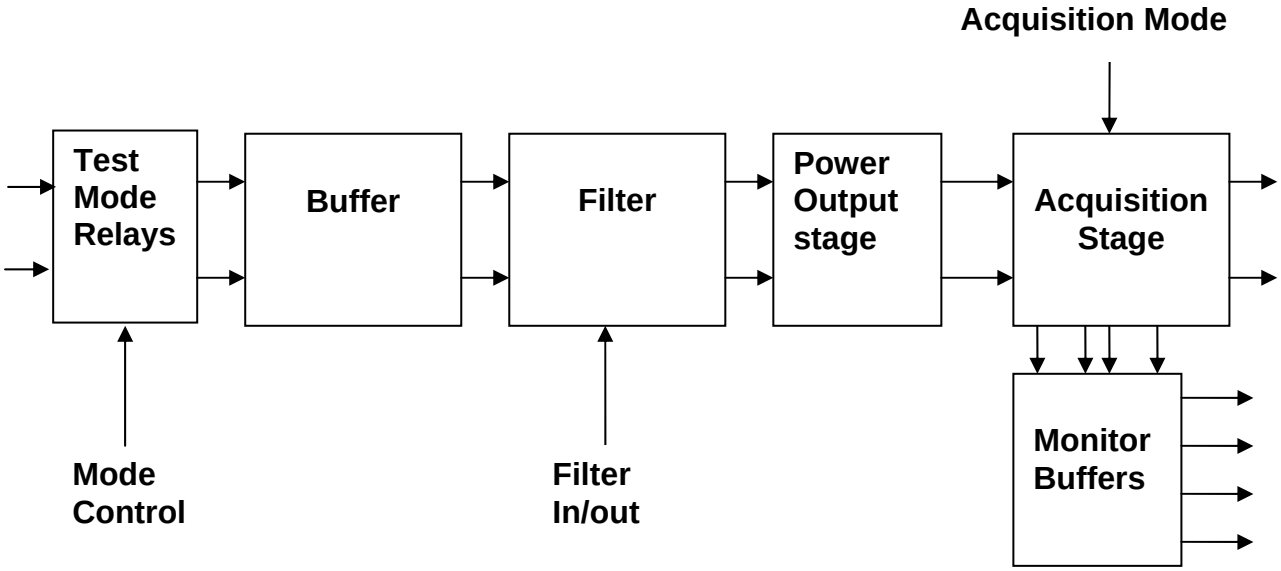

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
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The filter may be switched in and out by command as required under relay control.

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The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
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Relay test box

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Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

J7 slightly lifted off the board.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

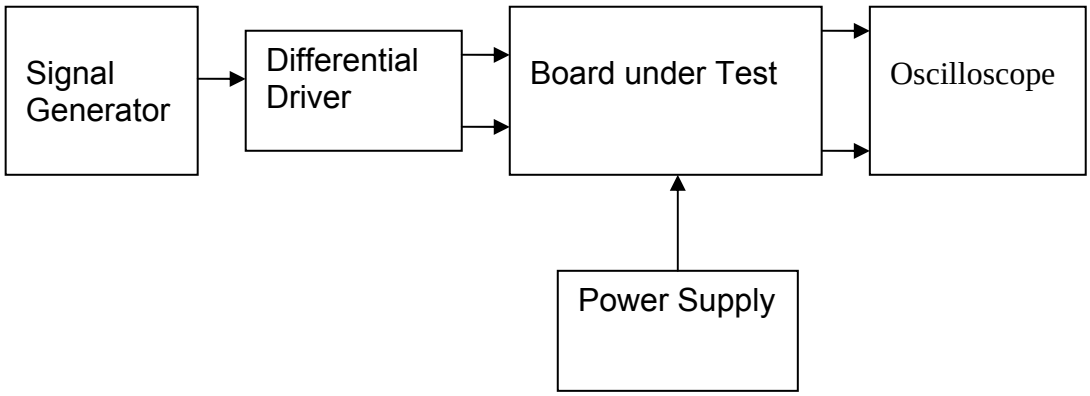
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P39….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.82V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P39….Serial No ……
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Date …26/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-29.1	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P39….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

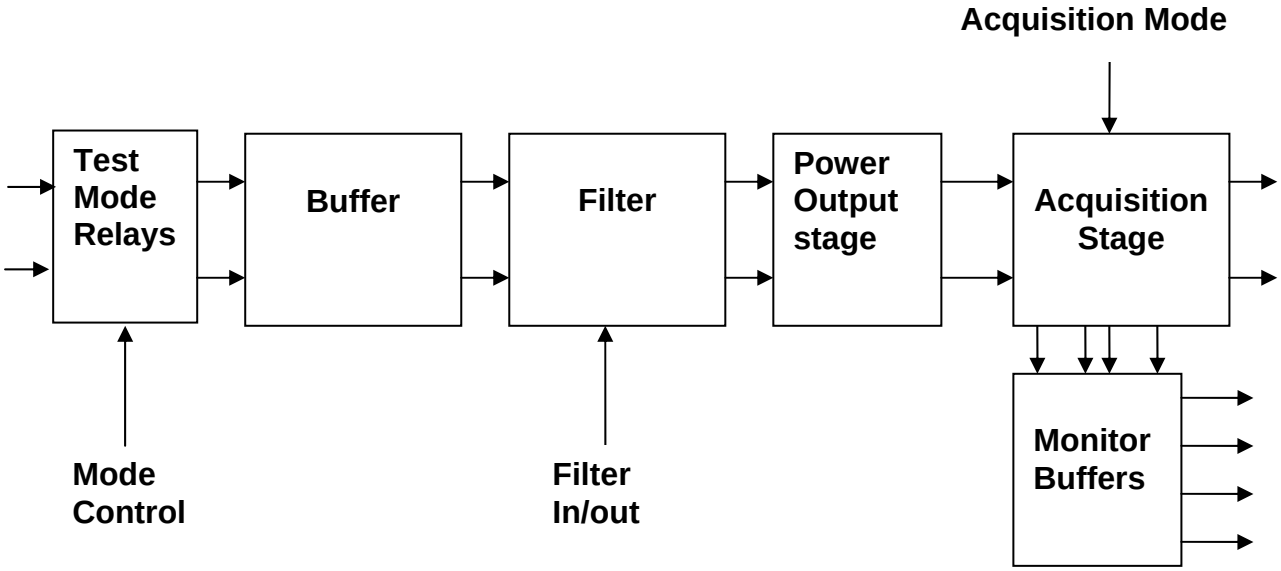
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P40….Serial No ……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

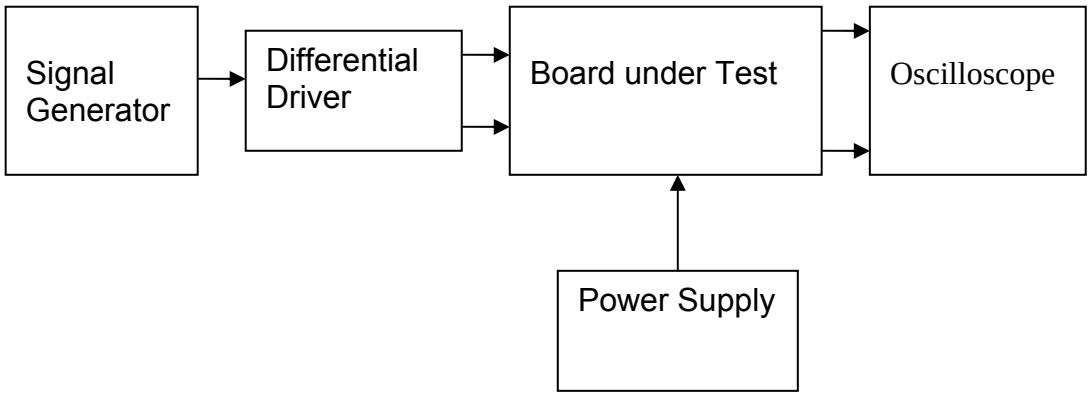
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P40….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.09V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-14.88V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P40….Serial No ……
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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.0	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.5	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P40….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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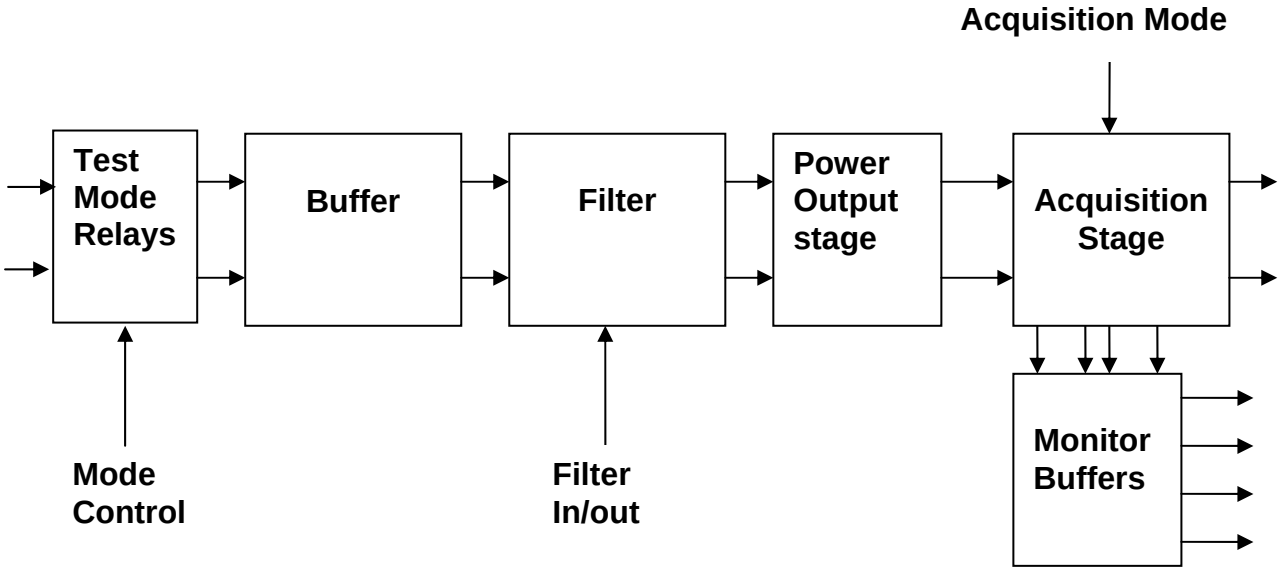
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P41….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P41….Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

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Date …26/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P41….Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

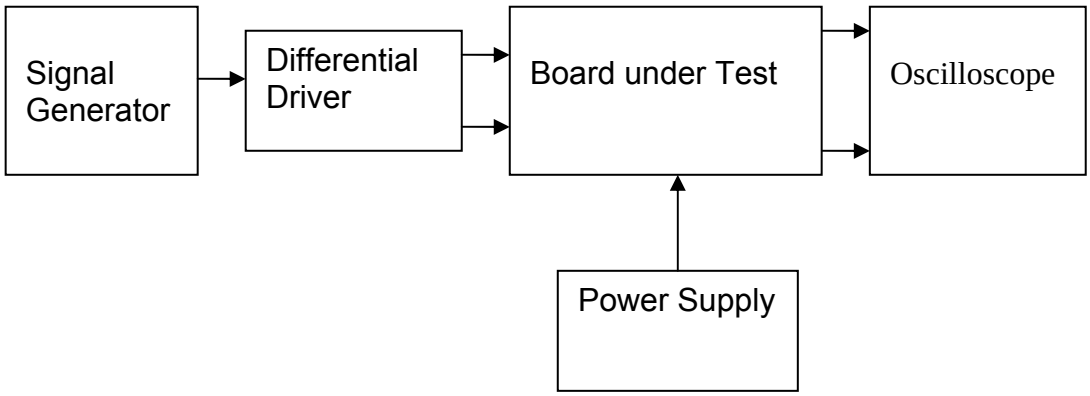
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P41….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.00V	√	1mV
+15v TP4	14.92V	√	1mV
-15v TP6	-14.93V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P41….Serial No ……
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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P41….Serial No ……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.8	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P41….Serial No ……
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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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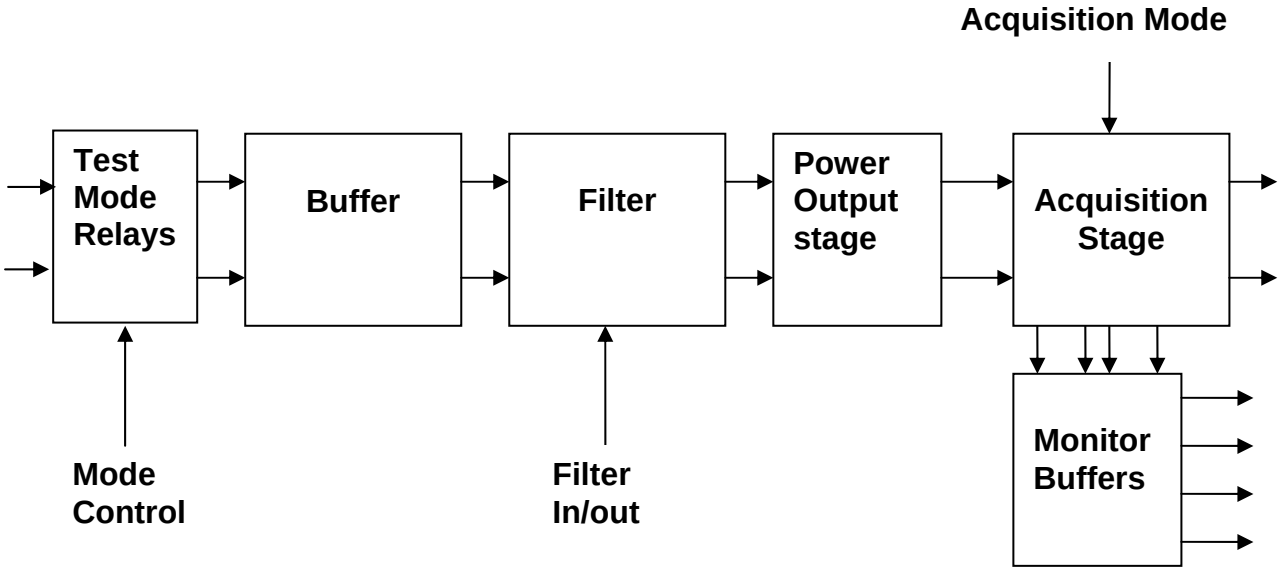
Block diagram



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Relay test box

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Relay test box	N/A	N/A	N/A
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

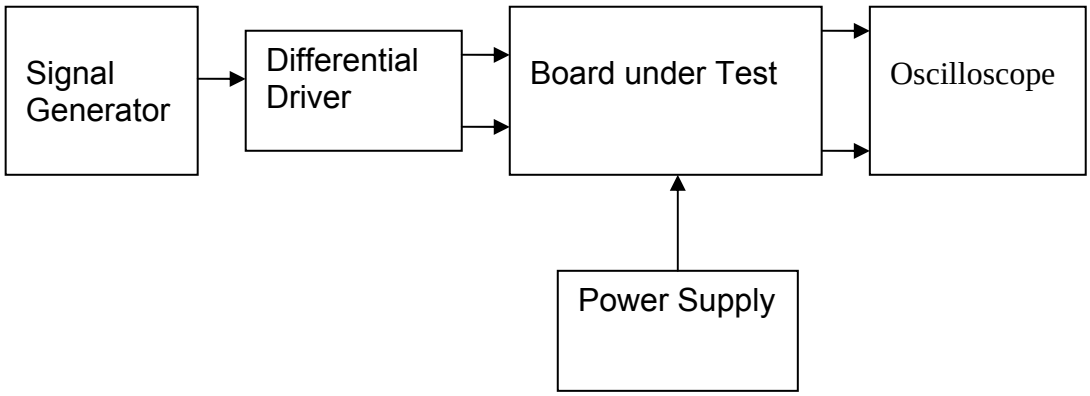
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

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Differential signal inputs to the board under test:
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J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-14.93V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P42….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.20V	Pin 1 to Pin 2	2.20V	√
2	2.20V	Pin 5 to Pin 6	2.20V	√
3	2.20V	Pin 9 to Pin 10	2.20V	√
4	2.20V	Pin 13 to Pin 14	2.20V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P42….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P42….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P42….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P42….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

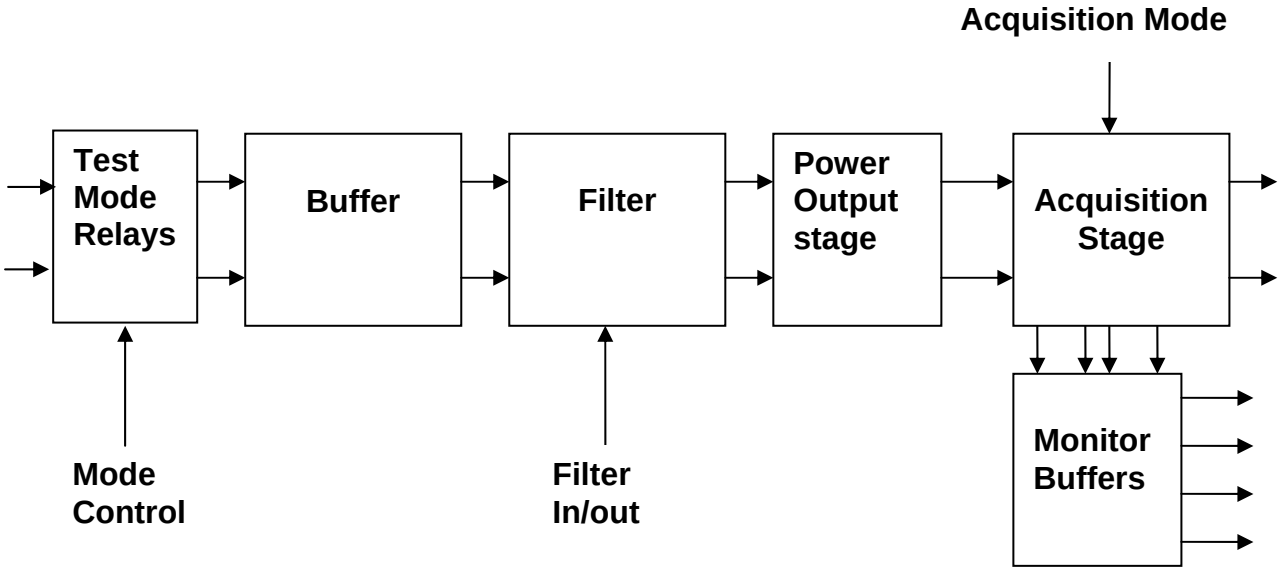
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

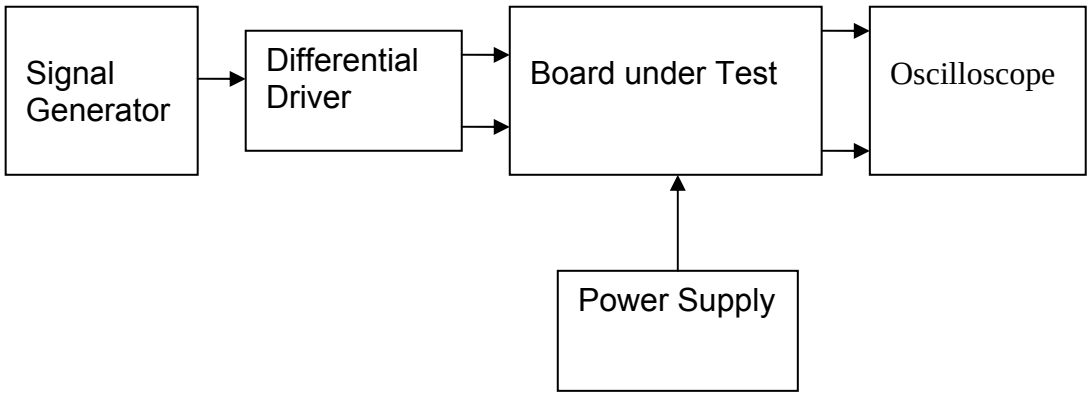
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P43….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-15.04V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P43….Serial No ……
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Date …27/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.8	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P43….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

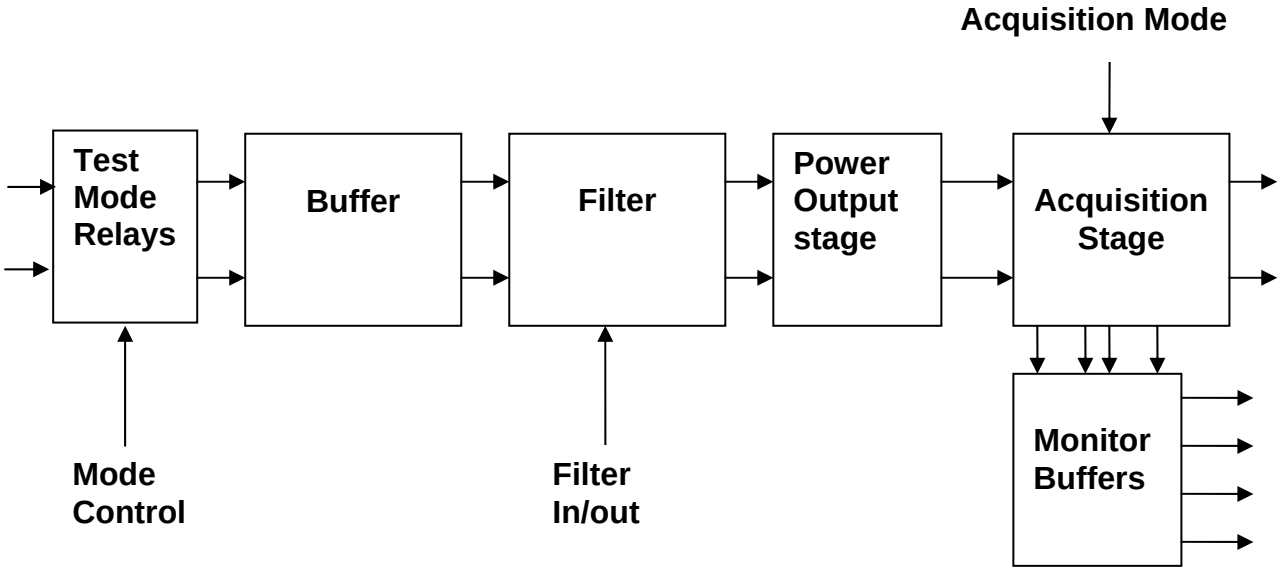
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

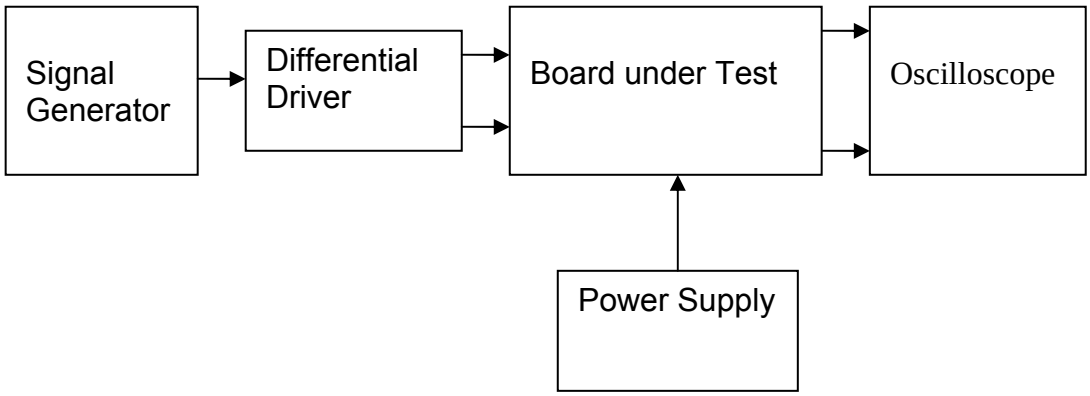
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.86V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P44….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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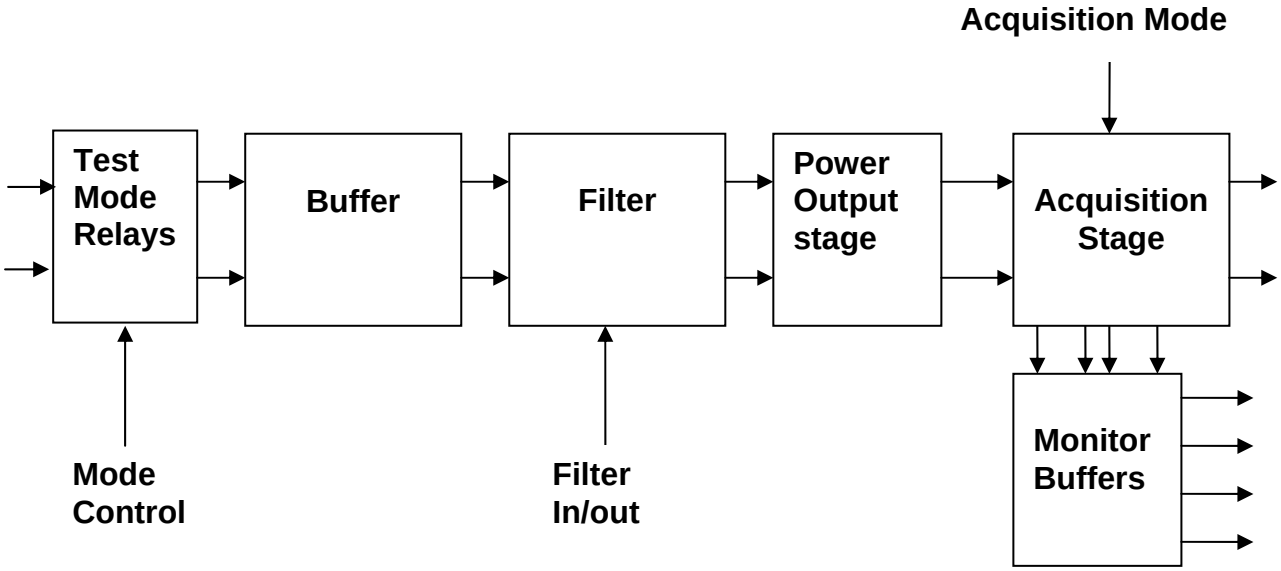
Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P45….Serial No ……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Small solder splash inside the D connector housing on J3. Doesn't appear to cause an access blockage.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

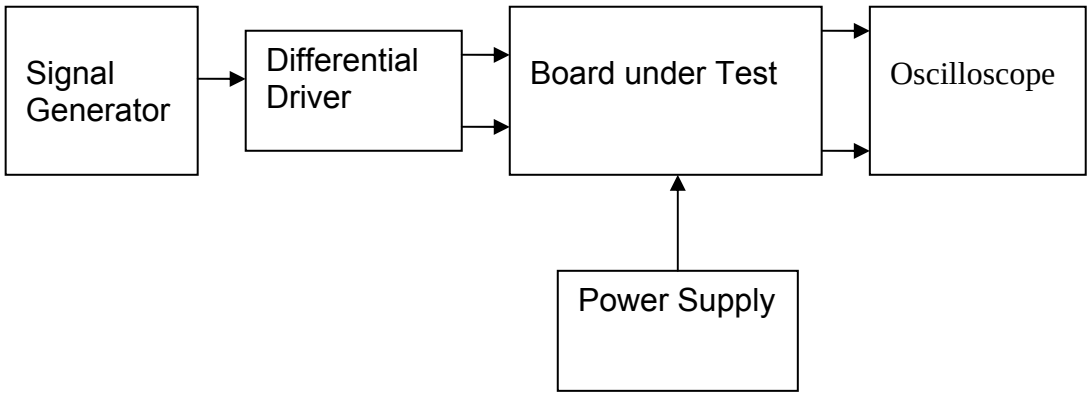
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P45….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	15.00V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P45….Serial No ……
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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.4	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.4	-30dB	-27dB	√
Ch2	-29.0	-30dB	-27dB	√
Ch3	-29.4	-30dB	-27dB	√
Ch4	-29.1	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P45….Serial No ……
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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P45….Serial No ……
Test Engineer …Simon Pyatt……
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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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Test Engineer …Simon Pyatt……
Date …28/04/10……

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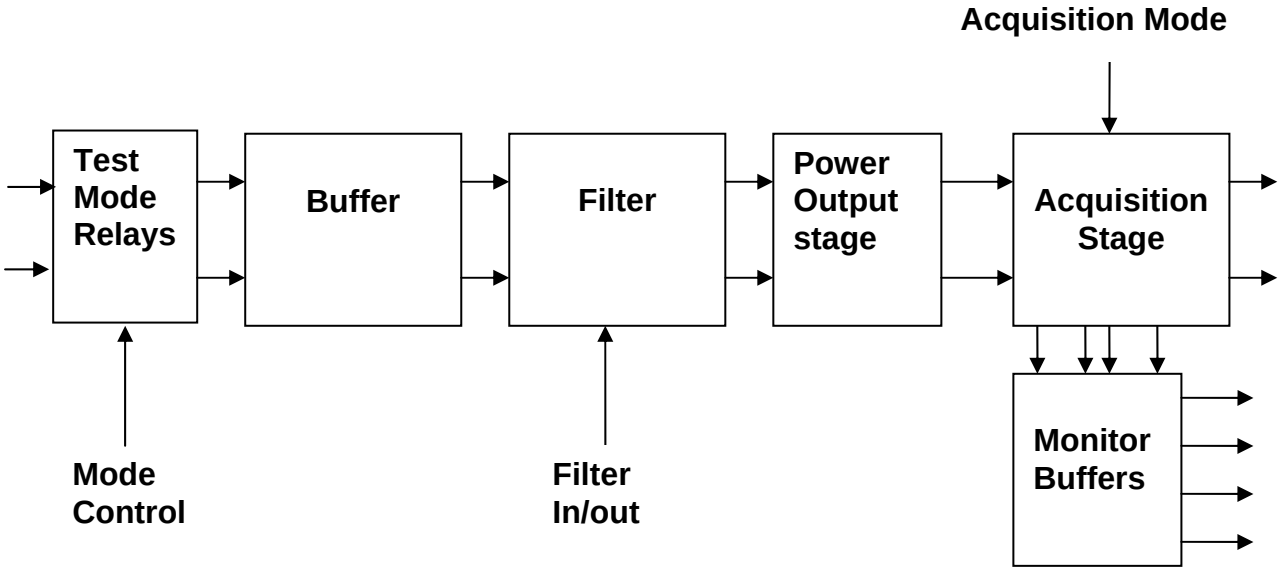
Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P46….Serial No ……
Test Engineer …Simon Pyatt……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P46….Serial No ……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

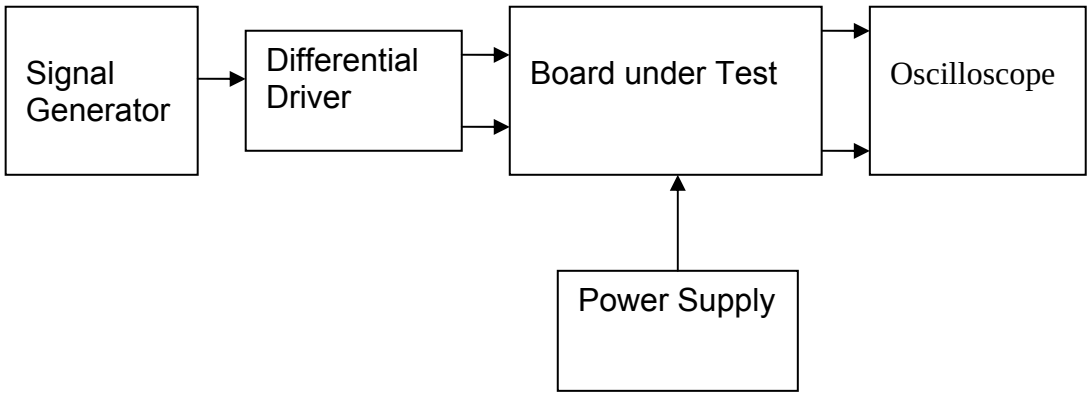
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.13V	√	1mV
+15v TP4	14.82V	√	1mV
-15v TP6	-15.04V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P46….Serial No ……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.0	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.1	-21dB	-18dB	√

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Date …21/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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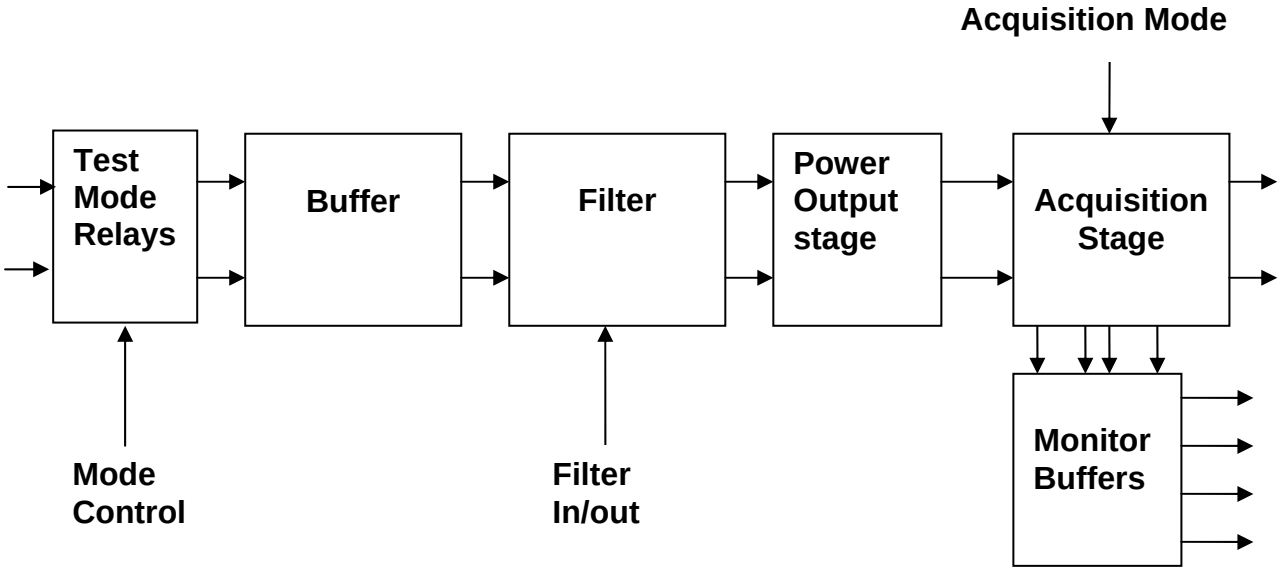
Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

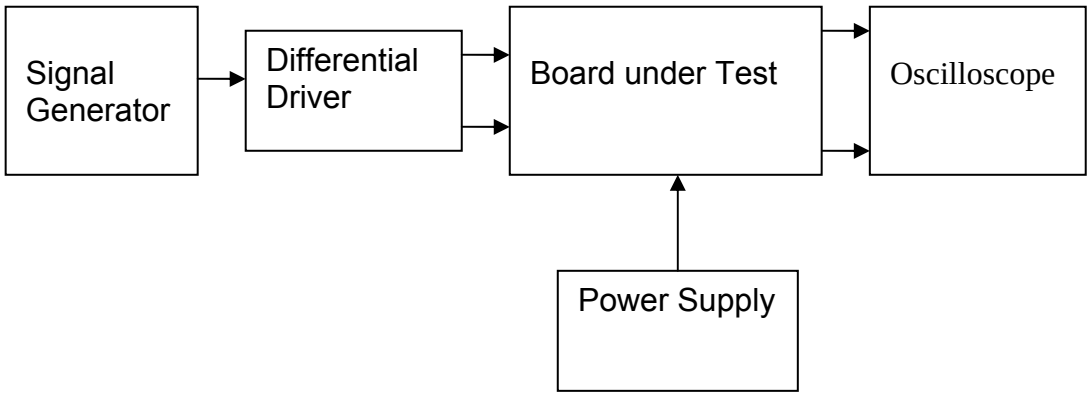
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.12V	√	1mV
+15v TP4	14.80V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P47….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

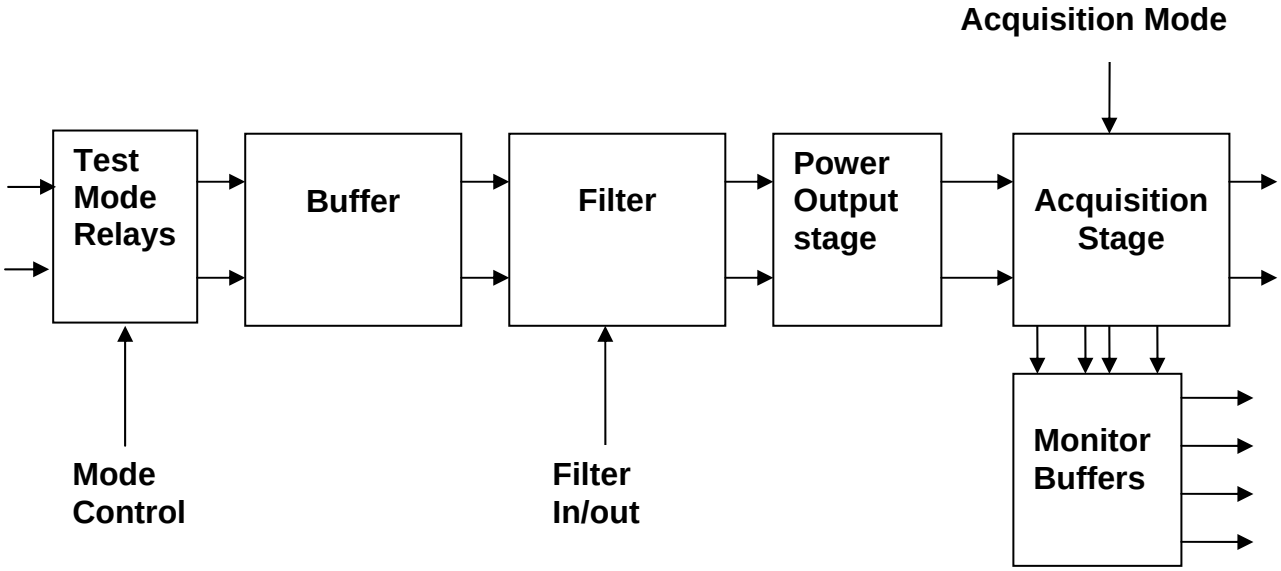
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
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Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
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Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

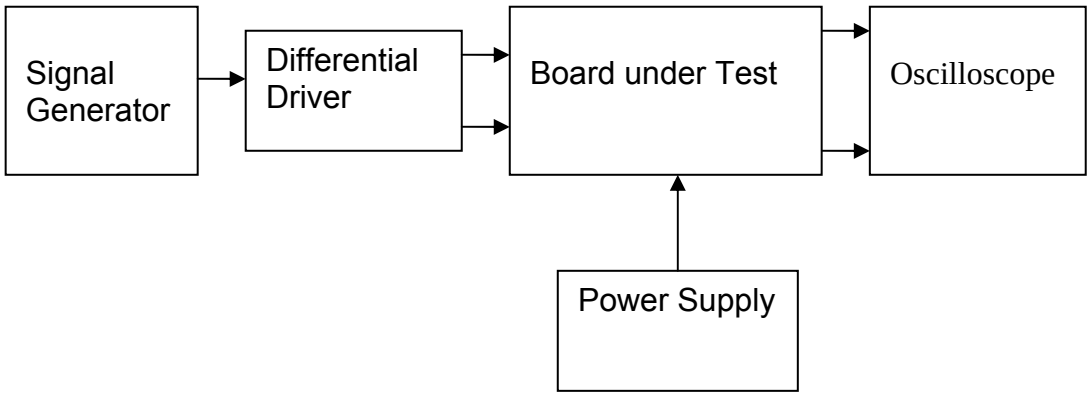
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.09V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	-14.85V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.5	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-17.9	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-17.8	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.8	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.7	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.5	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.4	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.4	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.4	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.4	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.3	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P48….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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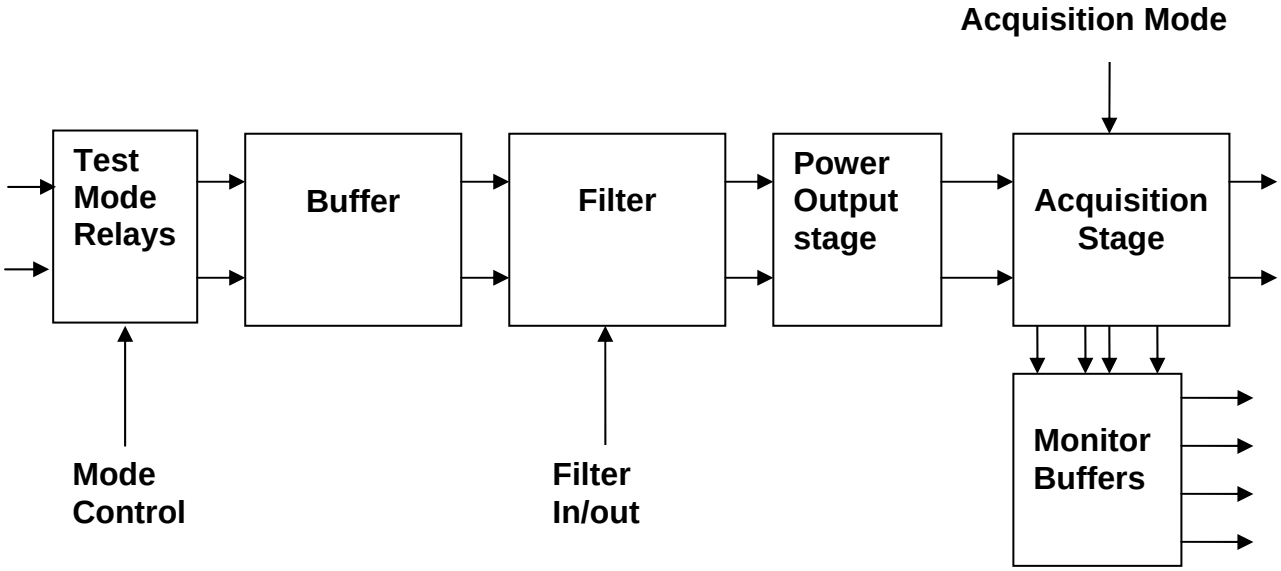
Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

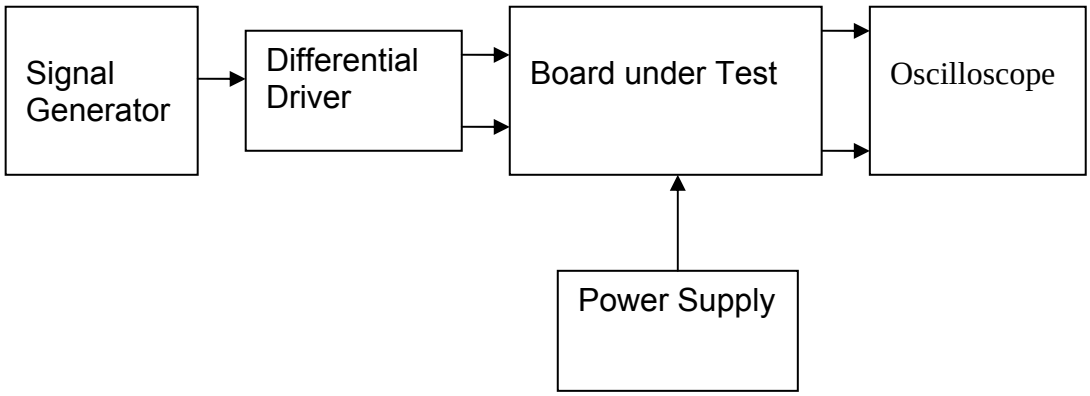
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P49….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-15.01V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P49….Serial No ……
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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P49….Serial No ……
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P49….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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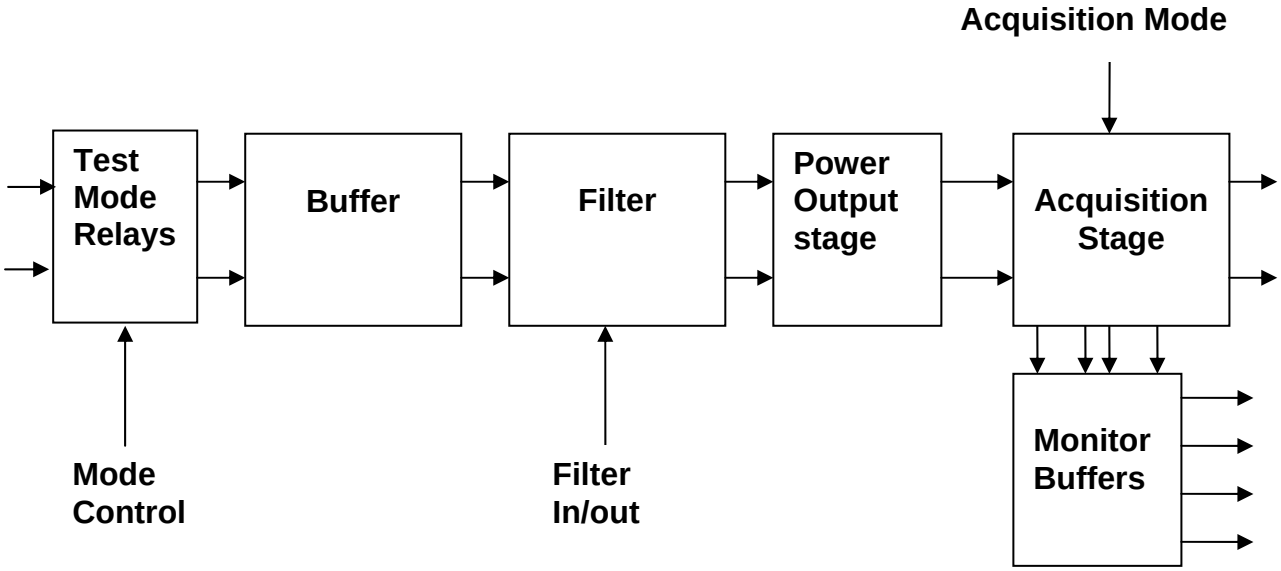
Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

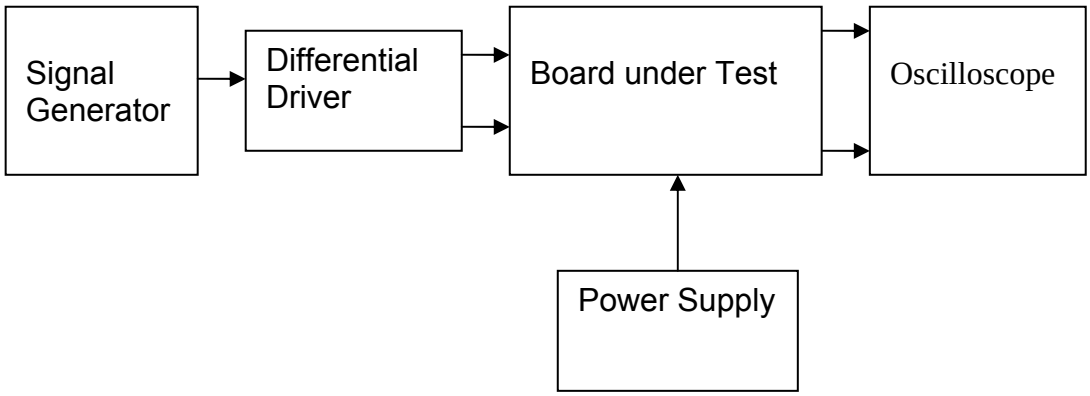
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.91V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.4	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.0	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P50….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

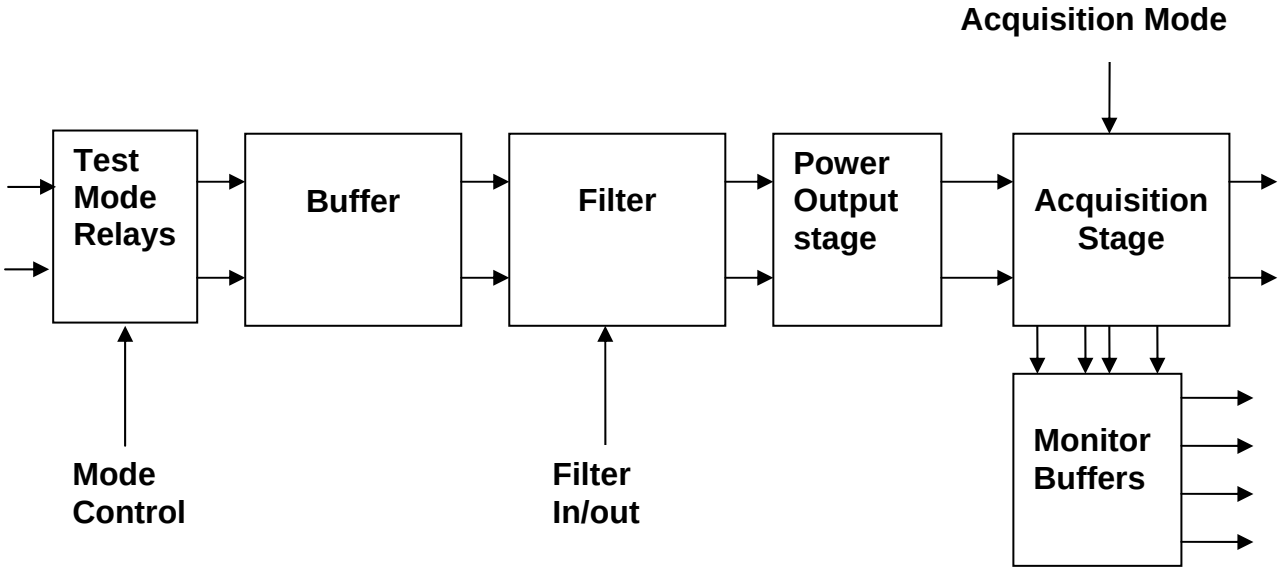
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

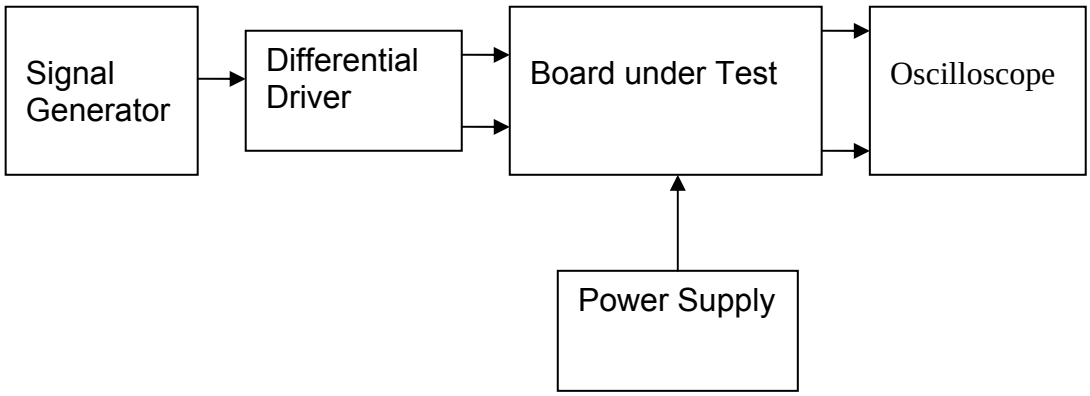
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.80V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.20V	Pin 1 to Pin 2	2.20V	√
2	2.20V	Pin 5 to Pin 6	2.20V	√
3	2.20V	Pin 9 to Pin 10	2.20V	√
4	2.20V	Pin 13 to Pin 14	2.20V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.32V	Pin 3 to Pin 4	0.32V	√
2	0.32V	Pin 7 to Pin 8	0.32V	√
3	0.33V	Pin 11 to Pin 12	0.33V	√
4	0.33V	Pin 15 to Pin 16	0.33V	√

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P51….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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Unit…T_ACQ_P52….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

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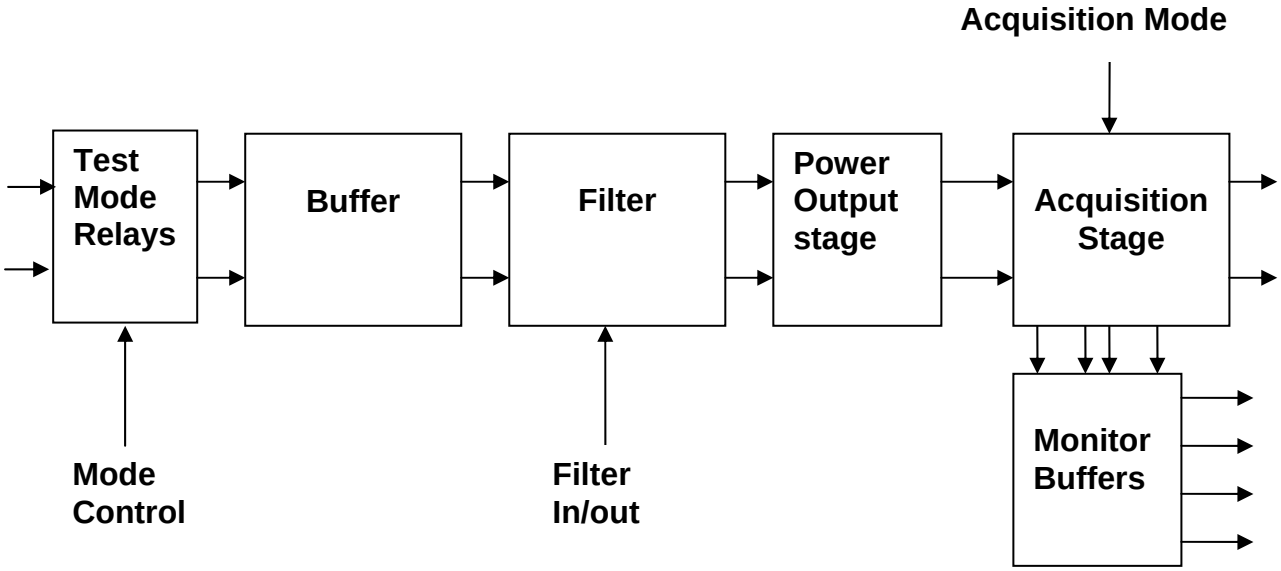
Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P52….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P52….Serial No ……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P52….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

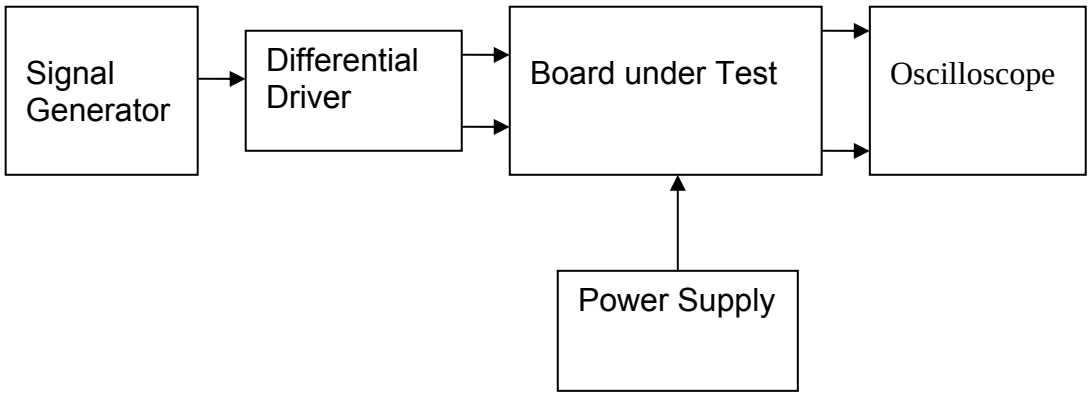
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.01V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.04V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P52….Serial No ……
Test Engineer …Simon Pyatt……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P52….Serial No ……
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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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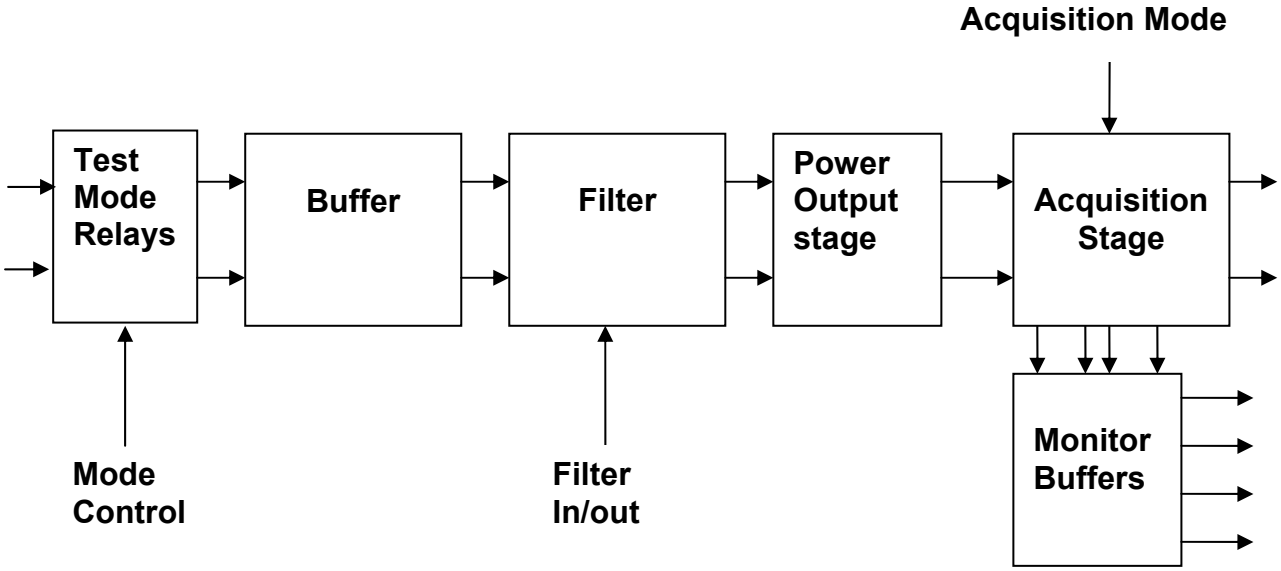
Block diagram



1. Description

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The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

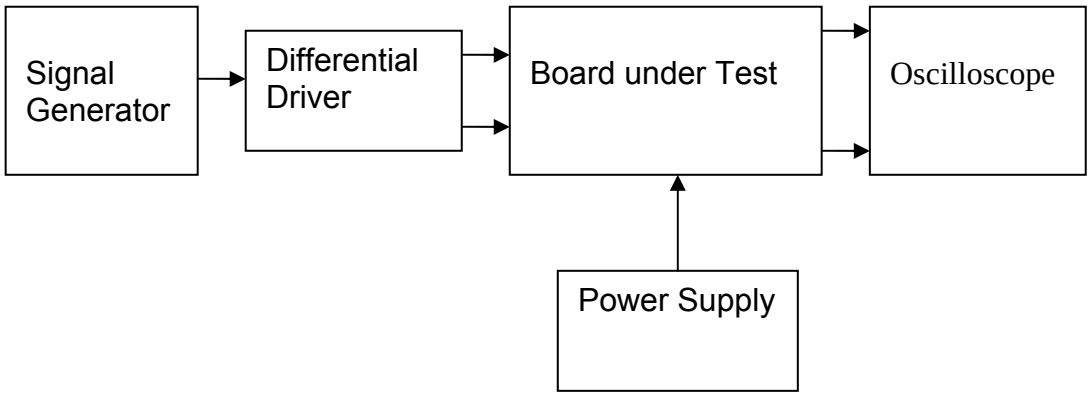
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.79V	√	1mV
-15v TP6	-15.08V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.1	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P53….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

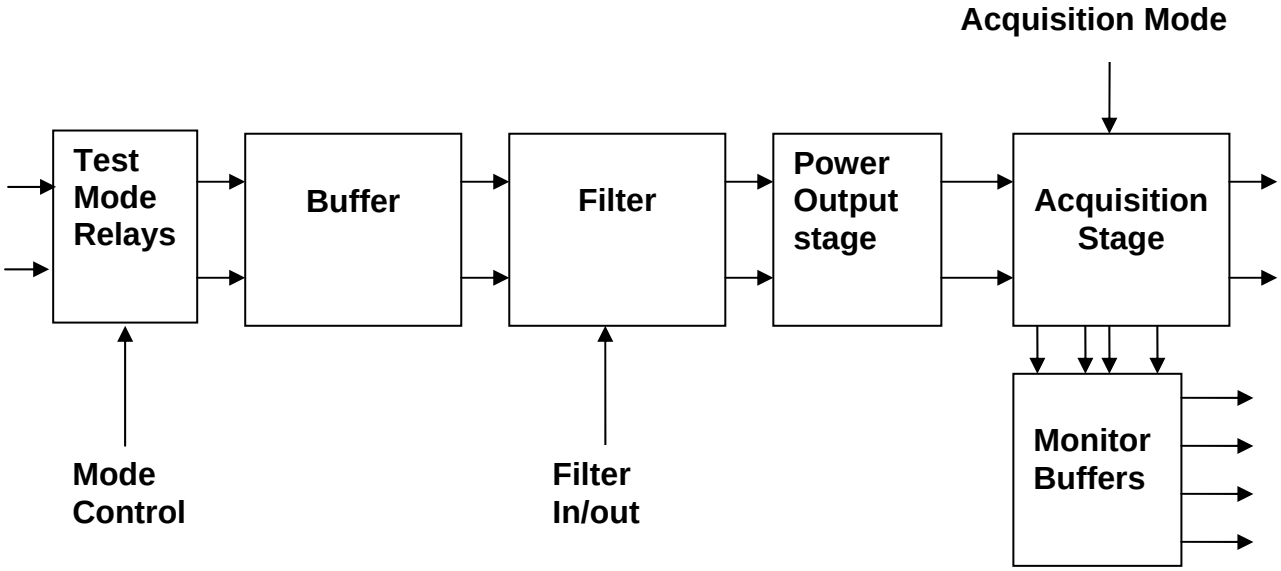
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

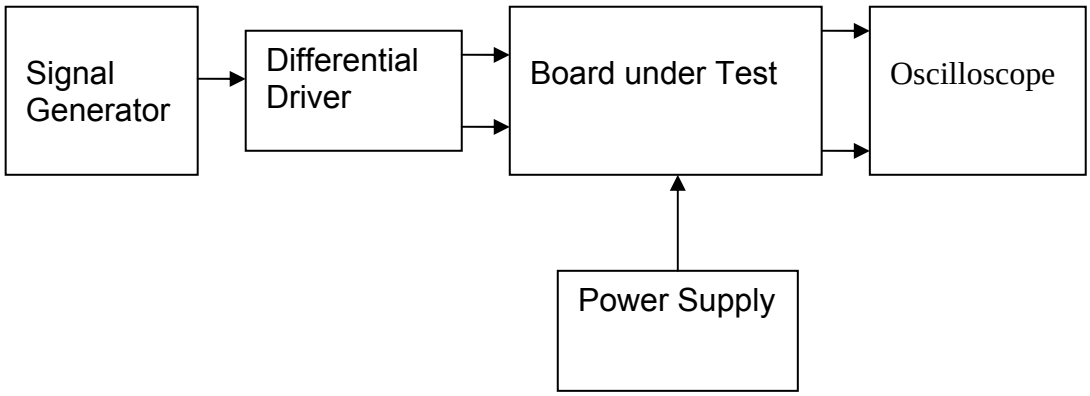
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-14.93V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-29.0	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …19/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P54….Serial No ……
Test Engineer …Simon Pyatt……
Date …29/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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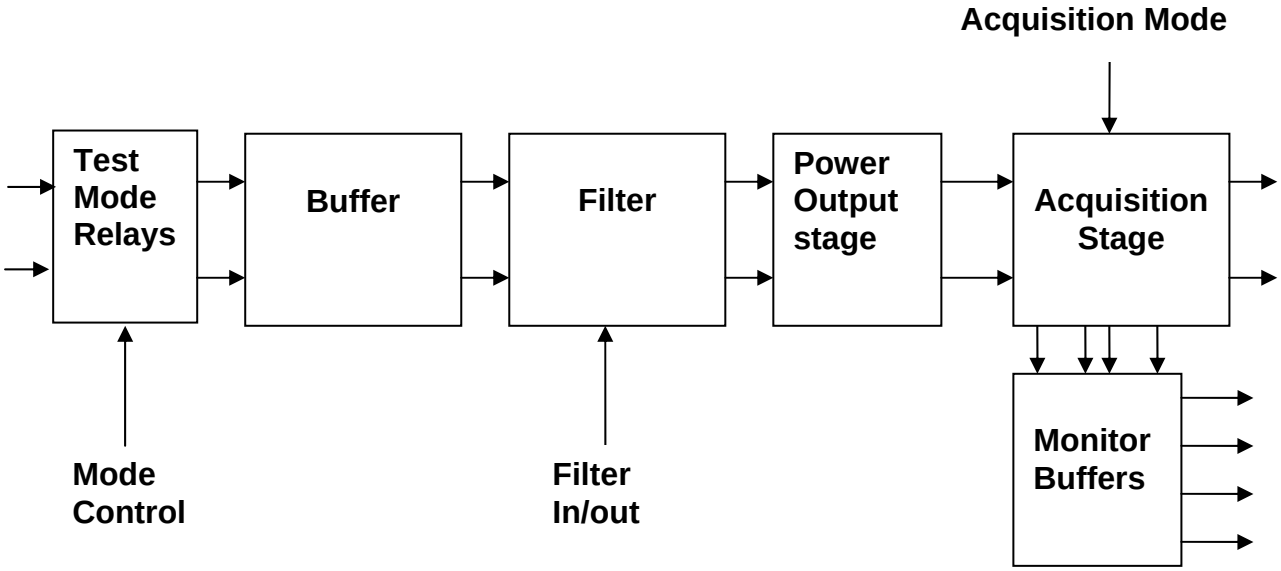
Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

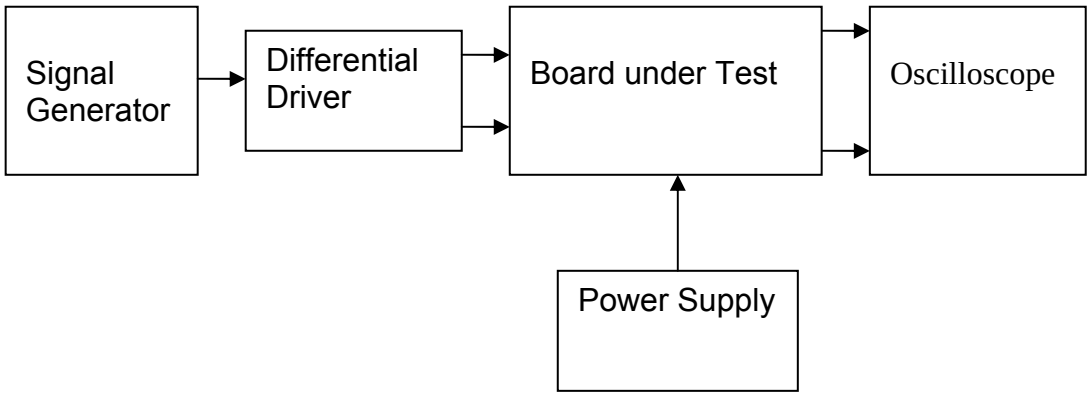
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P55….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.07V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-29.4	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P55….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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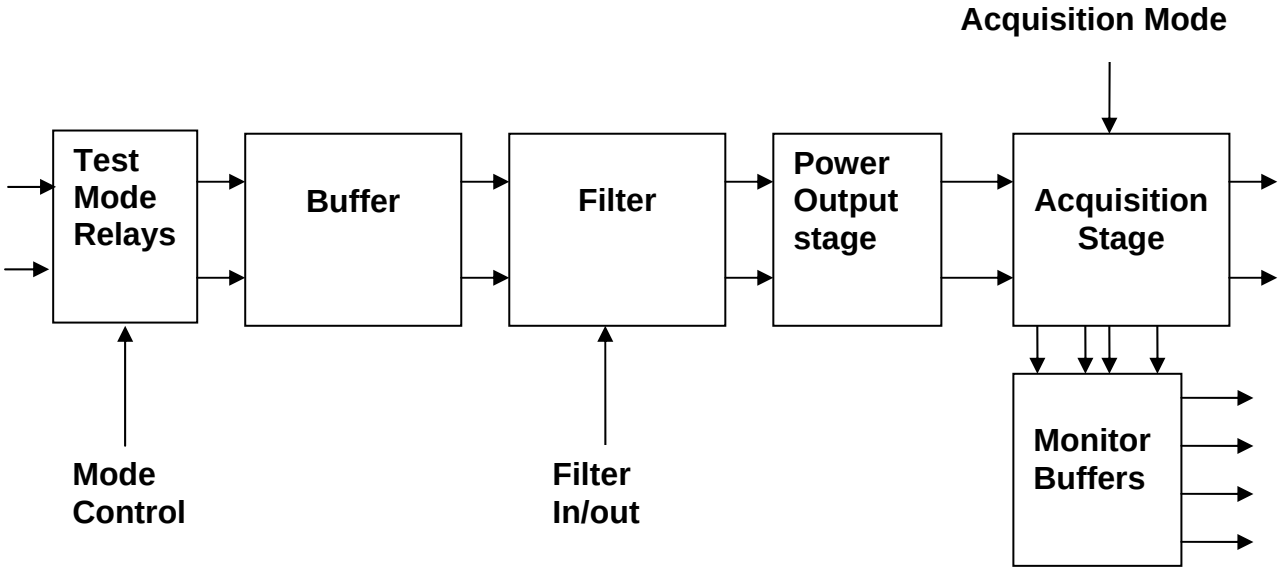
Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

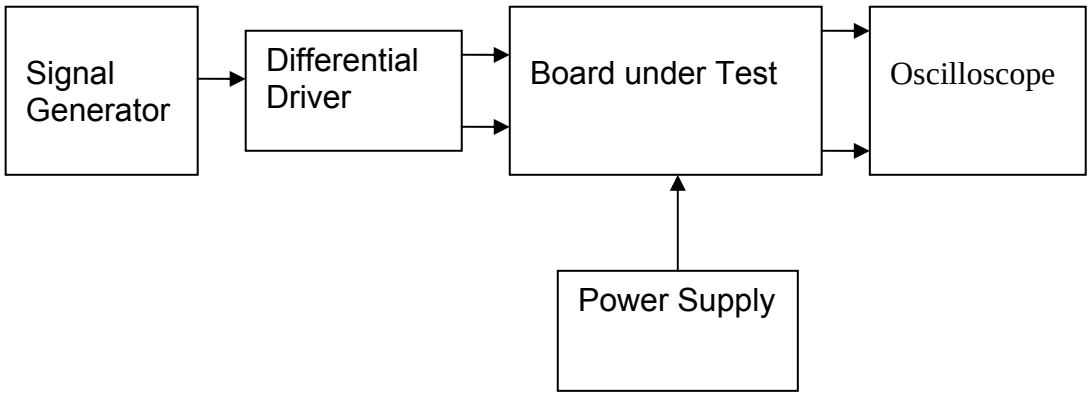
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	14.99V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.0	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-29.3	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …20/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P56….Serial No ……
Test Engineer …Simon Pyatt……
Date …30/04/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

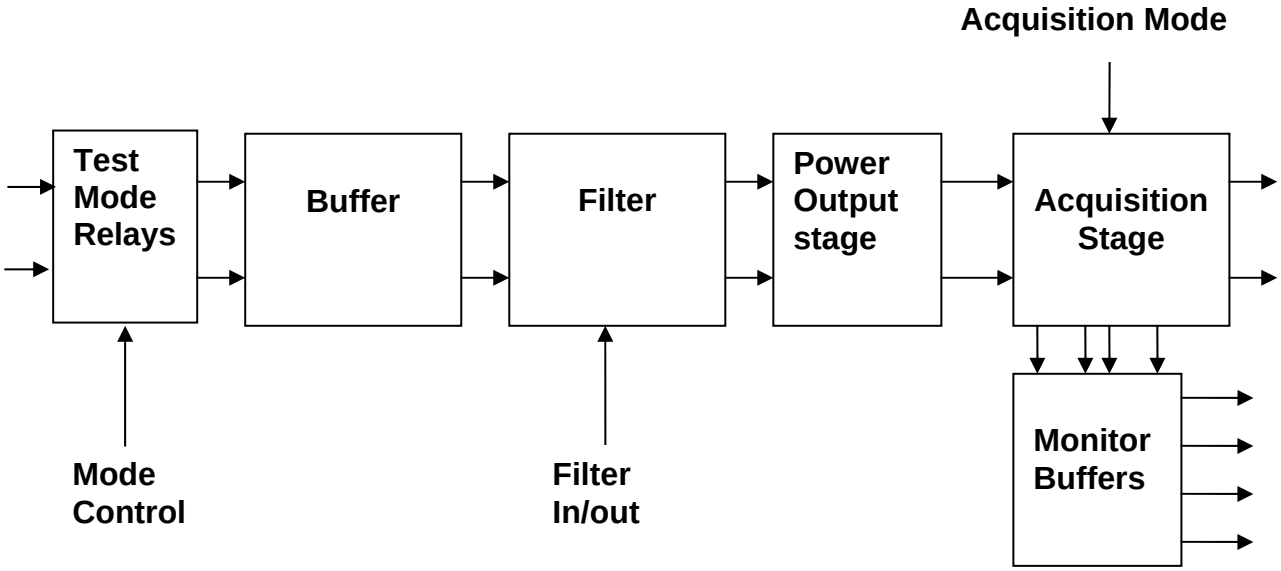
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

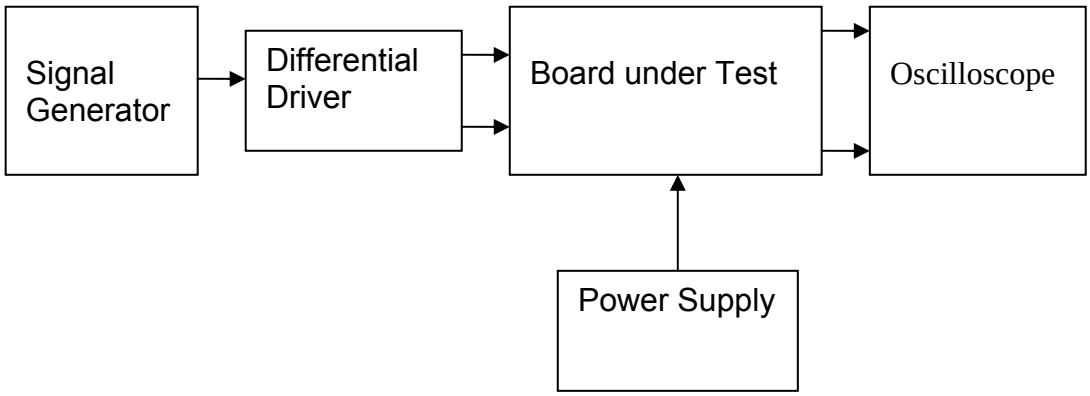
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-15.05V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.4	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.4	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.8	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P57….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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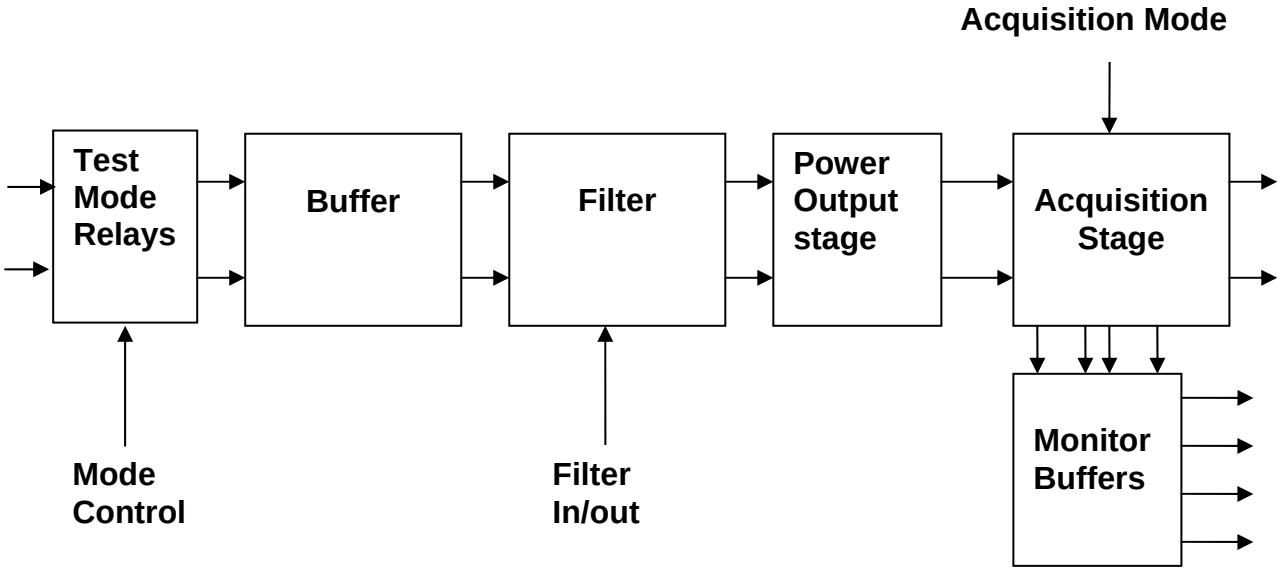
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Low voltage test revealed that C18 Ch4 was causing a short circuit. Component has been replaced.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P58….Serial No ……
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

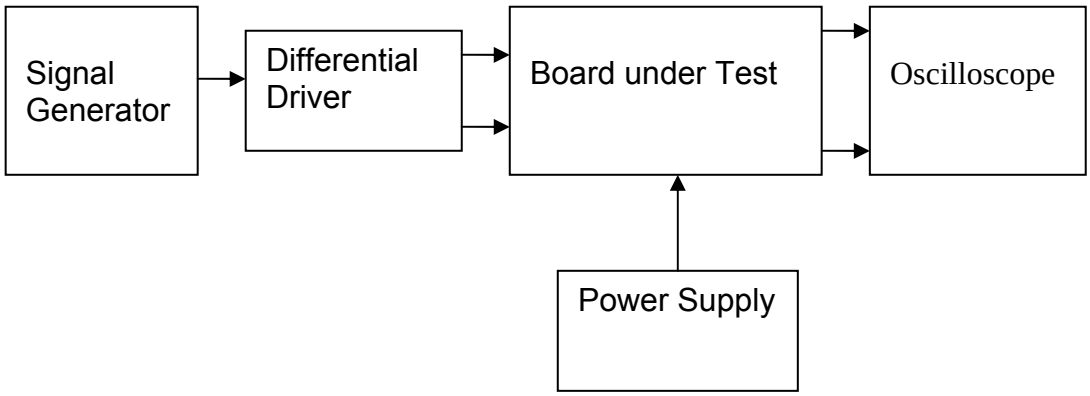
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.98V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
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8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.0	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P58….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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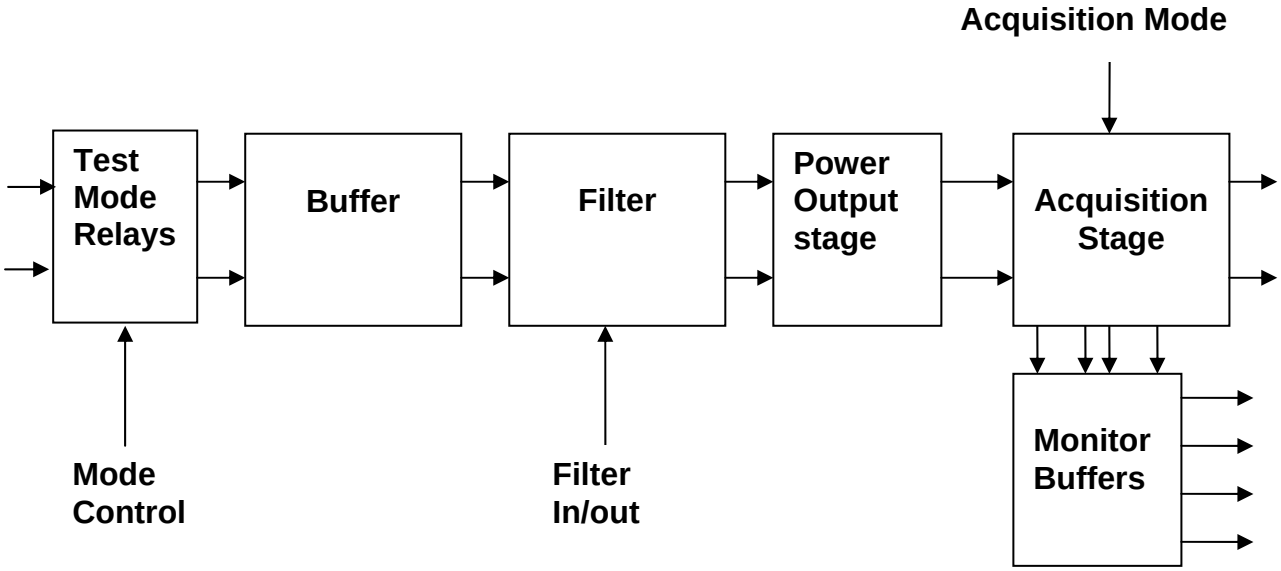
Block diagram



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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

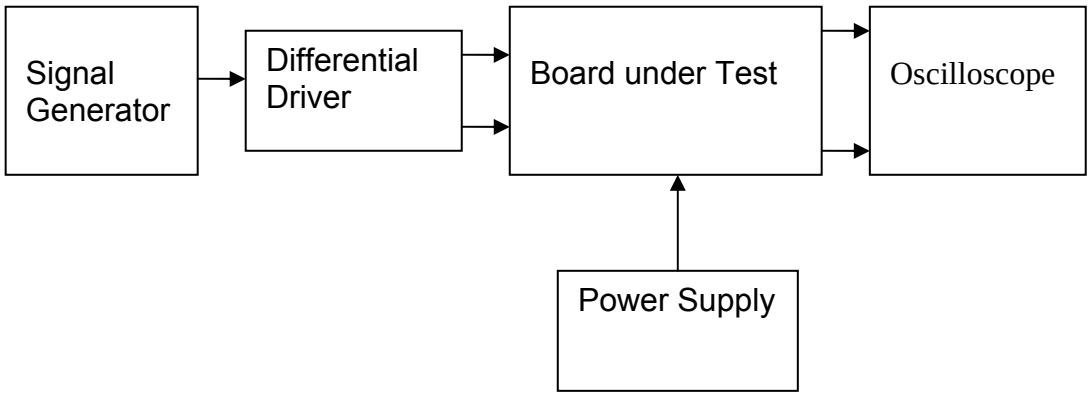
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.94V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.9	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.2	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P59….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

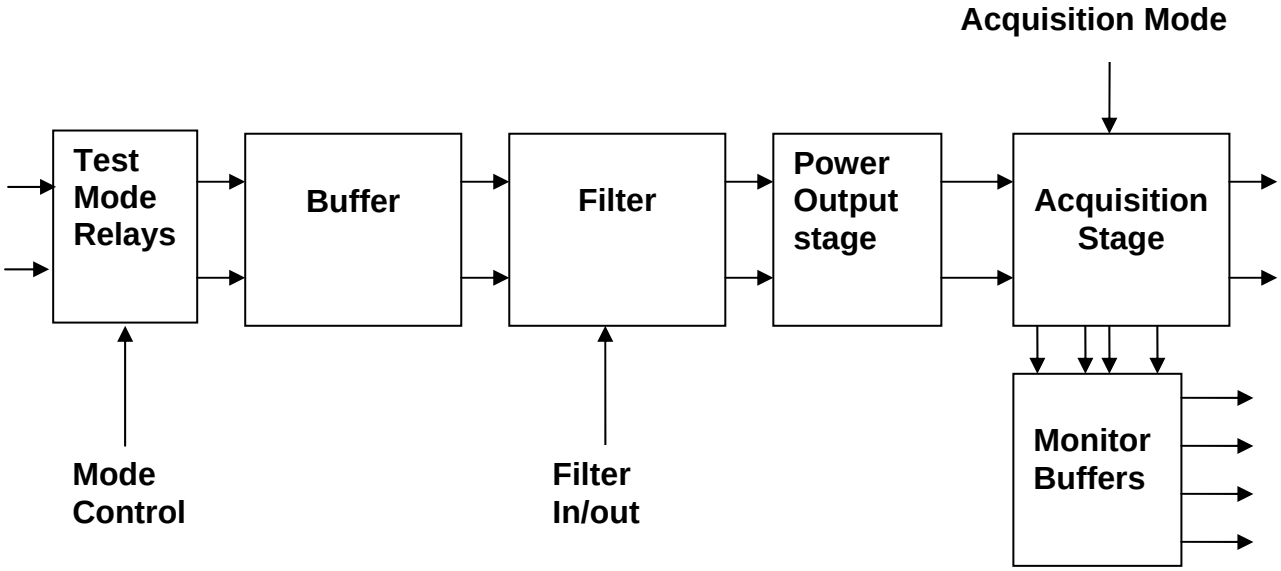
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is very slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

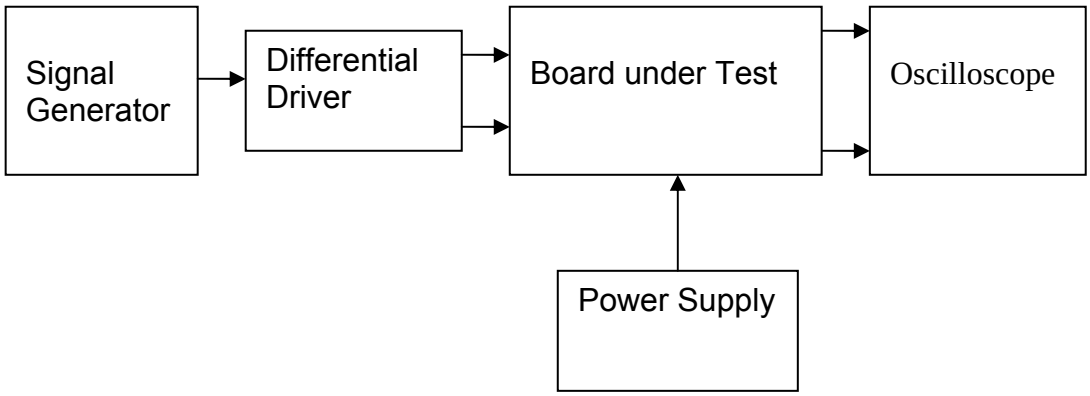
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P60….Serial No ……
Test Engineer …Simon Pyatt……
Date …26/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

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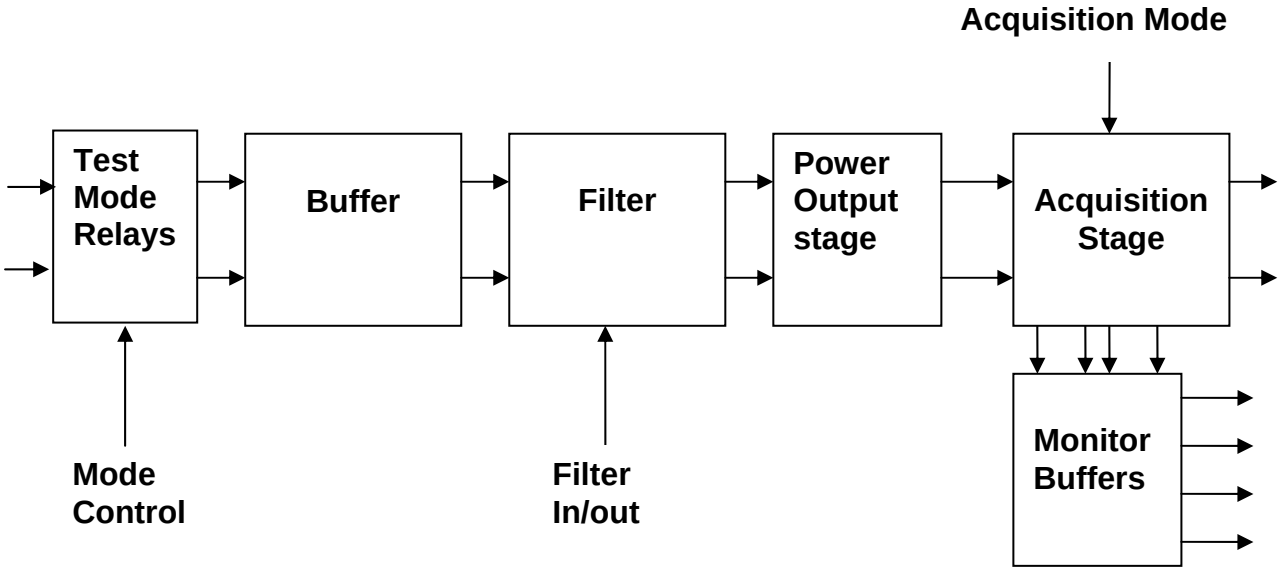
Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

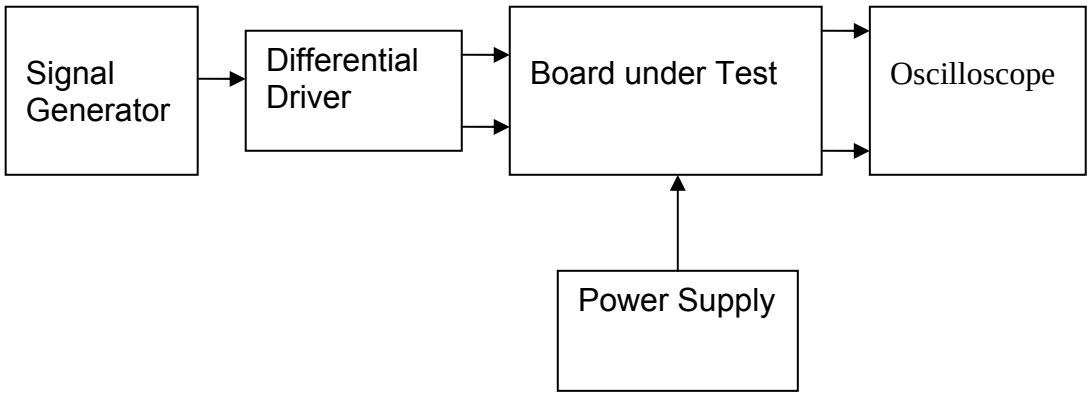
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P61….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.03V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-15.05V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.0	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.3	-30dB	-27dB	√
Ch3	-28.5	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P61….Serial No ……
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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P61….Serial No ……
Test Engineer …Simon Pyatt……
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12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V		-22V		-22V		-22V	
-1v	-4.5V		-4.5V		-4.5V		-4.5V	
0v	0V		0V		0V		0V	
1v	4.5V		4.5V		4.5V		4.5V	
5v	22V		22V		22V		22V	

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of the Advanced LIGO Project, prepared by members of the UK team.

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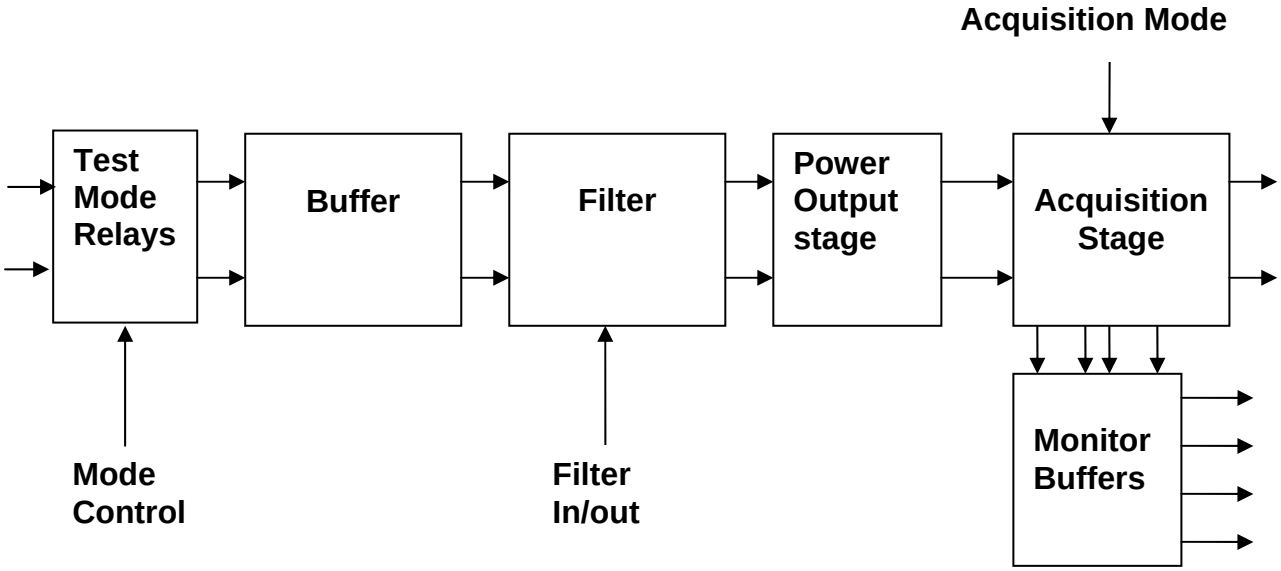
Block diagram



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The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

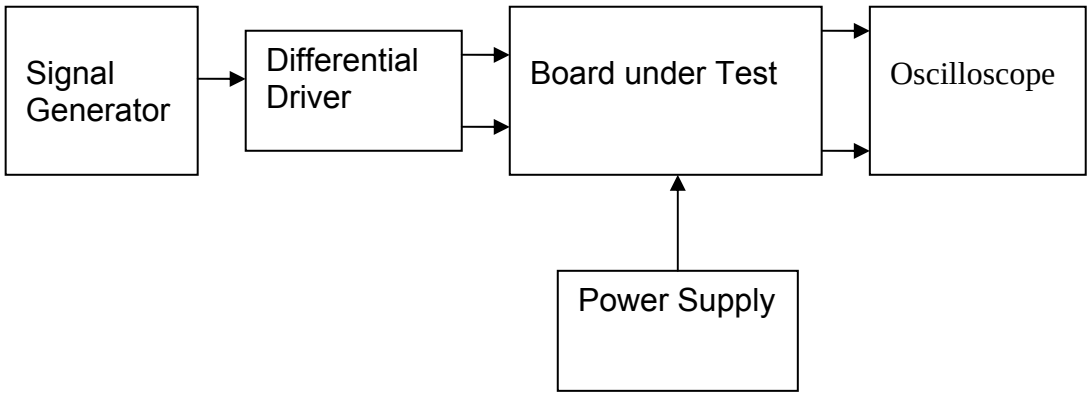
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.89V	√	1mV
-15v TP6	-14.94V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.0	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-29.1	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P62….Serial No ……
Test Engineer …Simon Pyatt……
Date …27/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

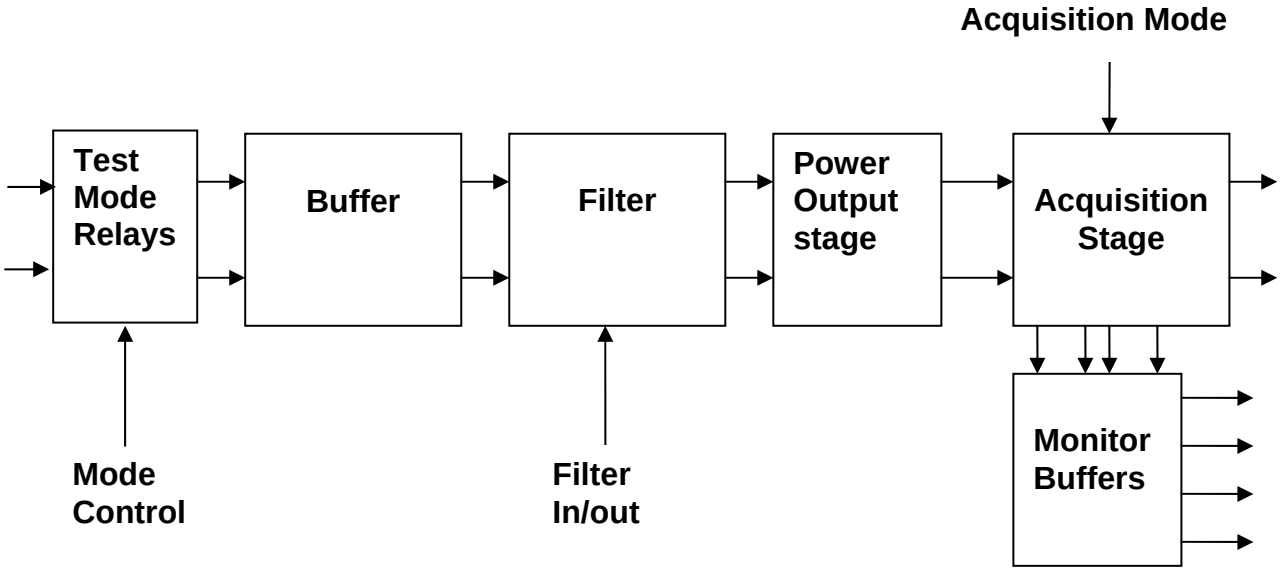
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

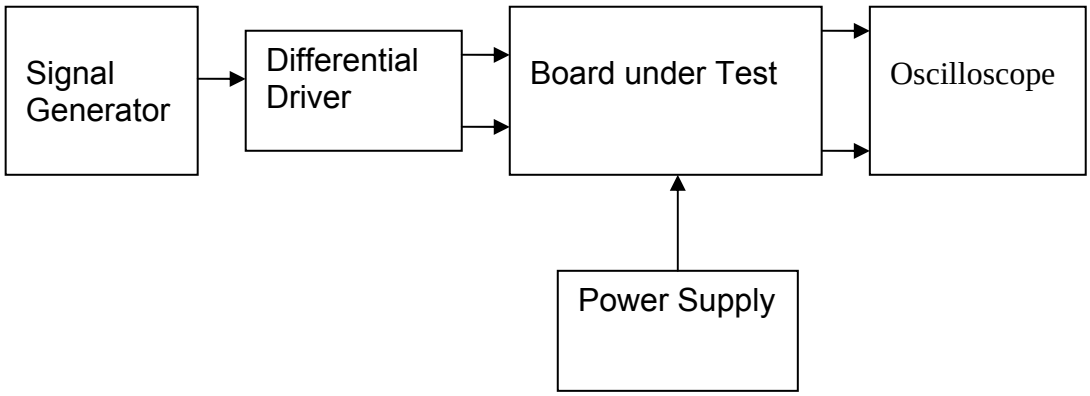
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.4	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-29.4	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P63….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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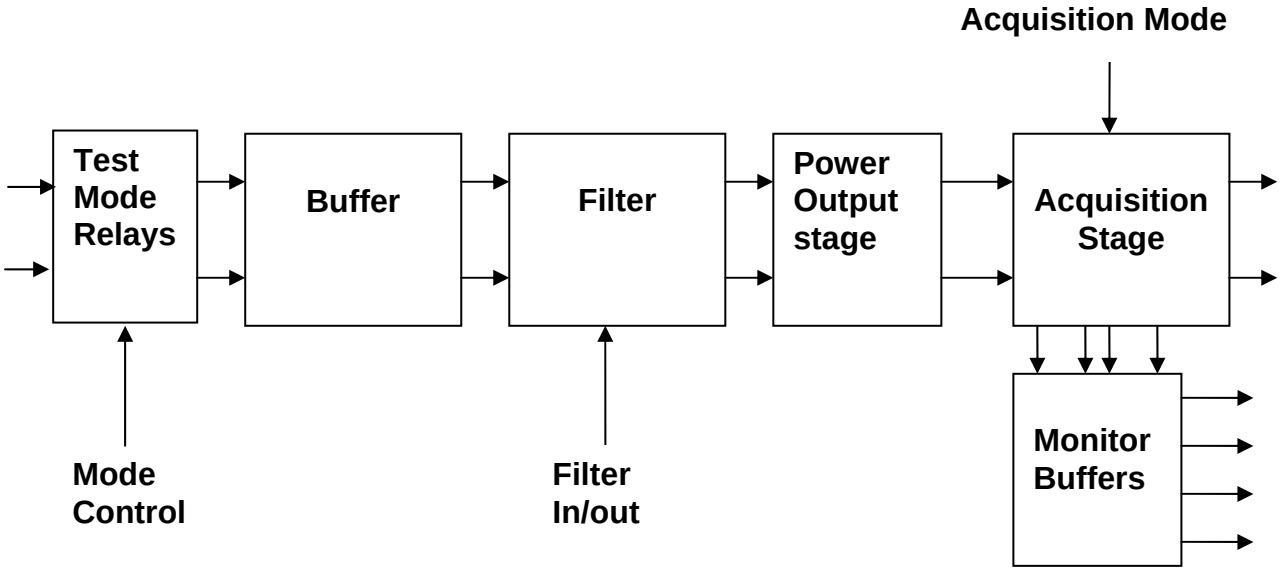
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …28/05/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

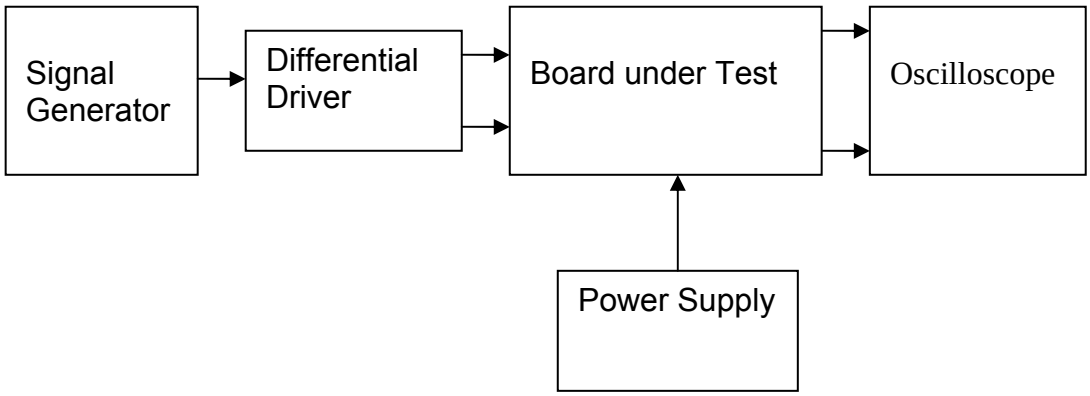
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P64….Serial No ……
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Date …01/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.82V	√	1mV
-15v TP6	-15.13V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P64….Serial No ……
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.8	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.5	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.5	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P64….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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Unit…T_ACQ_P65….Serial No ……
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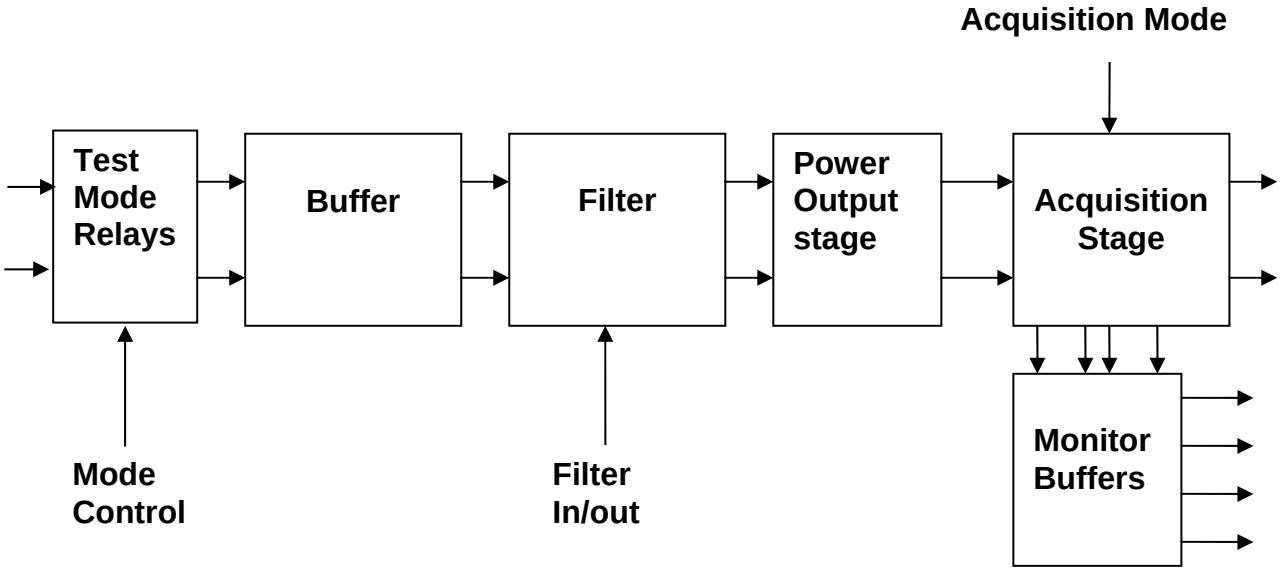
Block diagram



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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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Unit…T_ACQ_P65….Serial No ……
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Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

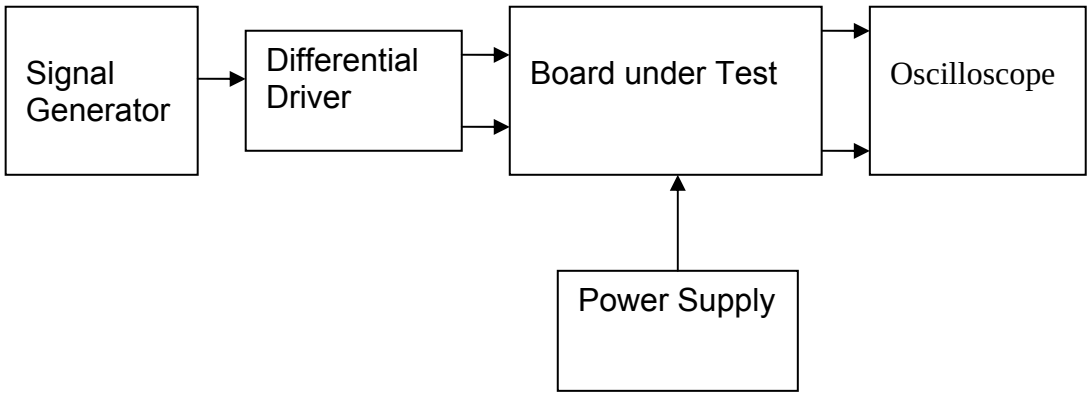
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.00V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-15.11V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P66….Serial No ……
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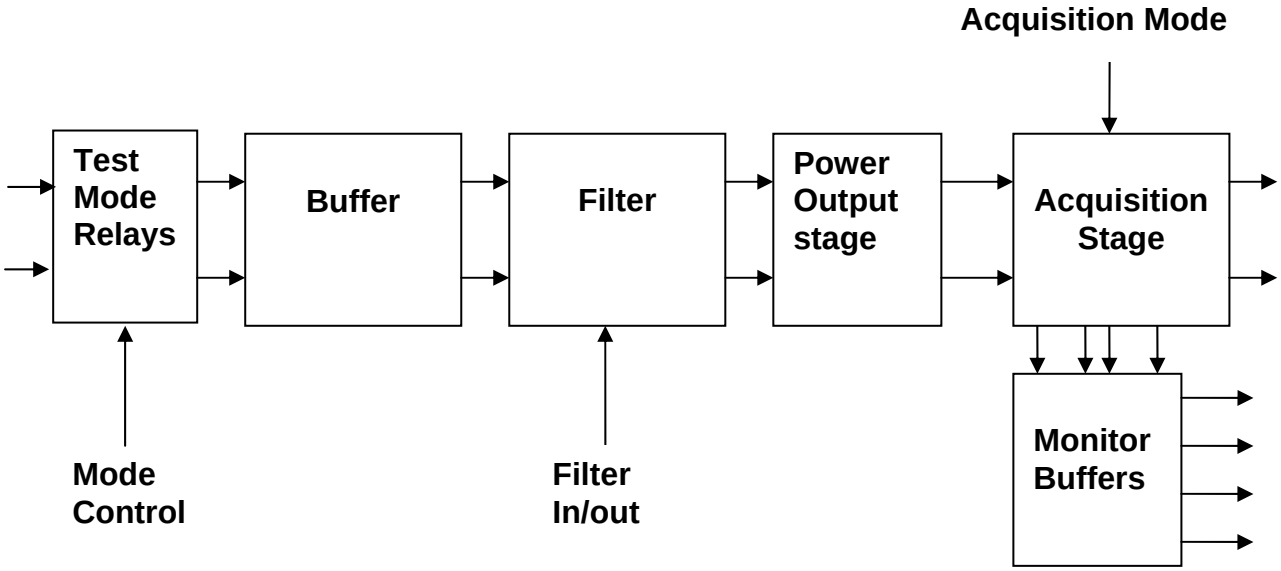
Date …01/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

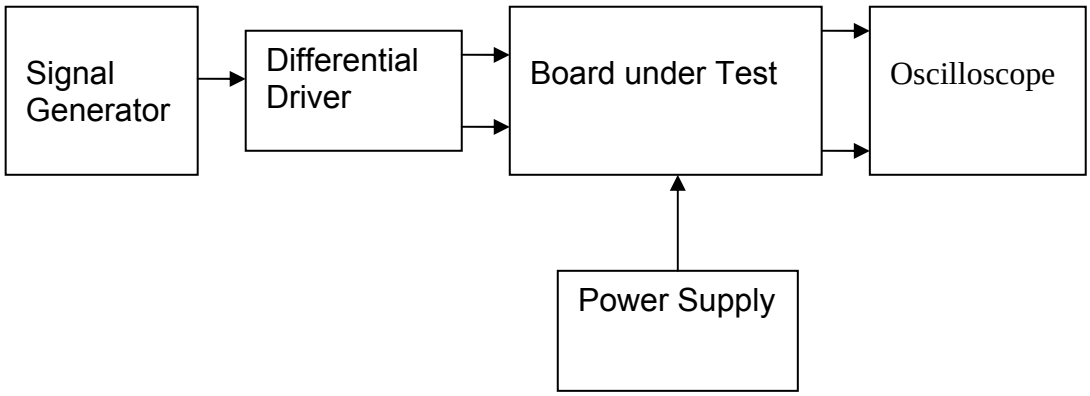
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.07V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.85V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-29.3	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …11/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P65….Serial No ……
Test Engineer …Simon Pyatt……
Date …01/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

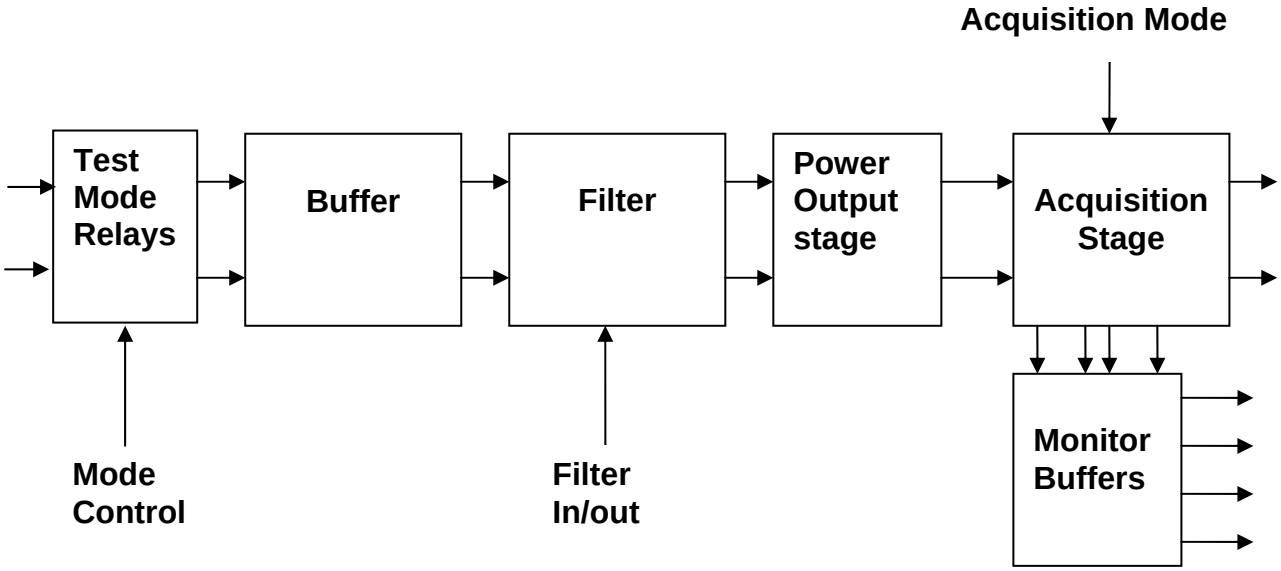
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

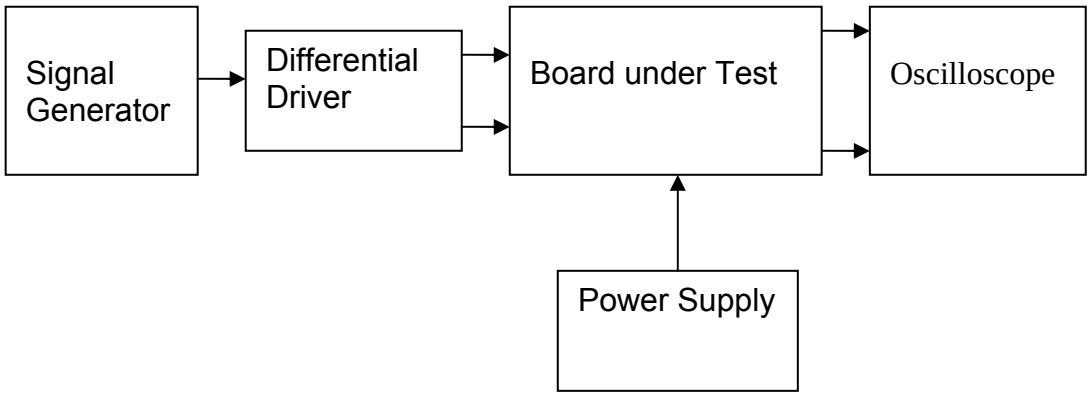
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.09V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.8	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-29.1	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …10/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P67….Serial No ……
Test Engineer …Simon Pyatt……
Date …02/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

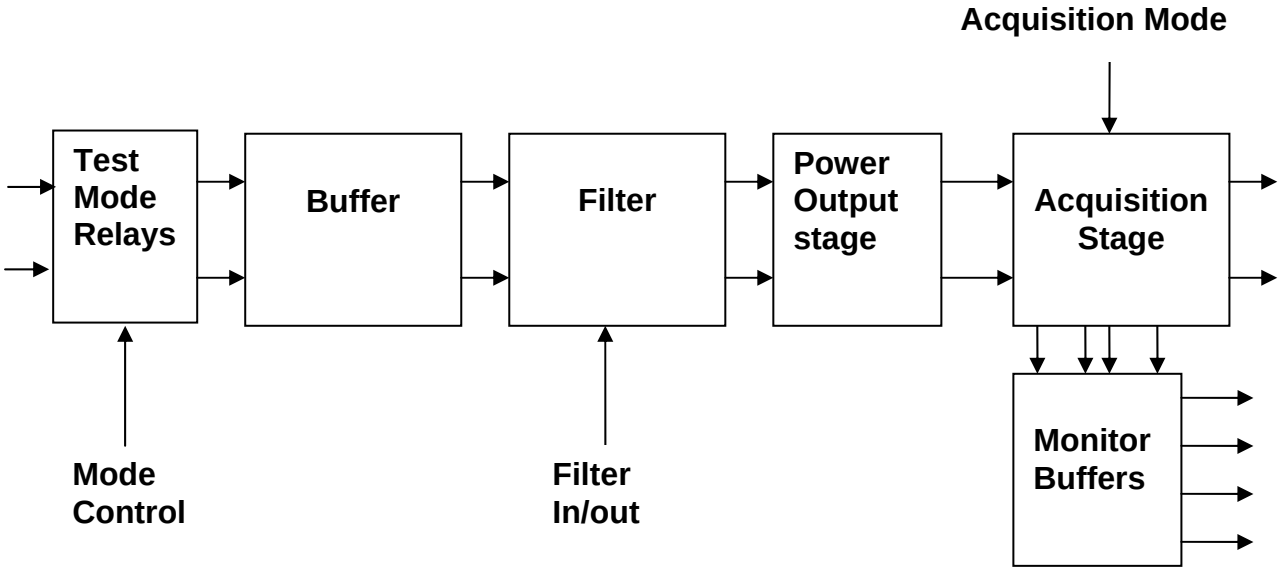
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

Contents

Block diagram



1. Description

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

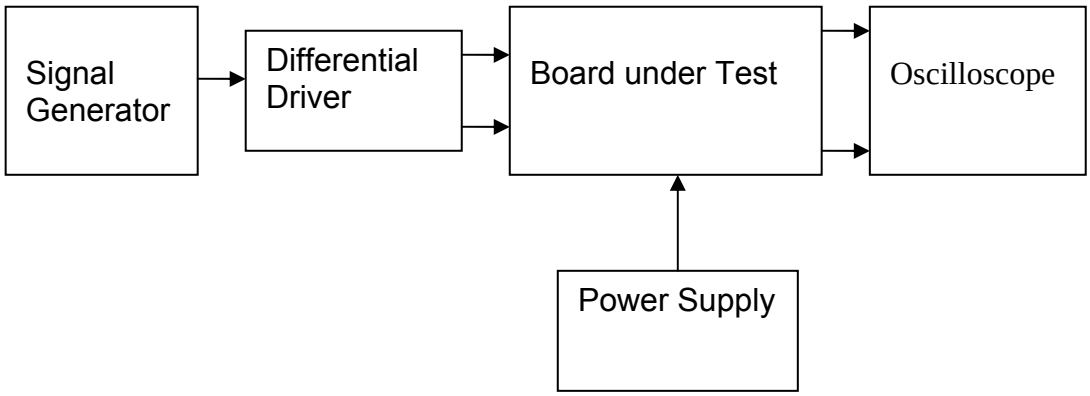
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.79V	√	1mV
-15v TP6	-15.00V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.4	-30dB	-27dB	√
Ch2	-29.0	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P68….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

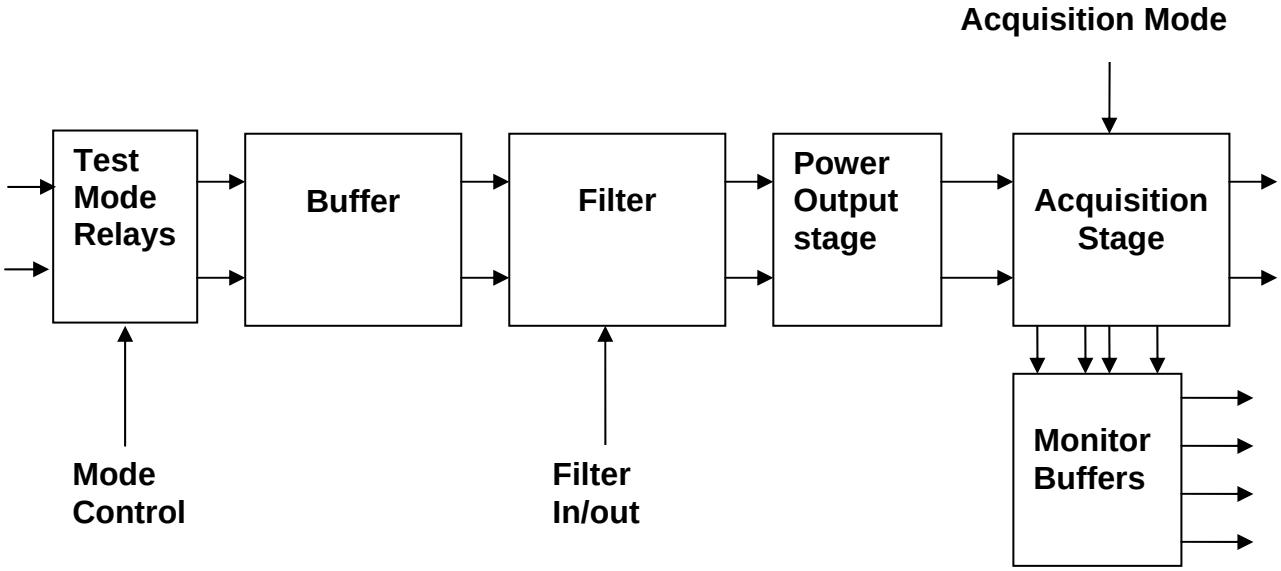
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

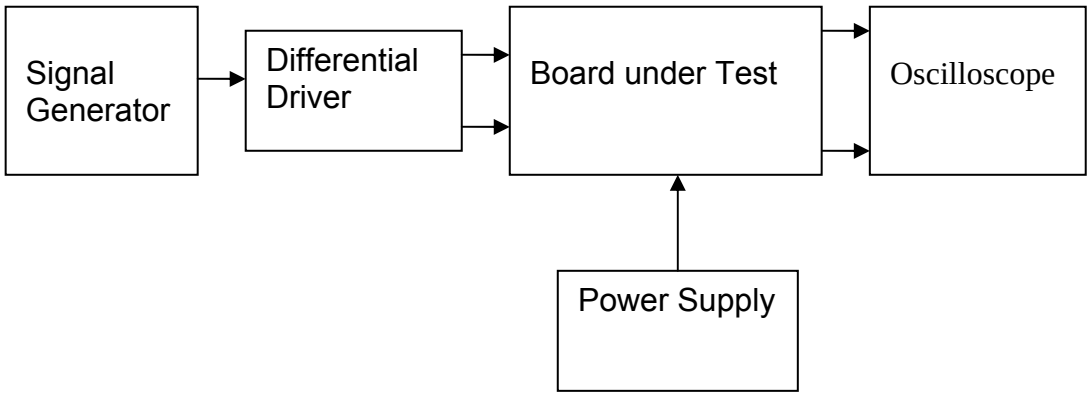
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.13V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-14.92V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.1	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.1	-21dB	-18dB	√

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-34.8	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.7	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.5	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.3	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.4	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.3	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P69….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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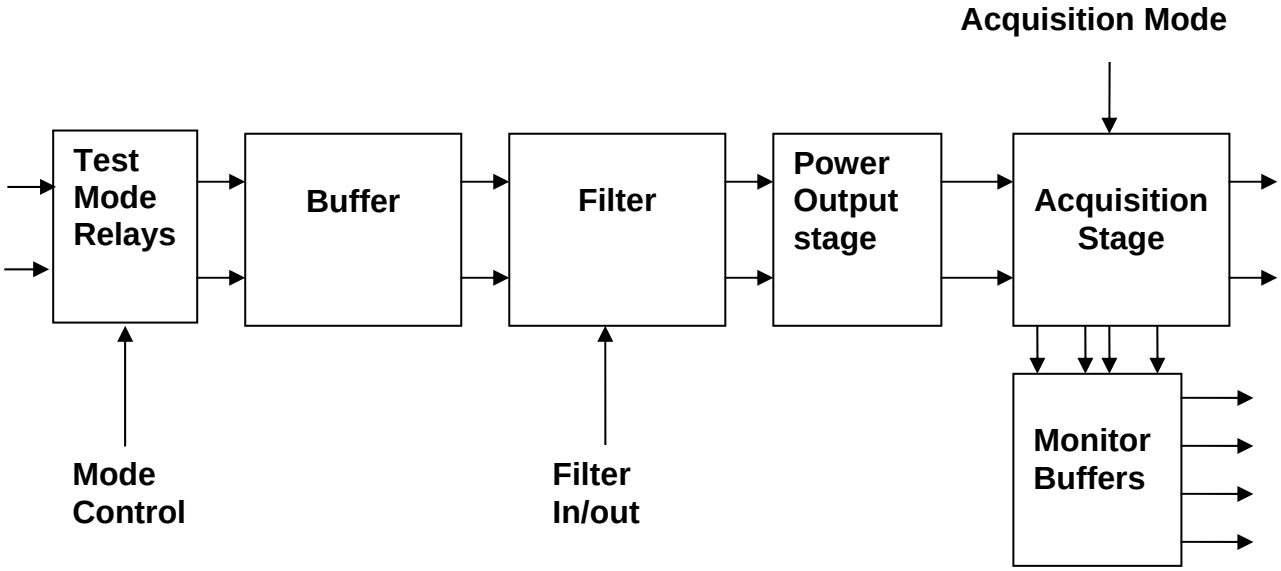
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

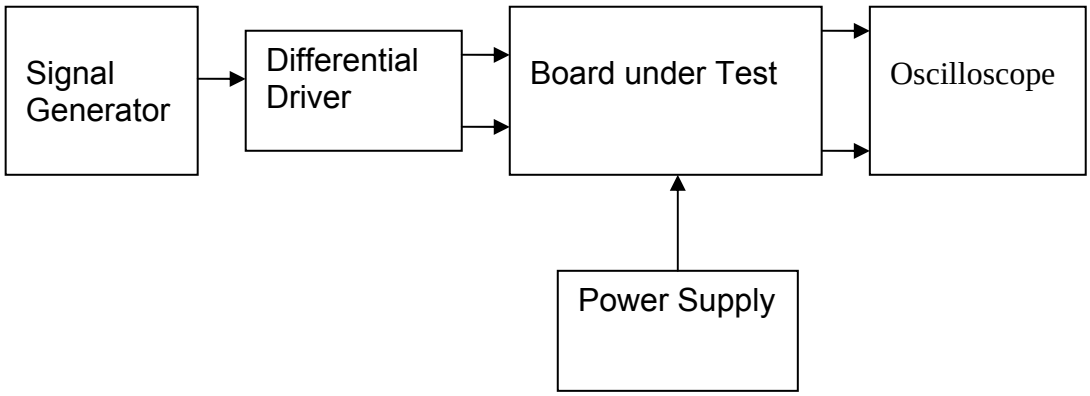
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …03/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	14.79V	√	1mV
-15v TP6	-15.07V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.3	-30dB	-27dB	√
Ch2	-29.3	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.2	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.6	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P70….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V		-22V		-22V		-22V	
-1v	-4.5V		-4.5V		-4.5V		-4.5V	
0v	0V		0V		0V		0V	
1v	4.5V		4.5V		4.5V		4.5V	
5v	22V		22V		22V		22V	

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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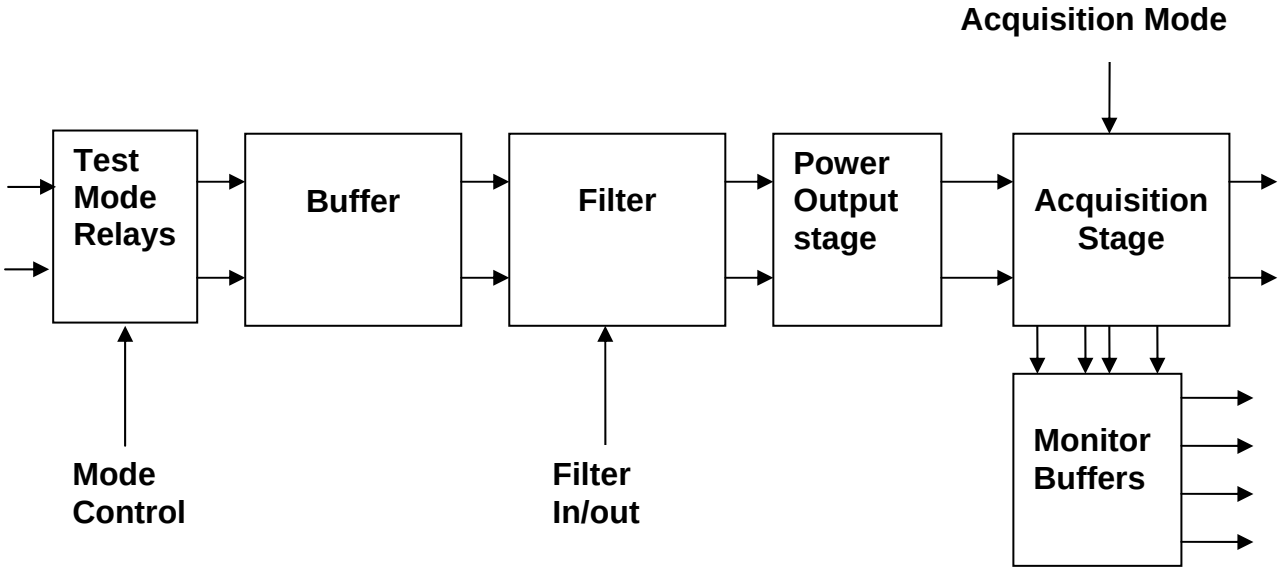
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

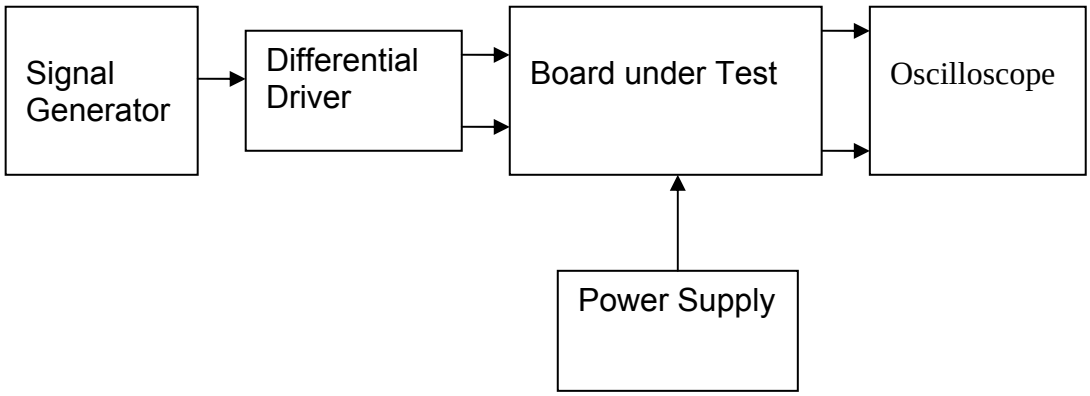
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.96V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.7	-42.5dB	-39.5dB	√
Ch3	-40.5	-42.5dB	-39.5dB	√
Ch4	-40.3	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.3	-53dB	-50dB	√
Ch3	-51.0	-53dB	-50dB	√
Ch4	-50.5	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.1	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.1	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.1	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-18.9	-21dB	-18dB	√

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.7	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.4	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.0	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.6	-6dB / 570mV	-4dB / 565mV	√
Ch3	-4.7	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.8	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.5	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.3	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.4	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.4	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.3	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.3	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.4	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …04/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P71….Serial No ……
Test Engineer …Simon Pyatt……
Date …08/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

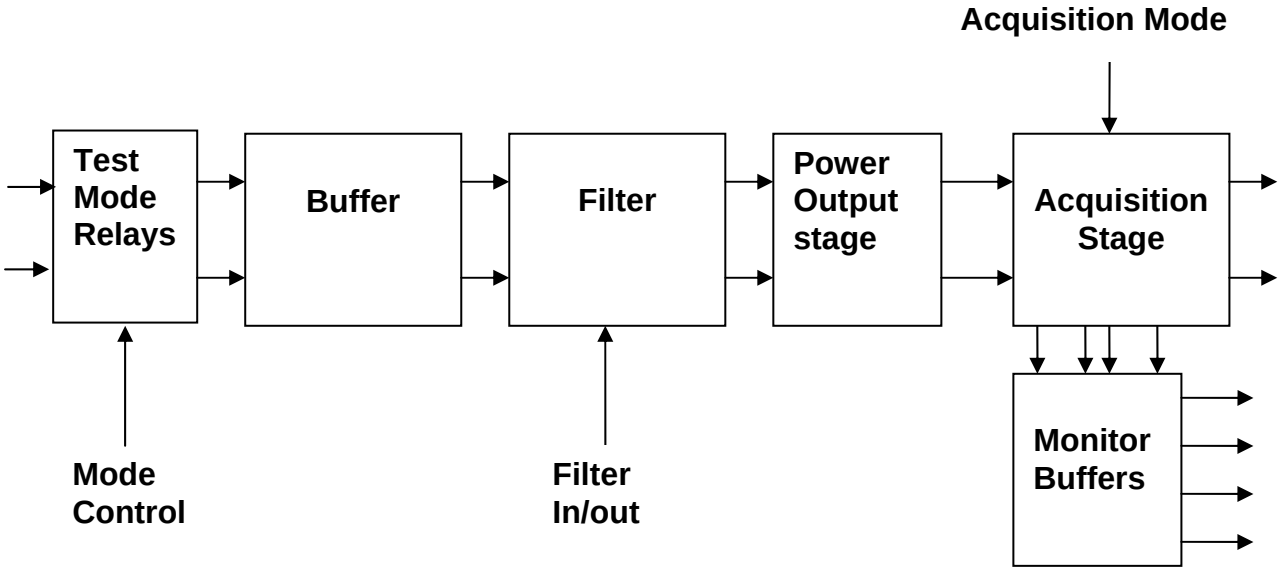
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

U3 (LM2990S) noisy, component has been replaced.

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

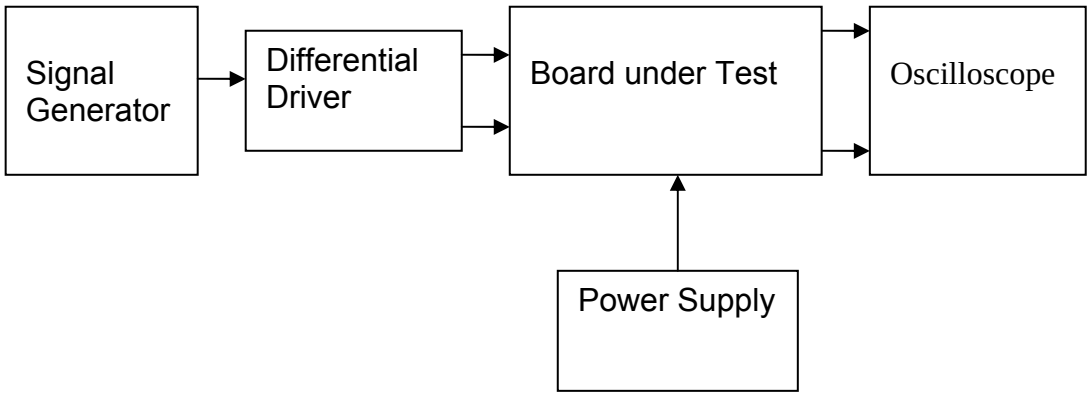
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.10V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-14.86V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-29.1	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P72….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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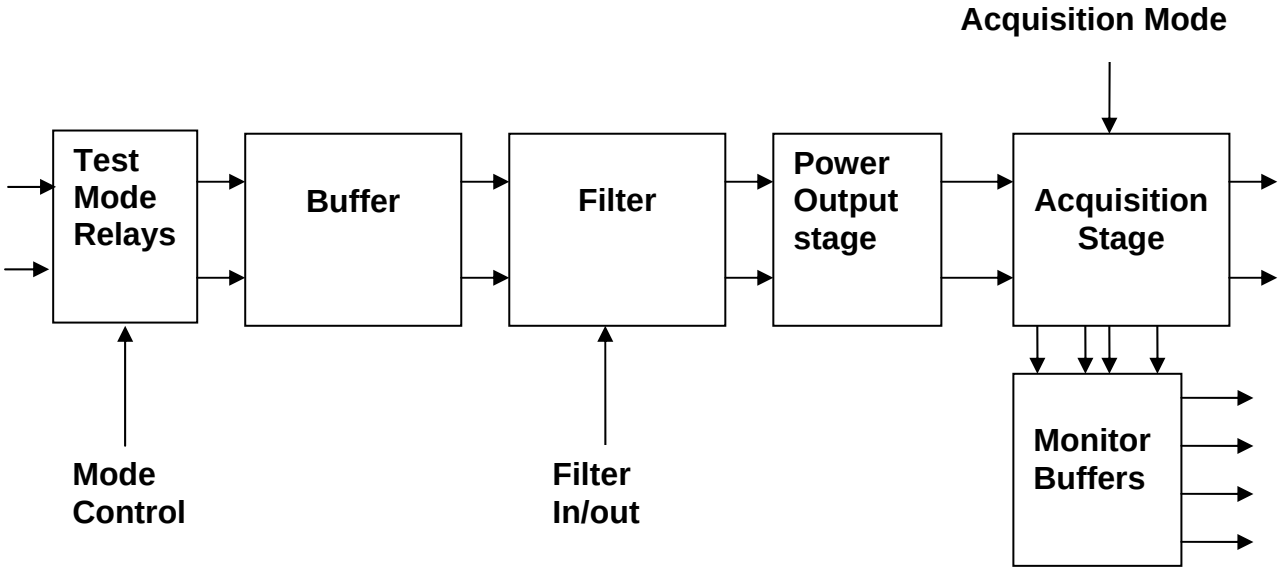
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

J6 connector replace. Original had solder splash on it preventing use.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

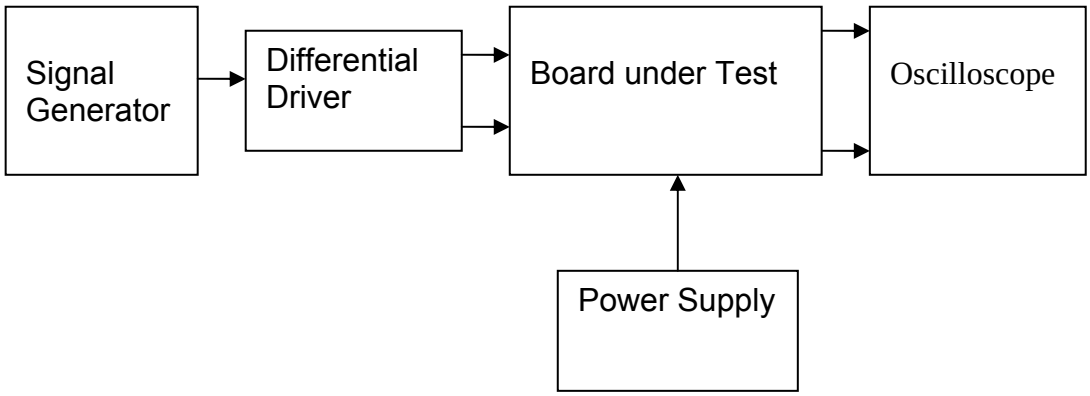
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	15.02V	√	1mV
-15v TP6	-14.98V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.27V	Pin 3 to Pin 4	0.27V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P73….Serial No ……
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.3	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.5	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …14/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P73….Serial No ……
Test Engineer …Simon Pyatt……
Date …15/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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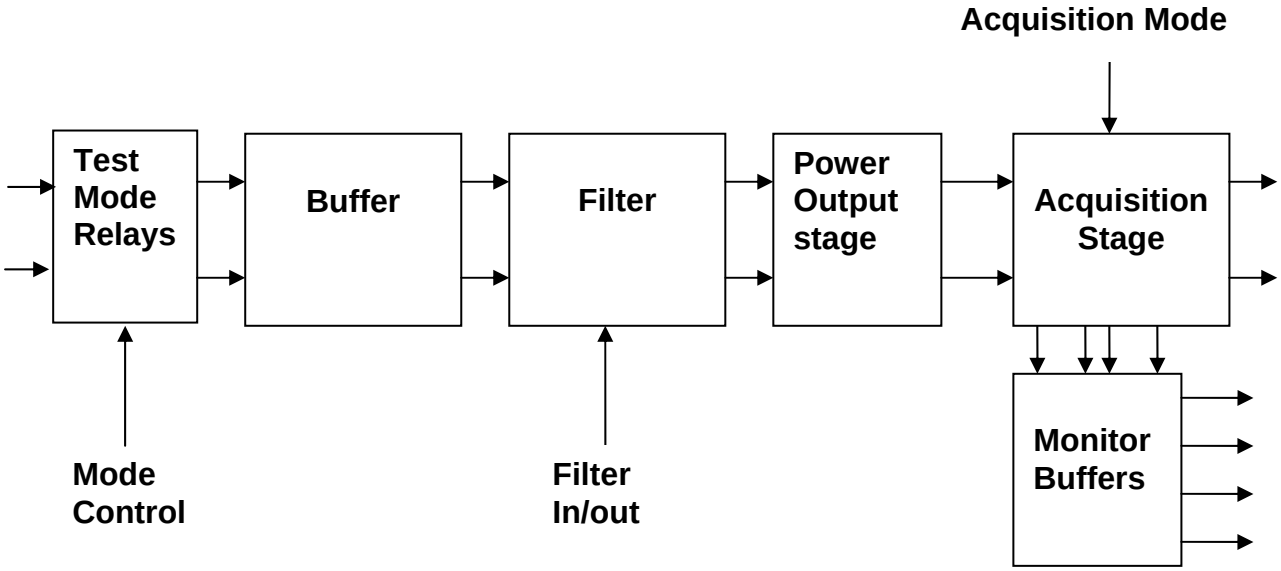
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

Contents

Block diagram



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The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

2. Test equipment

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Agilent Dynamic Signal Analyser (or similar)
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Relay test box

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Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Regulator (LM2990S) was noisy and has been replaced.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

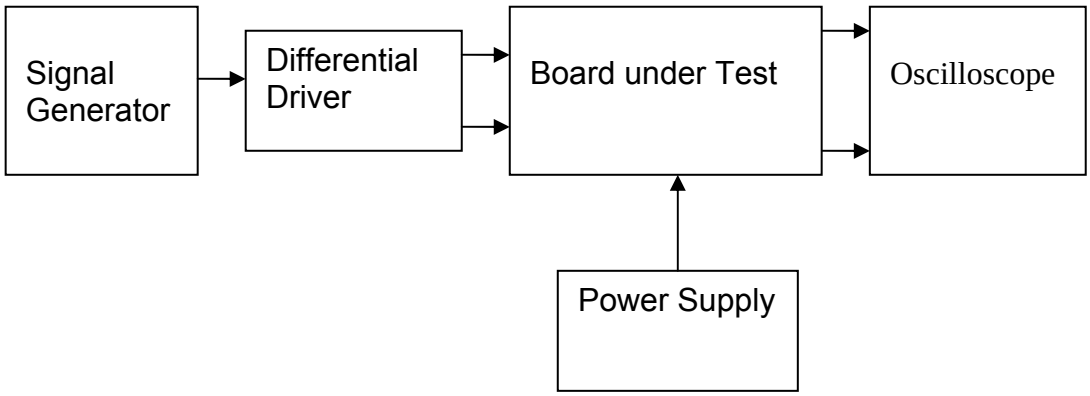
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.93V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.3	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.6	-30dB	-27dB	√
Ch3	-29.0	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …16/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P74….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

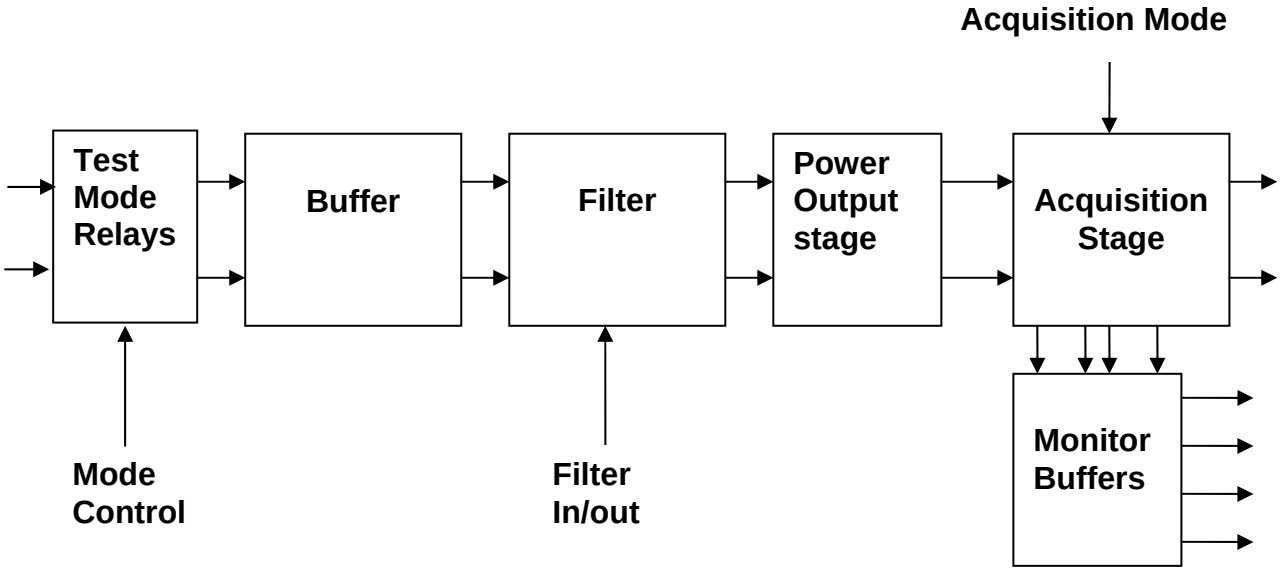
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P75….Serial No ……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

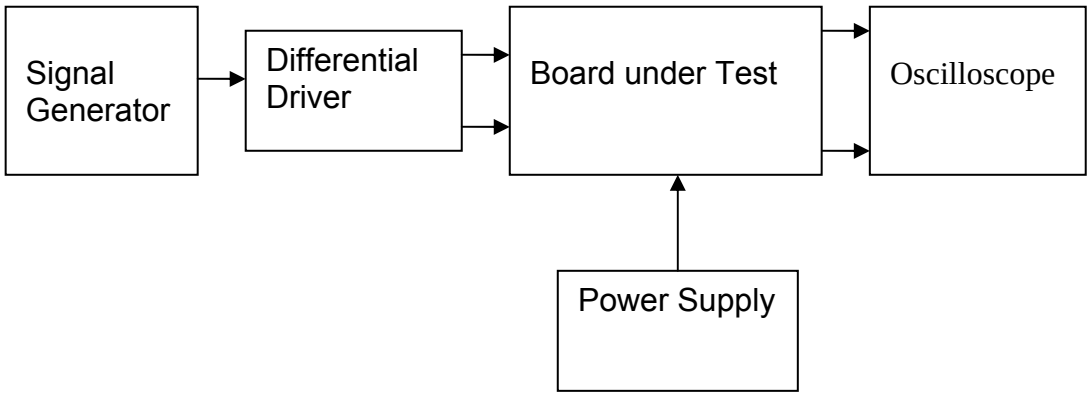
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P75….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-15.06V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.27A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	27mV	-40dB/25mV	-36dB/28mV	√
Ch2	27mV	-40dB/25mV	-36dB/28mV	√
Ch3	27mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.8	-42.5dB	-39.5dB	√
Ch4	-40.7	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.4	-53dB	-50dB	√
Ch2	-51.5	-53dB	-50dB	√
Ch3	-51.5	-53dB	-50dB	√
Ch4	-51.6	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-29.3	-30dB	-27dB	√
Ch2	-29.2	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-29.0	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.2	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.8	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.5	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.5	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P75….Serial No ……
Test Engineer …Simon Pyatt……
Date …21/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V		-22V		-22V		-22V	
-1v	-4.5V		-4.5V		-4.5V		-4.5V	
0v	0V		0V		0V		0V	
1v	-4.5V		-4.5V		-4.5V		-4.5V	
5v	-22V		-22V		-22V		-22V	

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

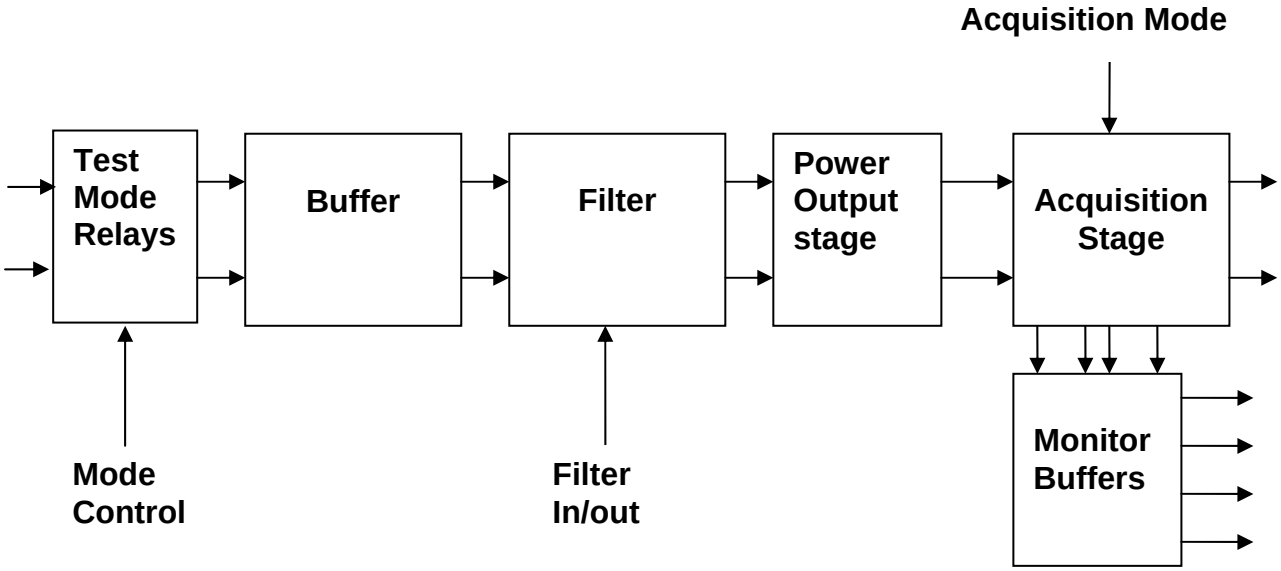
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

J7 not sitting flat on board, slightly lifted.

P2 mounted at an slight angle.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

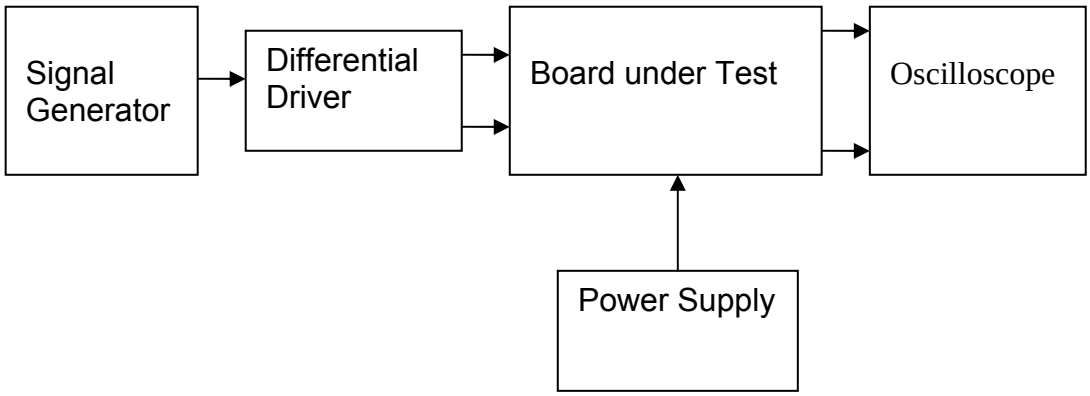
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.91V	√	1mV
-15v TP6	-14.95V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.9	-30dB	-27dB	√
Ch3	-28.9	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P76….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P77….Serial No ……
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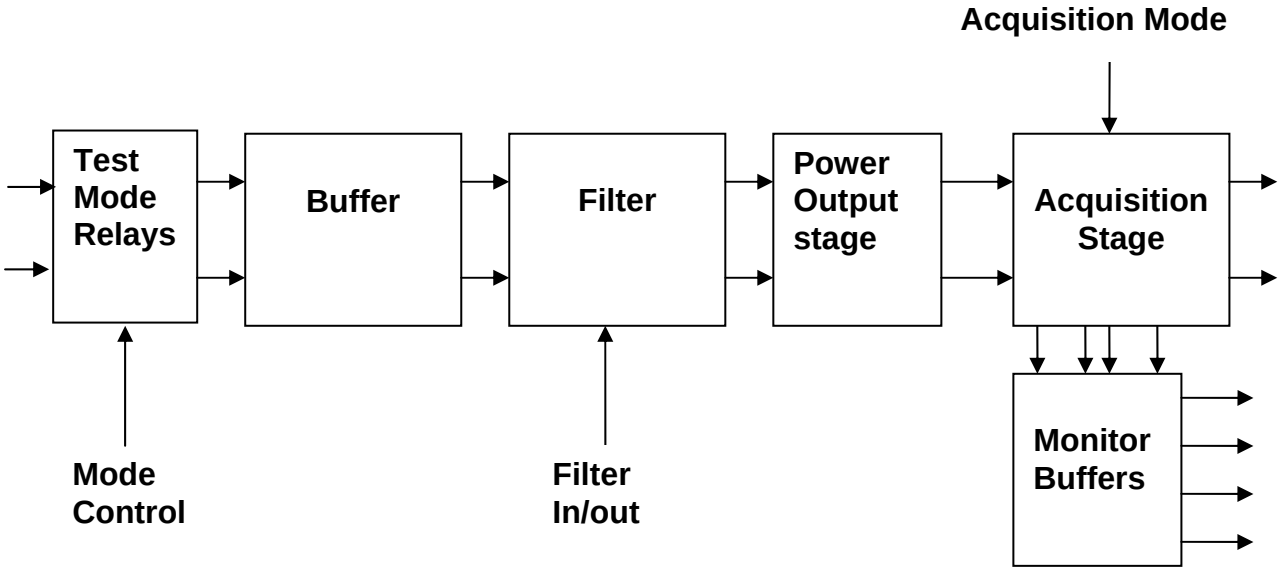
Block diagram



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This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

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The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P77….Serial No ……
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Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

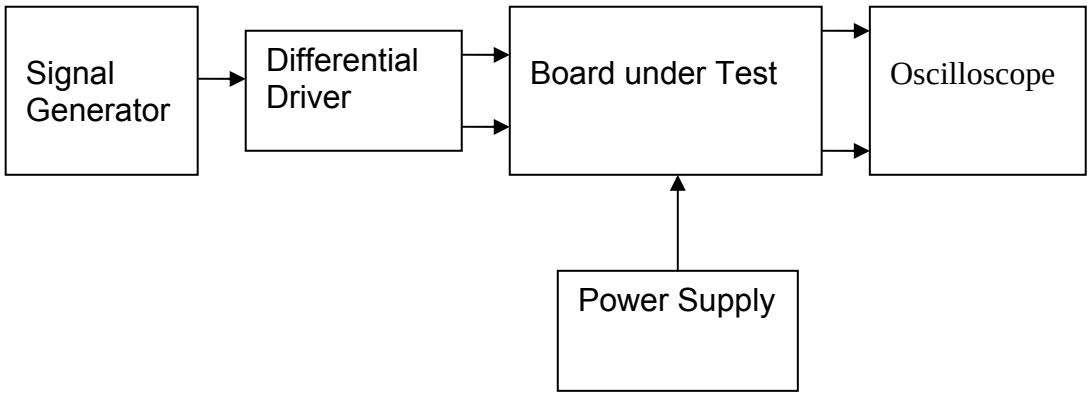
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



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J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
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J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.97V	√	1mV
-15v TP6	-15.02V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1		-40dB/25mV	-36dB/28mV	√
Ch2		-40dB/25mV	-36dB/28mV	√
Ch3		-40dB/25mV	-36dB/28mV	√
Ch4		-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.4	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.9	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …22/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P77….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	-22V	√	-22V	√	-22V	√	-22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

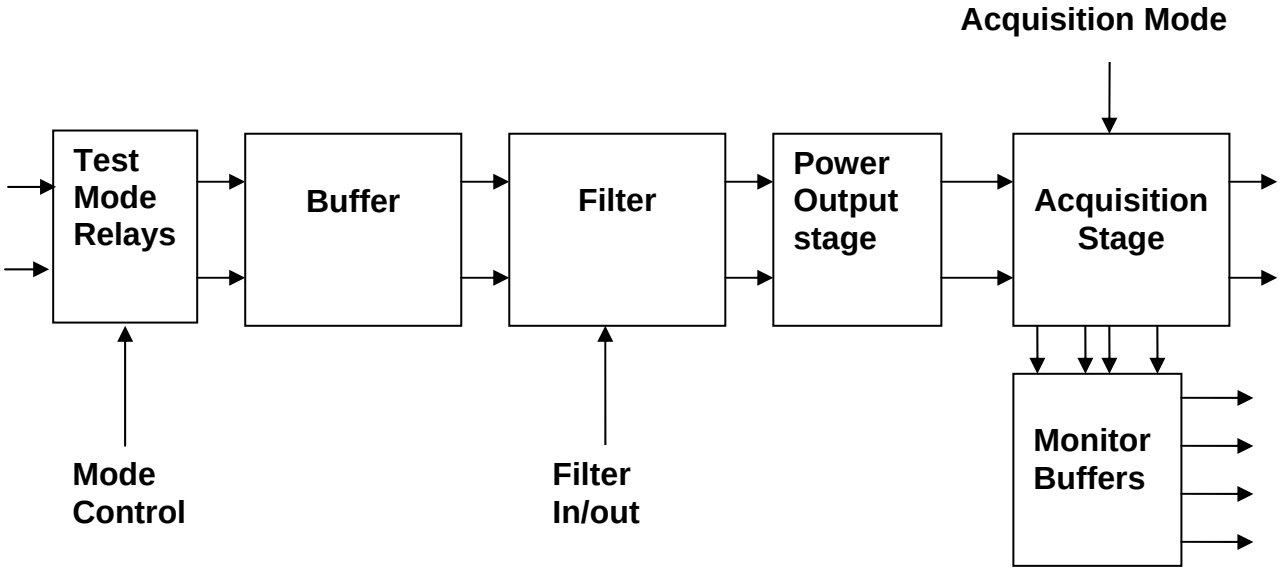
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is bowed.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

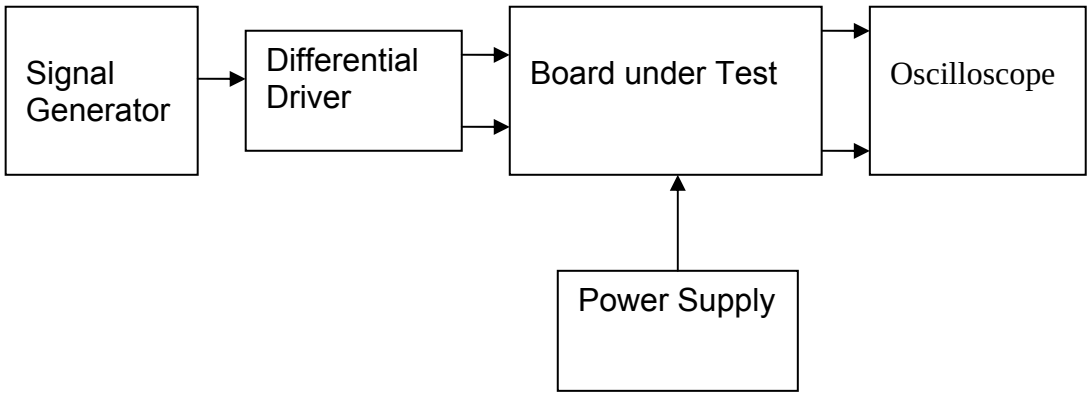
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-15.07V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.0	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.6	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	√
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P78….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

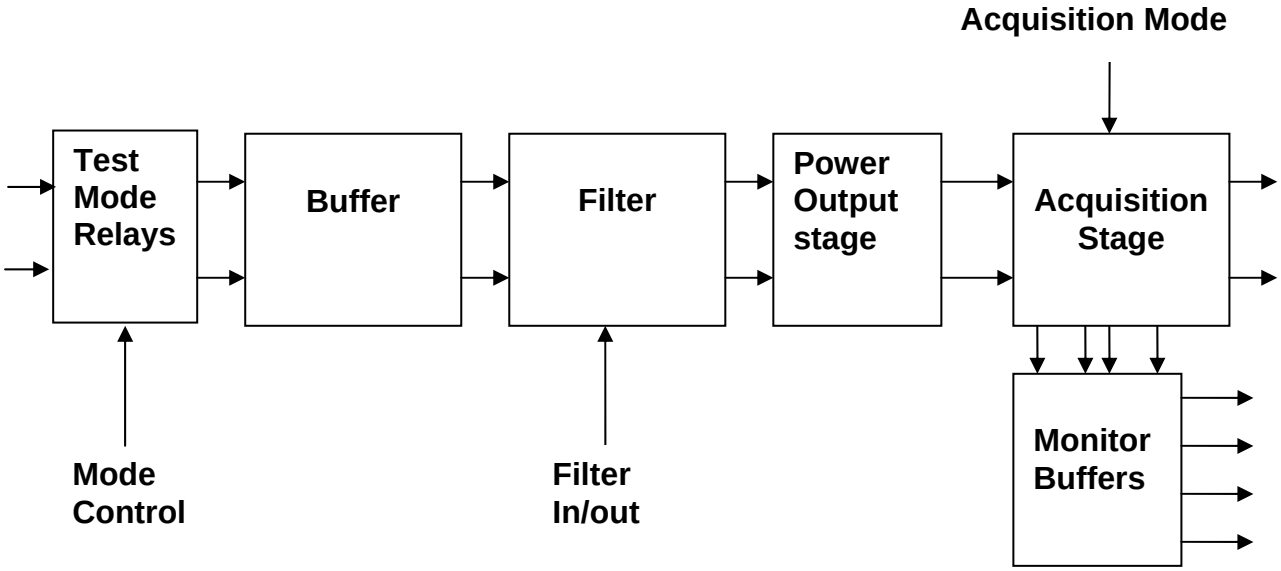
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	**Digimess**	**BP3002**	**211259**
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Signal Analyser	**N/A**	**N/A**	**N/A**
Diff driver circuit	**N/A**	**N/A**	**N/A**
Relay test box	**N/A**	**N/A**	**N/A**
Power supply	**Digimess**	**BP3002**	**211259**

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

P2 mounted at a slight angle.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

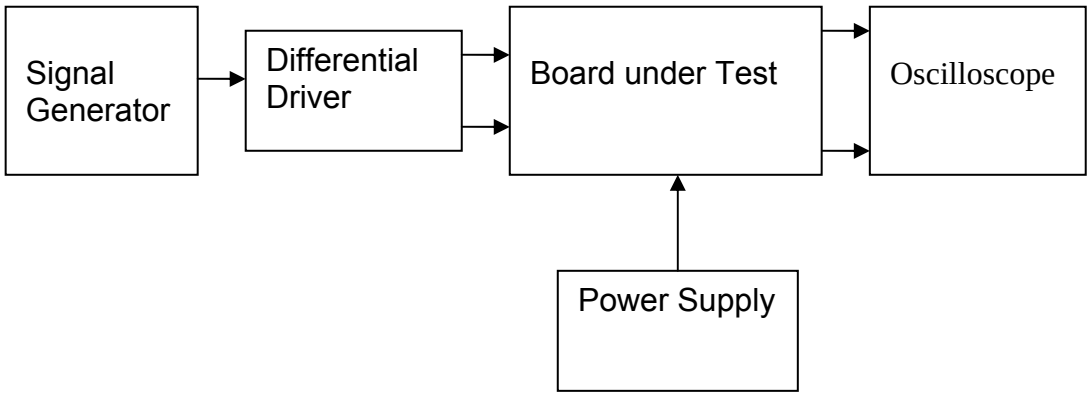
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05V	√	1mV
+15v TP4	14.95V	√	1mV
-15v TP6	-14.92V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.7	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-29.1	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.5	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch2	-4.9	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P79….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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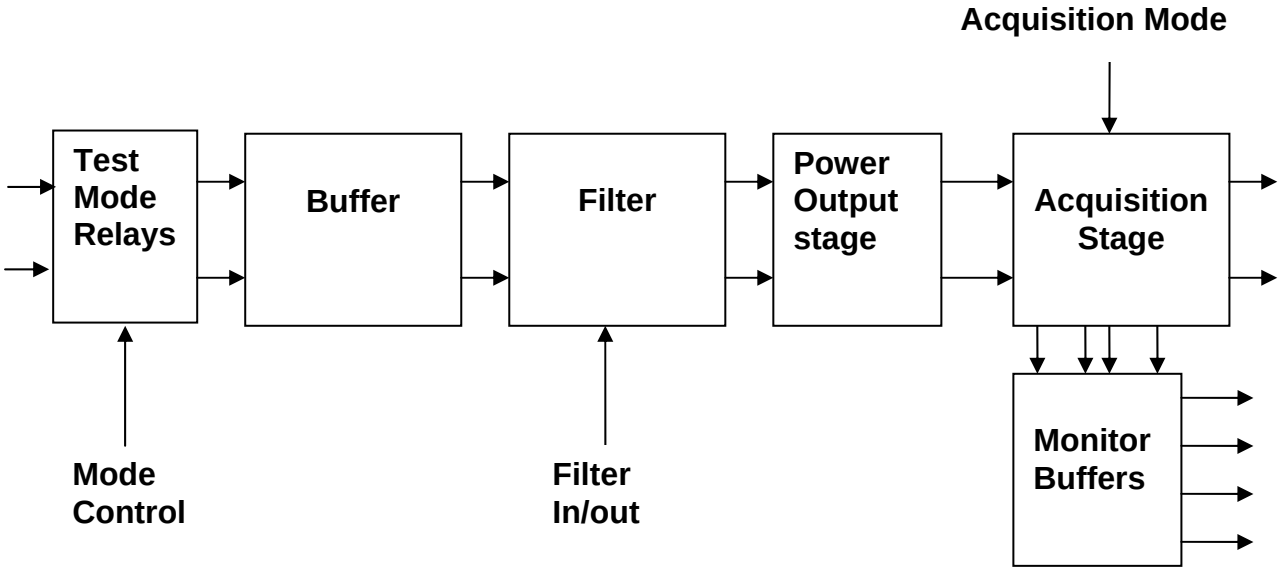
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

Contents

Block diagram



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Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
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The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

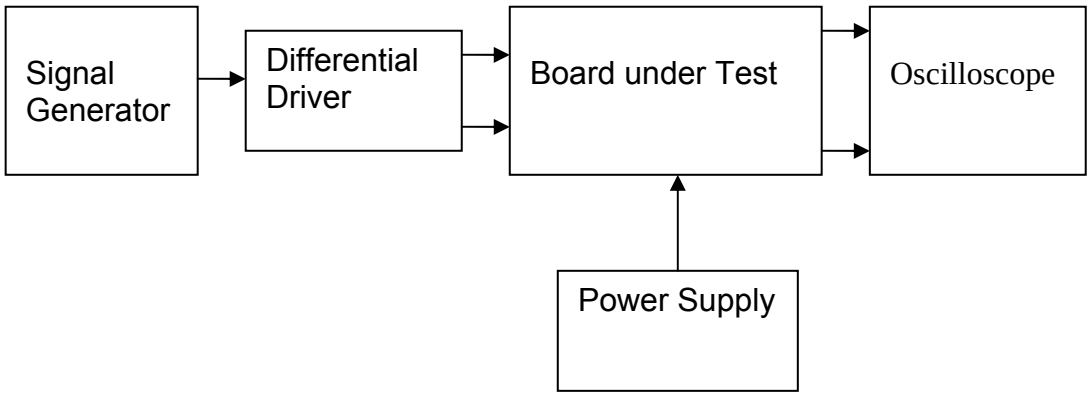
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

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Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.90V	√	1mV
-15v TP6	-14.96V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …23/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.5	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.7	-30dB	-27dB	√
Ch2	-28.5	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P80….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

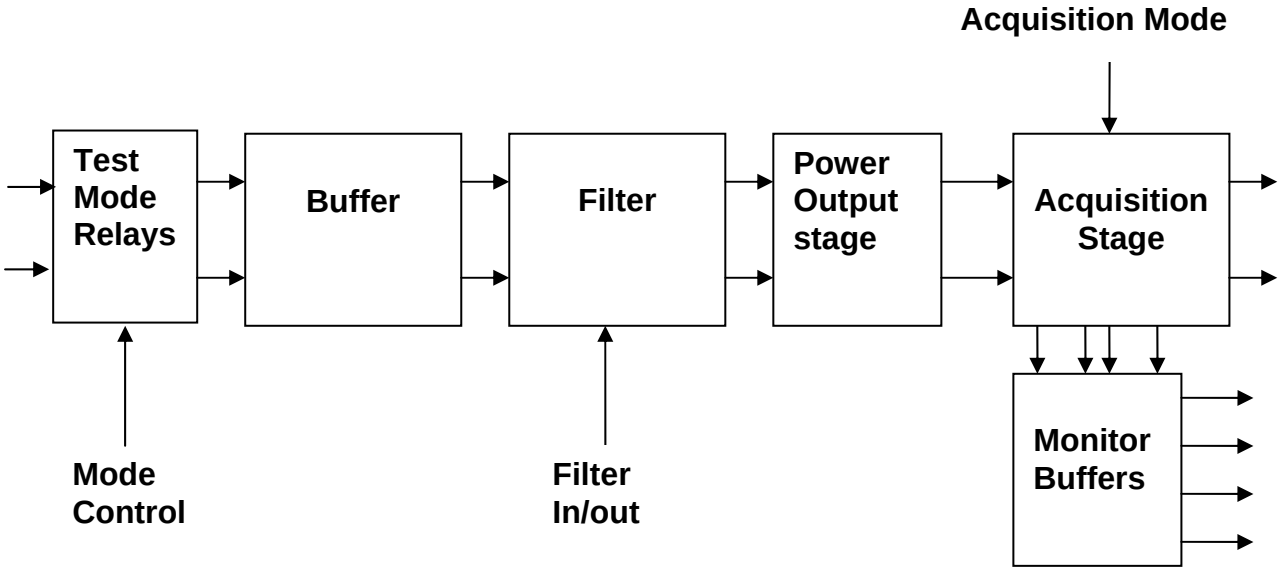
http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Board is slightly bowed.

J3 connector was of the wrong gender, component has been replaced.

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

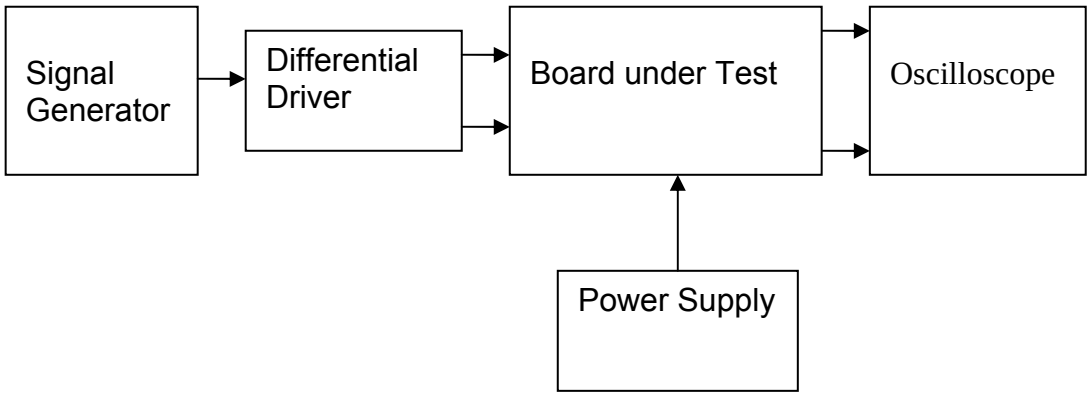
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P81….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.06V	√	1mV
+15v TP4	14.94V	√	1mV
-15v TP6	-14.87V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	27mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.5	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.5	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.1	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.1	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.8	-30dB	-27dB	√
Ch4	-28.8	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.6	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P81….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T1000125-v1 Advanced LIGO UK March 2010

Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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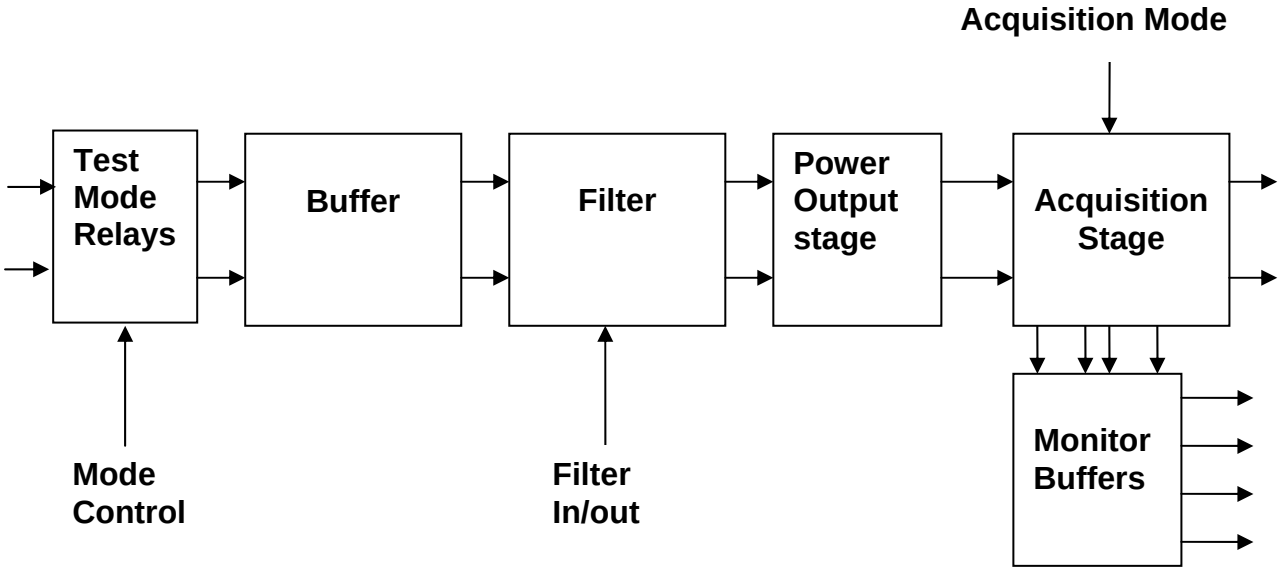
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	Digimess	BP3002	211259
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

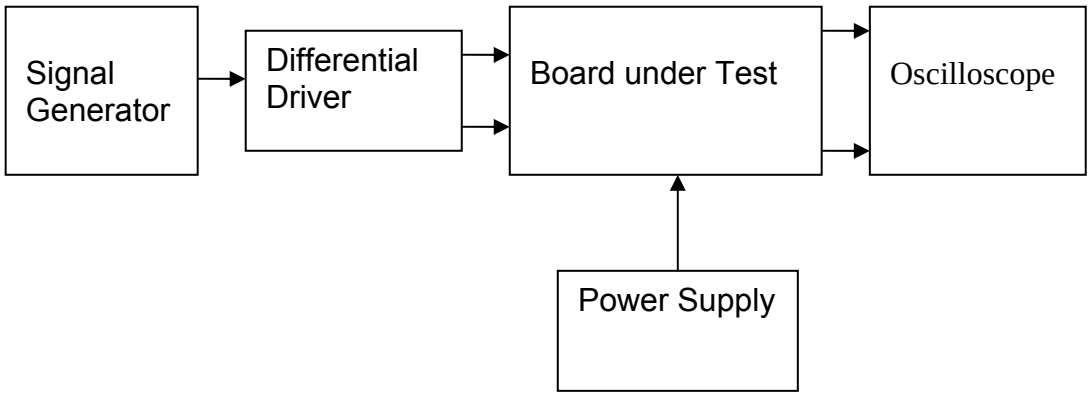
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02V	√	1mV
+15v TP4	14.90V	√	1mV
-15v TP6	-14.97V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P82….Serial No ……
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.6	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.6	-42.5dB	-39.5dB	√
Ch4	-40.6	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.3	-53dB	-50dB	√
Ch2	-51.1	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.2	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.9	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …24/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.1	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.5	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.4	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.4	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.0	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P82….Serial No ……
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11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P82….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

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LIGO- T1000125-v1 Advanced LIGO UK March 2010

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http://www.ligo.caltech.edu/

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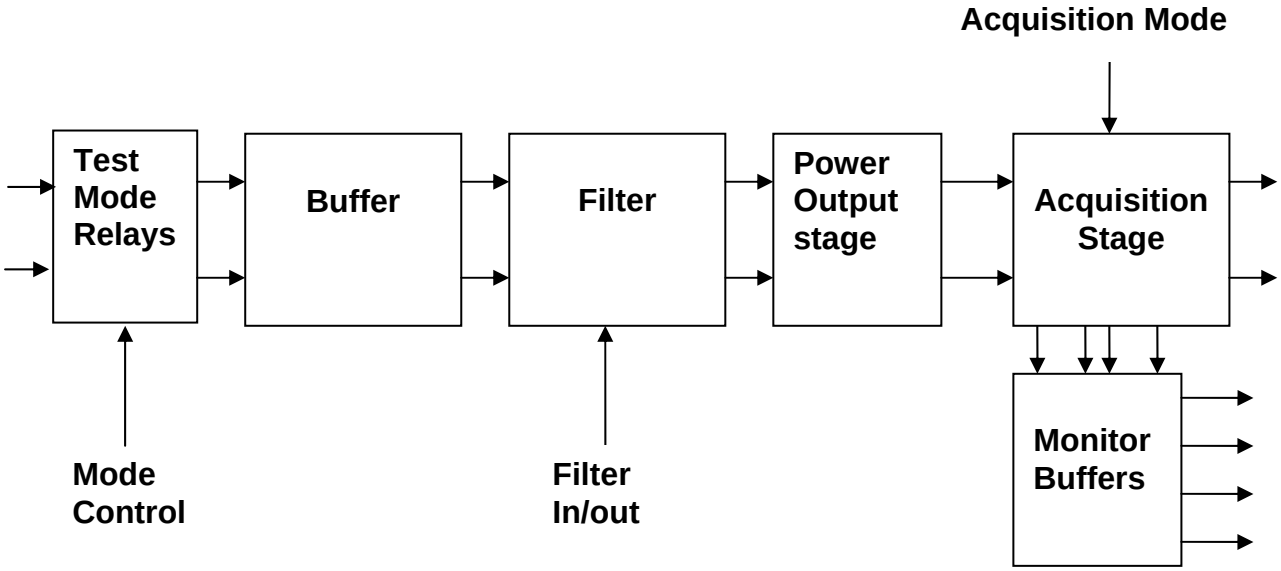
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

Contents

Block diagram



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The filter may be switched in and out by command as required under relay control.

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The outputs to the monitor board are buffered by unity gain voltage followers.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
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Relay test box

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Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Signal Analyser	N/A	N/A	N/A
Diff driver circuit	N/A	N/A	N/A
Relay test box	N/A	N/A	N/A
Power supply	Digimess	BP3002	211259

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

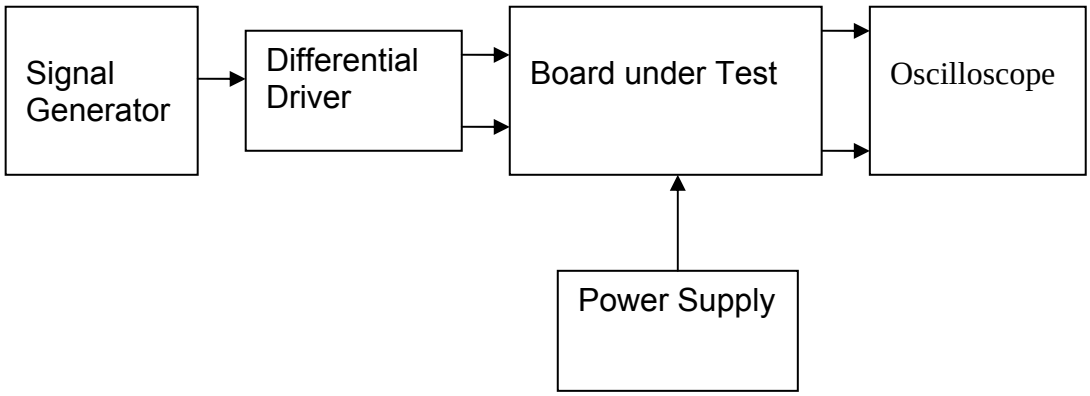
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…T_ACQ_P83….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08V	√	1mV
+15v TP4	14.89V	√	1mV
-15v TP6	-15.03V	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.28A
-16.5v	0.23A

If the supplies are correct, proceed to the next test.

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.19V	Pin 1 to Pin 2	2.19V	√
2	2.19V	Pin 5 to Pin 6	2.19V	√
3	2.19V	Pin 9 to Pin 10	2.19V	√
4	2.19V	Pin 13 to Pin 14	2.19V	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28V	Pin 3 to Pin 4	0.28V	√
2	0.28V	Pin 7 to Pin 8	0.28V	√
3	0.28V	Pin 11 to Pin 12	0.28V	√
4	0.28V	Pin 15 to Pin 16	0.28V	√

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.7	-42.5dB	-39.5dB	√
Ch2	-40.6	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.8	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.2	-53dB	-50dB	√
Ch4	-51.3	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.8	-30dB	-27dB	√
Ch2	-28.8	-30dB	-27dB	√
Ch3	-28.7	-30dB	-27dB	√
Ch4	-28.6	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.4	-21dB	-18dB	√
Ch2	-19.4	-21dB	-18dB	√
Ch3	-19.4	-21dB	-18dB	√
Ch4	-19.4	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.2	-21dB	-18dB	√
Ch2	-19.2	-21dB	-18dB	√
Ch3	-19.2	-21dB	-18dB	√
Ch4	-19.2	-21dB	-18dB	√

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.3	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.0	-6dB / 570mV	-4dB / 565mV	√
Ch4	-4.9	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch2	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch3	-3.7	-4.5dB / 665 mV	-2.5dB / 672mV	√
Ch4	-3.6	-4.5dB / 665 mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.6	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	3.3V	0.6V
Ch2	3.3V	0.6V
Ch3	3.3V	0.6V
Ch4	3.3V	0.6V

Unit…T_ACQ_P83….Serial No ……
Test Engineer …Simon Pyatt……
Date …25/06/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable?	Ch2 o/p	Ch2 stable?	Ch3 o/p	Ch3 stable?	Ch4 o/p	Ch4 stable?
-5v	-22V	√	-22V	√	-22V	√	-22V	√
-1v	-4.5V	√	-4.5V	√	-4.5V	√	-4.5V	√
0v	0V	√	0V	√	0V	√	0V	√
1v	4.5V	√	4.5V	√	4.5V	√	4.5V	√
5v	22V	√	22V	√	22V	√	22V	√

LIGO Laboratory / LIGO Scientific Collaboration

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Triple Acquisition Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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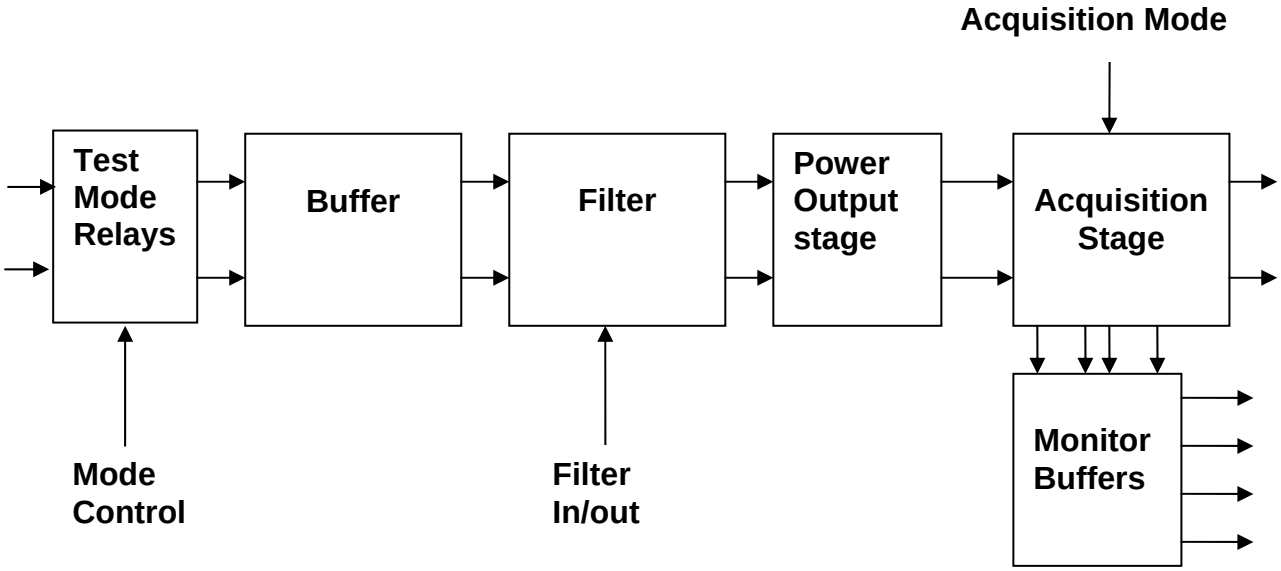
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

Contents

Block diagram



1. Description

Each Acquisition board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block is a unity gain buffer.

The third block contains a switchable filter. When the filter is switched in the corner frequency is 1Hz, with a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off.
At higher frequencies the signal is boosted by the input network to give the required dynamic range at high frequencies.
The filter may be switched in and out by command as required under relay control.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. This stage has a gain of 2.21, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The inputs of the power driver are protected by a resistor network.

The acquisition stage is used when a high coil current is required. In acquisition mode, the output resistors are bypassed by a low value resistor in series with a bank of capacitors, facilitating a high ac output current.
The outputs to the monitor board are buffered by unity gain voltage followers.

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	115	
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
V/I calibrator	Time Electronics	1044	

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

3. Inspection

Workmanship
Inspect the general workmanship standard and comment: √

Links:
Check that the link W4 is in place on each channel.

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5

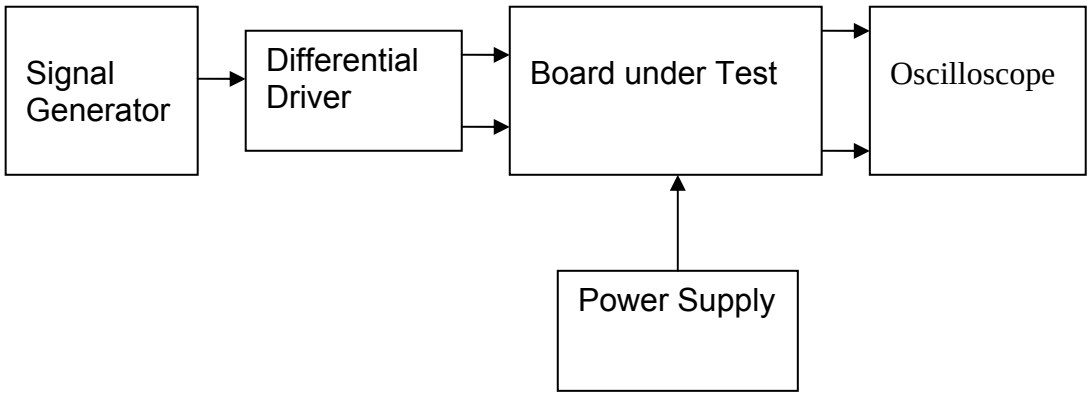
PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box

J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the differential driver.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:
Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11, 12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……T_ACQ_P85…….. ….Serial No ……
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6. Power

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the regulator output voltages, measured on a DVM with 4 or more digits.
Observe the regulator outputs on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.02	√	1mV
+15v TP4	14.96	√	1mV
-15v TP6	-15.11	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	225mA
-16.5v	300mA

If the supplies are correct, proceed to the next test.

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

7. Relay Operation

Note: 37- way to 25-way adapter cables are needed if the PUM test box is being used.

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

8. Outputs to Monitors

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s (704mVPP) input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP4 and TP5.
Measure the current monitor outputs and compare with the voltage between the outputs of R10 and R11. Repeat for each channel.

8.1 Voltage Monitors

Ch.	Output: TP4 to TP5	Monitor Pins P1	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	2.2	Pin 1 to Pin 2	2.2	√
2	2.2	Pin 5 to Pin 6	2.2	√
3	2.2	Pin 9 to Pin 10	2.2	√
4	2.2	Pin 13 to Pin 14	2.2	√

8.2 Current monitors

Ch.	Output between R10 and R11	Monitor Pins	Monitor out Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.28	Pin 3 to Pin 4	0.28	√
2	0.27	Pin 7 to Pin 8	0.27	√
3	0.28	Pin 11 to Pin 12	0.28	√
4	0.28	Pin 15 to Pin 16	0.28	√

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel and switch in the filters. Measure the frequency response of each channel across the 20 Ohm loads using the dynamic signal analyser. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output.

0.1 Hz measurements with the signal generator and oscilloscope

0.1Hz

	Output	Simulation		Pass/Fail
	mV	Min	Max	
Ch1	26mV	-40dB/25mV	-36dB/28mV	√
Ch2	26mV	-40dB/25mV	-36dB/28mV	√
Ch3	26mV	-40dB/25mV	-36dB/28mV	√
Ch4	26mV	-40dB/25mV	-36dB/28mV	√

1Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-40.8	-42.5dB	-39.5dB	√
Ch2	-40.8	-42.5dB	-39.5dB	√
Ch3	-40.7	-42.5dB	-39.5dB	√
Ch4	-40.9	-42.5dB	-39.5dB	√

10Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-51.2	-53dB	-50dB	√
Ch2	-51.2	-53dB	-50dB	√
Ch3	-51.1	-53dB	-50dB	√
Ch4	-51.4	-53dB	-50dB	√

100Hz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-28.6	-30dB	-27dB	√
Ch2	-28.4	-30dB	-27dB	√
Ch3	-28.5	-30dB	-27dB	√
Ch4	-28.7	-30dB	-27dB	√

1 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.5	-21dB	-18dB	√
Ch2	-19.5	-21dB	-18dB	√
Ch3	-19.5	-21dB	-18dB	√
Ch4	-19.5	-21dB	-18dB	√

5 kHz

	Output	Simulation		Pass/Fail
	dB	Min	Max	
Ch1	-19.3	-21dB	-18dB	√
Ch2	-19.3	-21dB	-18dB	√
Ch3	-19.3	-21dB	-18dB	√
Ch4	-19.3	-21dB	-18dB	√

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

10. Frequency Response Test, Acquisition Mode: Switch the filters off and switch the Acquisition mode in for each channel. Connect a 20 Ohm load resistor across each channel. Either test the response using the signal generator with a 1v r.m.s input signal between TP1 and TP2 or use the dynamic signal analyzer.

1Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch2	-35.0	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch3	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√
Ch4	-34.9	-36.5dB / 20mV	-33.5dB / 16mV	√

10Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-18.2	-20dB / 122mV	-17dB / 118mV	√
Ch2	-18.3	-20dB / 122mV	-17dB / 118mV	√
Ch3	-18.1	-20dB / 122mV	-17dB / 118mV	√
Ch4	-18.1	-20dB / 122mV	-17dB / 118mV	√

100Hz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch2	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch3	-5.1	-6dB / 570mV	-4dB / 565mV	√
Ch4	-5.1	-6dB / 570mV	-4dB / 565mV	√

1 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch2	-3.8	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch3	-3.9	-4.5dB / 665mV	-2.5dB / 672mV	√
Ch4	-3.8	-4.5dB / 665mV	-2.5dB / 672mV	√

5 kHz

	Output	Simulation		Pass/Fail
		Min	Max	
Ch1	-3.7	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch2	-3.8	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch3	-3.9	-4.5dB / 675mV	-2.5dB / 665mV	√
Ch4	-3.8	-4.5dB / 675mV	-2.5dB / 665mV	√

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

11. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1 kHz. Use the 20 Ohm loads. Observe the voltage across each dummy load resistor with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……T_ACQ_P85…….. ….Serial No ……
Test Engineer…..Xen…….
Date……..…6/10/10……

12. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage using the scope between TP4 and TP5. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable?**	**Ch2 o/p**	**Ch2 stable?**	**Ch3 o/p**	**Ch3 stable?**	**Ch4 o/p**	**Ch4 stable?**
-5v	-22.0	√	-22.0	√	-22.0	√	-22.0	√
-1v	-4.5	√	-4.5	√	-4.5	√	-4.5	√
0v	0	√	0	√	0	√	0	√
1v	4.5	√	4.5	√	4.5	√	4.5	√
5v	22.0	√	22.0	√	22.0	√	22.0	√