LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

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AdL Quad Suspension UK Coil Driver Design Requirements		
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1 Introduction

1.1 Purpose

The purpose of this document is to outline the design requirements for UK portion of the electronics for the AdL Quad suspension. The requirements for the US portion of the electronics will be detailed in another document. The requirements detailed below are the result of modeling done over the past few months by Rana Adhikari with input from Peter Fritschel, Ken Strain and others. The details of the modeling can be found at:
http://www.its.caltech.edu/~rana/aLIGO/suselecreq.html

1.2 Precedence

The design requirements outlined in this document are specific to the design of the AdL Quad Suspension Coil Drivers. In addition to the requirements outlined below, the requirements outlined in LIGO document number T000053, "Universal Suspension Subsystem Design Requirements" must be met. In the event of a conflict between the requirements outlined in this document and the Universal DRD, the requirements in this document take precedence.

1.3 Assumptions

For the purposes of design, it can be assumed that the LIGO suspensions controls will provide input signals to the coil drivers with the following specifications:

- Voltage Range: +/-10V ($20V_{p-p}$)
- Noise Voltage: 100nV/√Hz over the frequency range of interest for the coil driver.

The LIGO suspension controls will also provide for monitoring of signals with a voltage range of +/-10V ($20V_{p-p}$). The LIGO suspension controls will be responsible for any whitening necessary to match the UK provided monitors into the ADCs. The LIGO-provided ADCs have the following specifications:

- Voltage Range: +/-10V ($20V_{p-p}$)
- Noise Voltage: 5uV/√Hz over the frequency range of interest for the coil driver.

2 Requirements

The requirements for each stage of the quad are detailed in the sections below. In general, each section contains requirements for dynamic range, noise, and operational modes specific to the stage. It has been assumed that the input referred noise being supplied to the UK electronics is 100nV/√Hz for all frequencies of interest. The US team is responsible for all filtering and signal conditioning necessary to achieve this. It has also been assumed that the input voltage range of the UK electronics is +/-10V, differential (20Vp-p between inputs terminals).

There is also a section that follows that details requirements common to all stages. The requirements in the

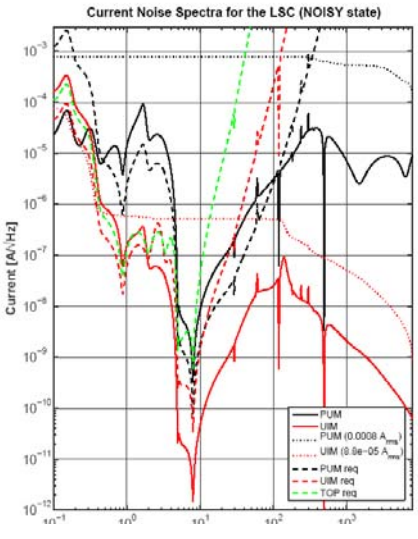

Figure 1: Noisy State

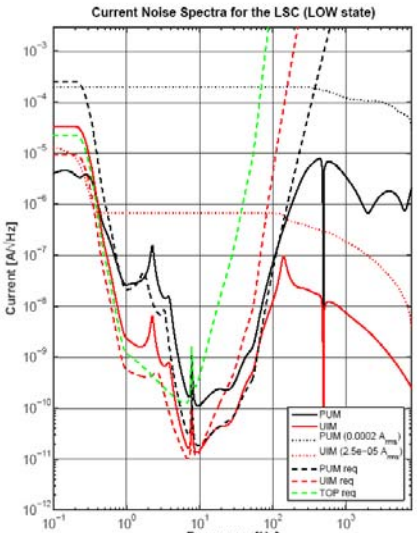

Figure 2: Low State

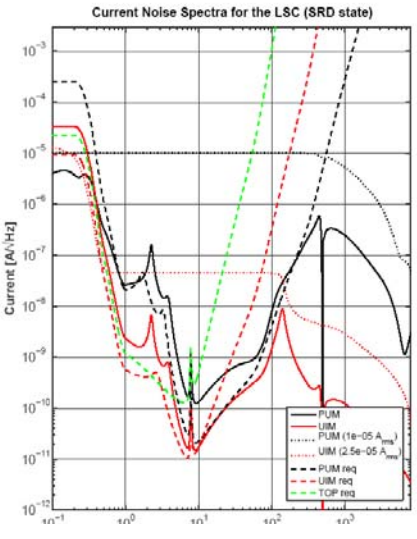

Figure 3: SRD State

sections below only show the output current requirements for the NOISY state and the noise requirements for the SRD state. The combinations of both of these requirements represent the extremes of the design. If it is determined that multiple pole/zero filtering is required to meet both designs, each stage of filtering shall be done in stages of 20dB of gain or attenuation. For example, 2 poles @ 3 Hz and 2 zeros @ 10 Hz in a single stage is acceptable, but a single pole at 3 Hz and a zero at 300 Hz has 40 dB of attenuation and would not be acceptable. Stages with complex poles and zeros and higher Q's will need to be discussed on a case by case basis.

2.1 Top Mass Requirements

The top mass requirements cover the 3 face coils, left, right and side coils for both the M0 and R0 stages.

2.1.1 Output Current

The maximum output current for each coil in the top stage shall be at least +/-200mA continuous. The requirement is almost completely driven by the need to statically align and position the suspension and correct for slow drifts.

2.1.2 Output Noise

The following is a table of the output noise requirements versus frequency.

Frequency	**Current Noise Requirement**
1 Hz	1 nA/√Hz
10 Hz	73 pA/√Hz
100 Hz	1000 nA/√Hz
1000 Hz	1000 nA/√Hz

2.2 Upper Intermediate Mass (UIM) Requirements

The UIM requirements cover the 4 coils used in the UIM. They are commonly referred to as UL, LL, UR and LR, denoting their relative positions.

2.2.1 Output Current

The maximum necessary output current predicated by the models in the NOISY state for the UIM is ~90uA_{rms}. Assuming a safety factor of 20 to cover transient events, the output current for each UIM coil driver should be at least 2mA_{rms}. As can be seen in Figure1 the UIM coil driver current is frequency dependent. For frequencies less than 1 Hz, the coil driver must be capable of supplying the full 2mA_{rms}, but the driver must also be capable of supplying currents of up to 16uA_{rms} (0.8uA x 20) for at 100Hz.

2.2.2 Output Noise

The following is a table of the output noise requirements versus frequency for SRD state.

Frequency	**Current Noise Requirement**
1 Hz	0.500 nA/√Hz
10 Hz	3 pA/√Hz
100 Hz	200 nA/√Hz
1000 Hz	1000 nA/√Hz

2.3 Penultimate Mass (PUM) Requirements

The PUM requirements cover the 4 coils used in the PUM. They are commonly referred to as UL, LL, UR and LR, denoting their relative positions.

2.3.1 Output Current

The maximum necessary output current predicated by the models in the NOISY state for the PUM is ~800uA$_{rms}$. Assuming a safety factor of 20 to cover transient events, the output current for each PM coil driver should be at least 16mA$_{rms}$. As can be seen in Figure1 the PUM coil driver current is frequency dependent. The driver must be capable of supplying currents of up to 16mA$_{rms}$ (800uA x 20) for frequencies from 200Hz to 5KHz.

2.3.2 Output Noise

The following is a table of the output noise requirements versus frequency for the SRD state.

Frequency	**Current Noise Requirement**
1 Hz	20 nA/√Hz
10 Hz	4 pA/√Hz
100 Hz	5 nA/√Hz
1000 Hz	1000 nA/√Hz

2.3.3 Operational Modes

The PUM coil drivers shall provide the following operating modes:

- RUN (low noise) - This is the nominal operating mode when the interferometer is locked. In this mode all of the noise and dynamic range requirements outlined in the sections above need to be met.
- Acquisition – This mode is used to lock the interferometer. In this mode of operation, the output noise requirements outlined above do not apply. The coil driver shall be capable of supplying at least 400mA peak currents during acquisition. If continuous currents of 400mA can damage the coils, fuses or other protection devices shall be incorporated into the design to prevent damage to the coils.

RUN and Acquire mode commands for all coil driver outputs in the PUM shall be ganged, i.e. all driver stages should respond to one mode switch command. The design of the mode switch shall be such that it does not cause an instantaneous change in the DC response (gain) or offset of the circuit.

2.4 Requirements Common to All Stages

2.4.1 Monitors

The following monitors shall be included for each coil driver output:

- Output voltage monitor- the output voltage monitor(s) shall be capable of covering the full dynamic range of the output, and additionally if a voltage source design is used, a monitor capable of seeing the noise floor of the output for 10Hz<freq<1KHz shall be included. Meeting these requirements may require multiple monitors. As an example, one low frequency monitor (freq<10Hz) could be used to measure the DC portion of the signal and an AC-coupled (whitened) monitor could be used for 10Hz<freq<1KHz.
- Output current monitor- There shall be monitors for the output current of each coil driver. One monitor shall be provided for fast (unfiltered), instantaneous measurement of the output current. One monitor of the RMS current with a time constant of 1 second shall be provided. An example of such a current monitor is included in the design of the LIGO LOS Coil Driver (D000325-C1). In this design the current through a 10 ohm resistor is measured using a differential amplifier. If a current source design is used for the coil driver there shall be a monitor provided that is capable of measuring the noise floor of the output for 10Hz<freq<1KHz. This monitor shall be capable of monitoring the full current range of the driver in all modes of operation.
- Status (position) monitors/read backs for all switches used in the design.

2.4.2 Mode Switches

In addition to the read back requirement outlined above all mode switches used in the design shall be capable of operating in less than TBD usec. This time shall be measured from the time the switch is commanded to operate until the time the operation is completed and includes all circuit delays and switch bounce.

2.4.3 Circuit Protection

He coil driver design shall incorporate fuses or other circuit protection devices to protect the coil from damage. In the past this has been done using slow blow fuses in the output. If fuses are used, there shall be some means of determining a blown fuse incorporated into the design. In the event of a blown fuse, the design of the driver should be such that fuse replacement can be accomplished in the field.

2.4.4 Test Inputs

The design shall incorporate test inputs for all coil driver channels. These test inputs shall be in parallel to the control input for each channel and will be used to inject signals into the circuit for transfer function measurements, troubleshooting and other operations while the coil driver is being bench tested and/or while the driver is installed in the control system. Connection of the test input signal to the circuit shall be made via an enable switch. The nominal position of this switch shall be such that the test signal is not connected to the circuit.