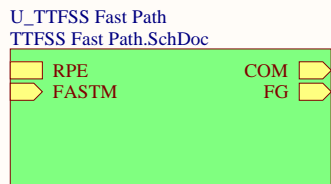
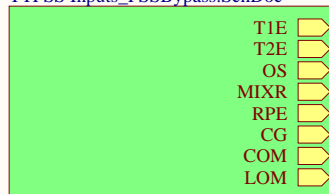
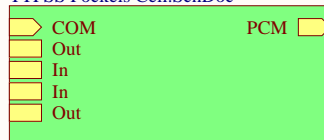


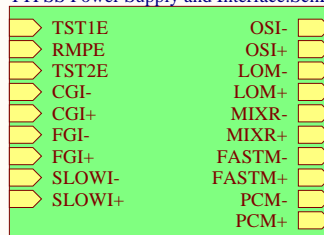
U_TTFSS Inputs_FSSBypass
TTFSS Inputs_FSSBypass.SchDoc



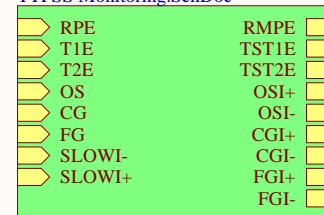
U_TTFSS Pockels Cell
TTFSS Pockels Cell.SchDoc



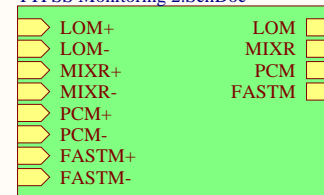
U_TTFSS Power Supply and Interface
TTFSS Power Supply and Interface.SchDoc



U_TTFSS Monitoring
TTFSS Monitoring.SchDoc



U_TTFSS Monitoring 2
TTFSS Monitoring 2.SchDoc



Captures modifications carried out for testing FSS/Ref Cav Bypass

Last Edited: 9/21/2018

Title **PSL TTFSS Bypass Overview**

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology



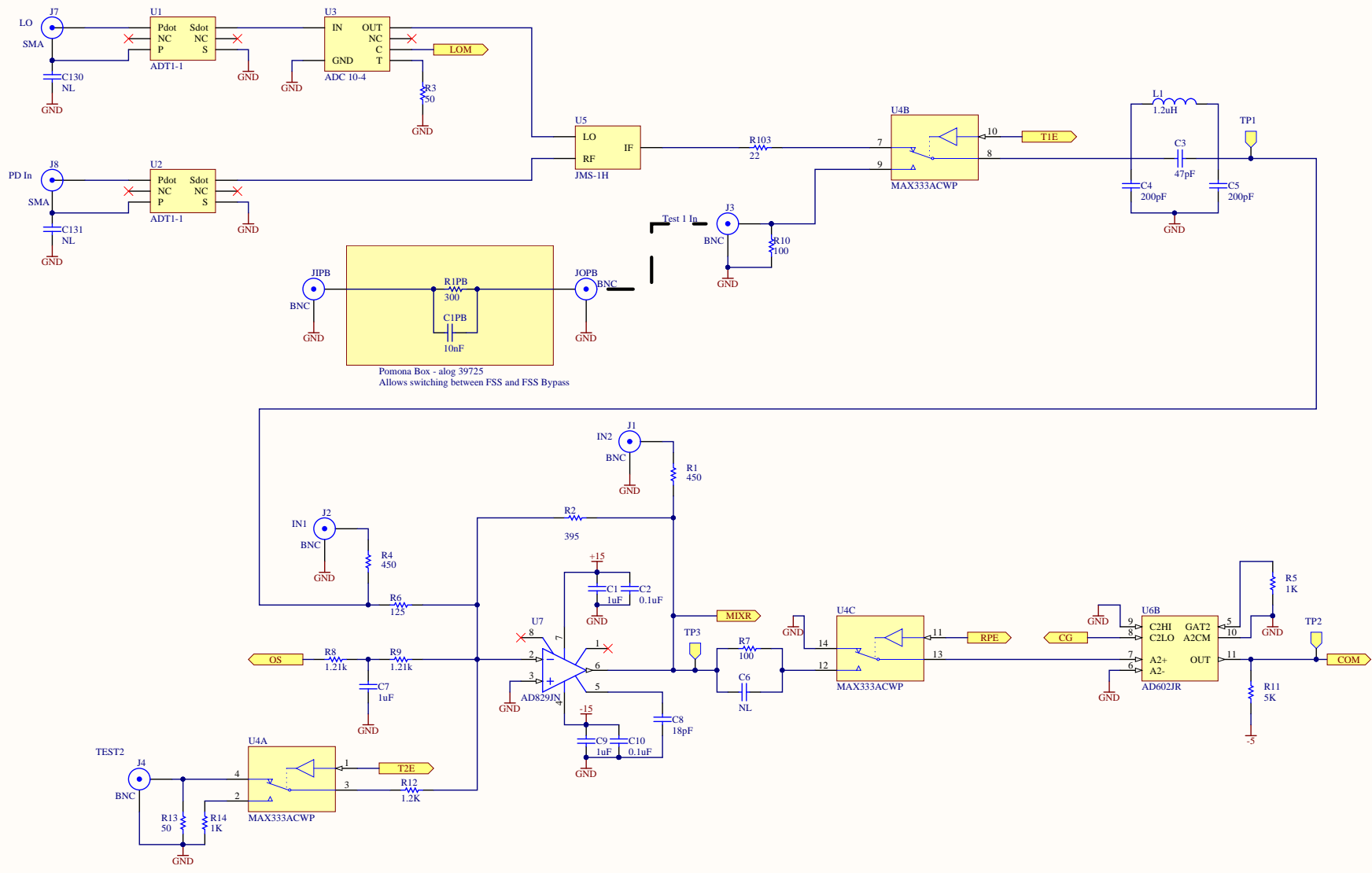
Size: A DCC Number: D040105 Revision: B Engineer: M. Laxen

Date: 9/26/2018
Time: 5:18:39 PM

Documentation Only - not for generating/laying out PCB

File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\FSS_Bypass.SchDoc

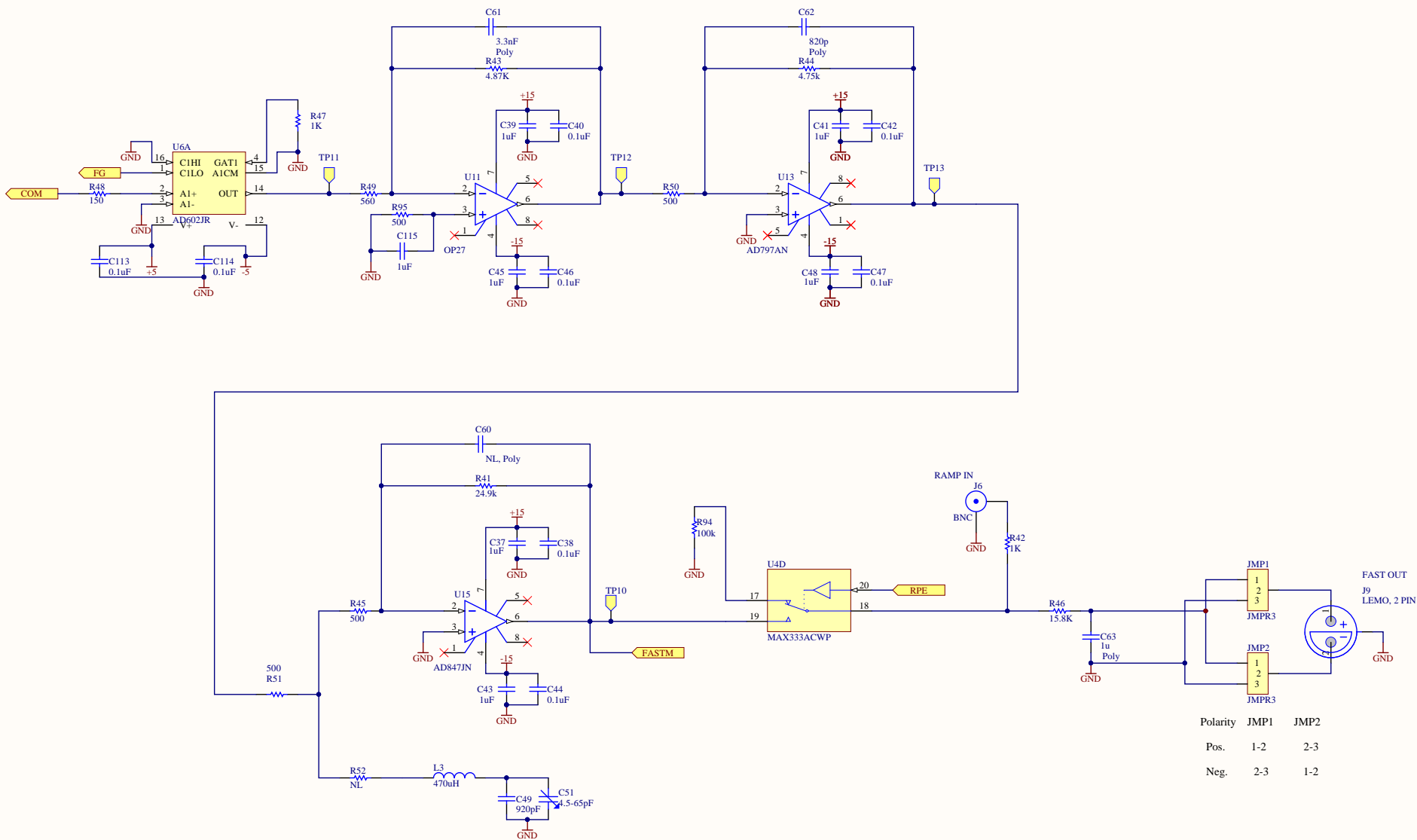
Sheet 1 of 7



Documentation Only - not for generating/laying out PCB

Last Edited: 9/21/2018

Title		PSL TFFSS Inputs with Bypass		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO	
Size: B	DCC Number: D040105	Revision: B	Engineer: M. Laxen	Date: 9/26/2018	Time: 5:18:39 PM		
File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\TFFSS Inputs_FSSBypass.SchDoc				Sheet 2 of 7			



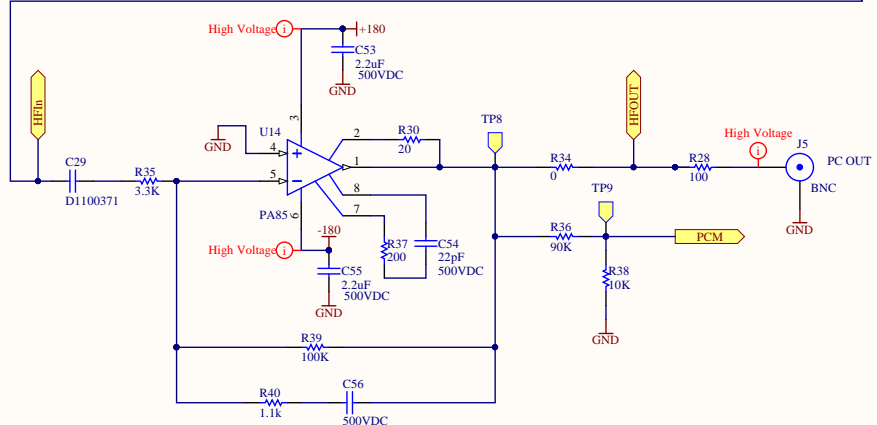
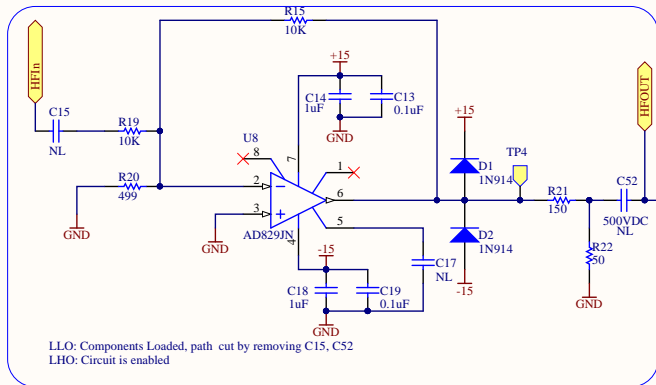
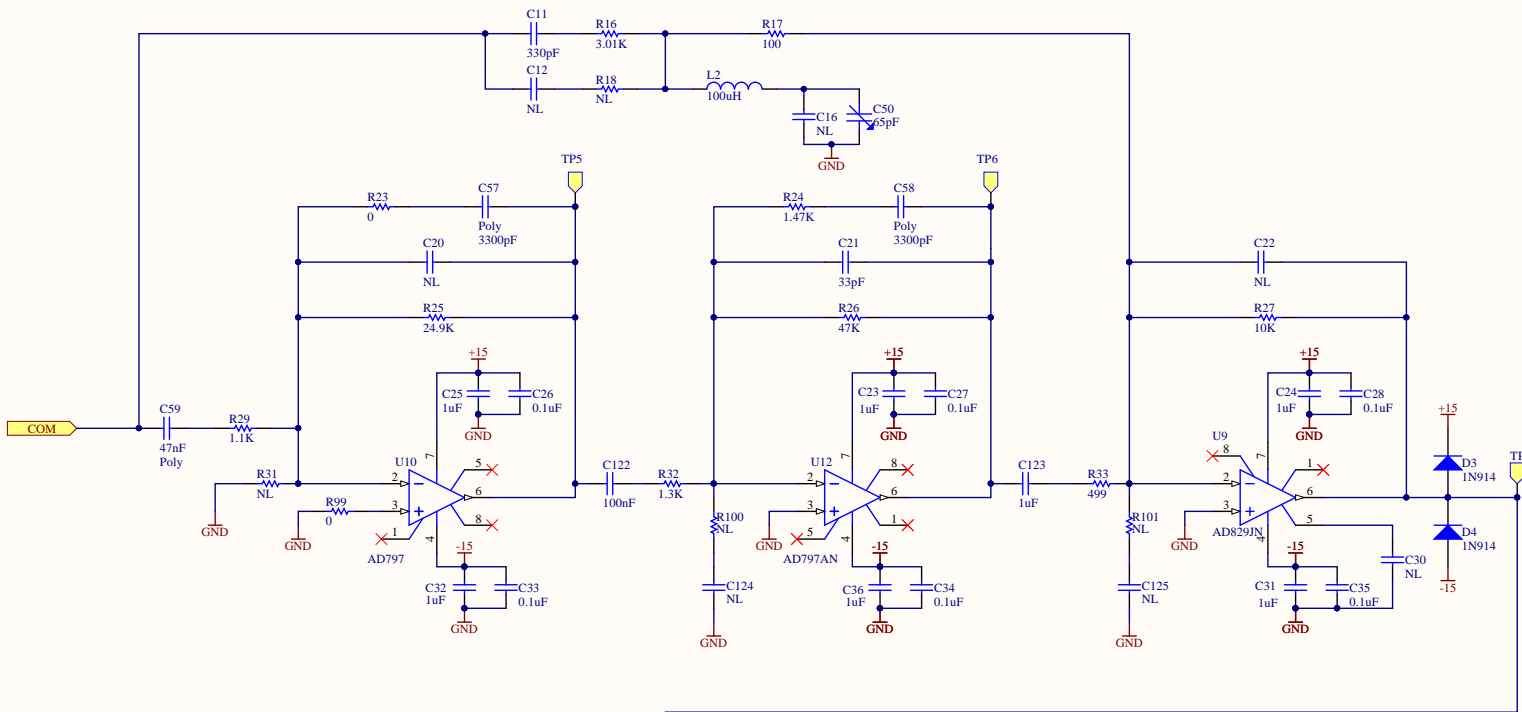
Documentation Only - not for generating/laying out PCB

Last Edited: 9/21/2018

Title PSL TFFSS Fast Path		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO [®]	
Size: B	DCC Number: D040105	Revision: B	Engineer: M.Laxen	Date: 9/26/2018	Time: 5:18:39 PM
File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\TFFSS Fast Path.SchDoc					

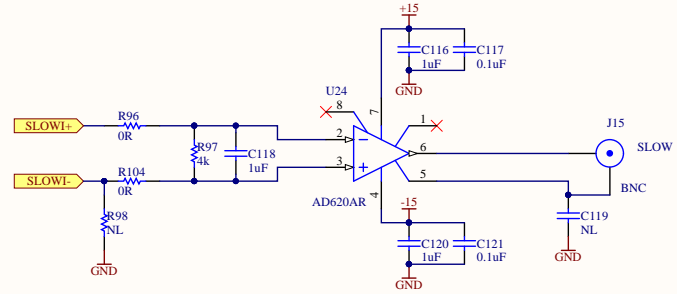
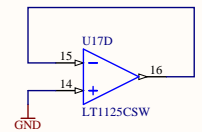
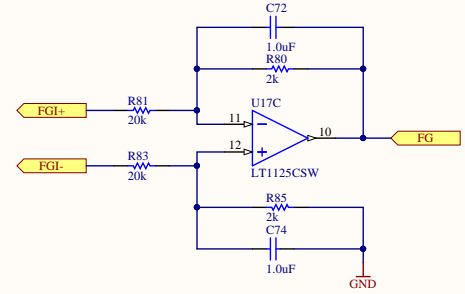
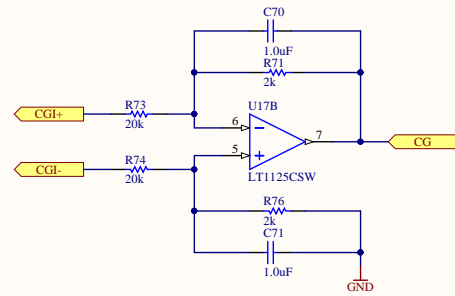
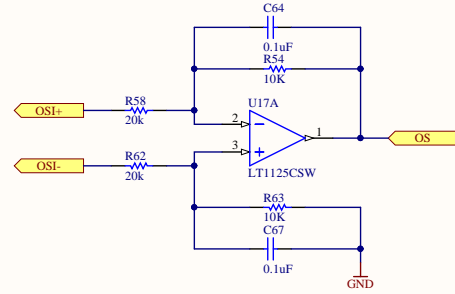
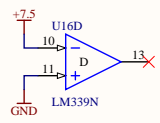
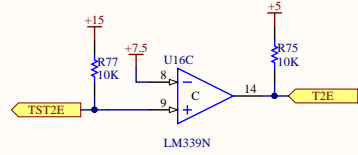
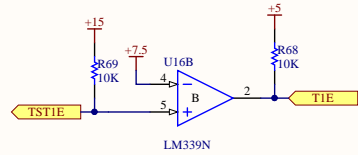
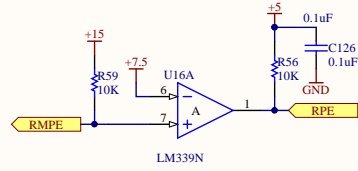
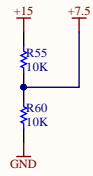
	JMP1	JMP2
Polarity	1-2	2-3
Pos.	1-2	2-3
Neg.	2-3	1-2

Sheet 3 of 7



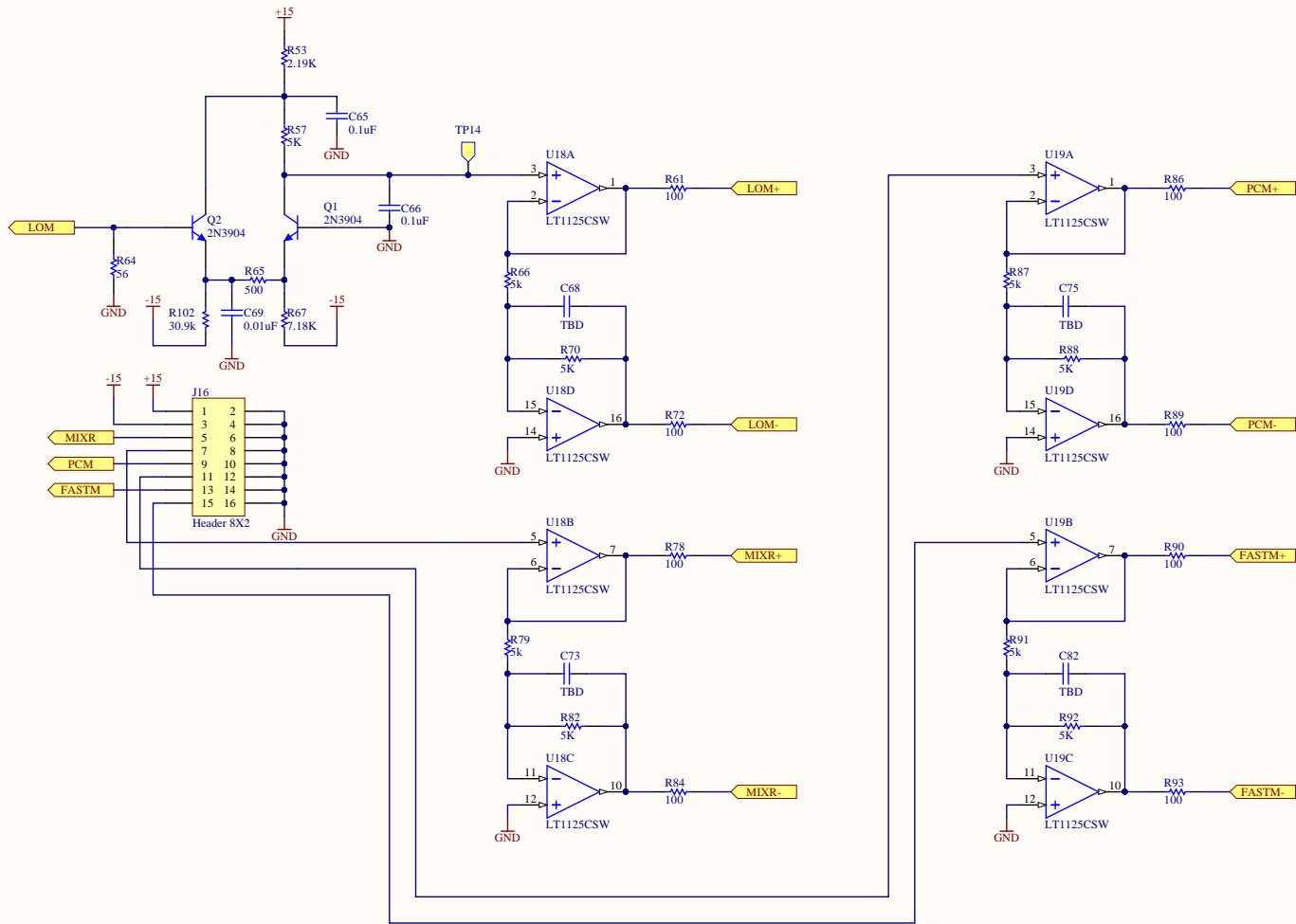
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Title		Last Edited: 9/21/2018	
PSL TTFSS Pockels Cell		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	
Size: B	DCC Number: D040105	Revision: B	Engineer: M. Laxen
File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\TTFSS Pockels Cell.SchDoc		Date: 9/26/2018	Time: 5:18:39 PM
		Sheet 4 of 7	



Documentation Only - not for generating/laying out PCB

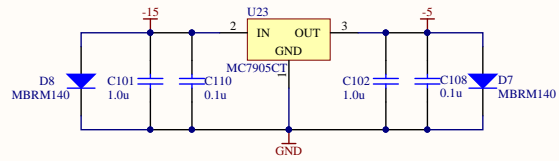
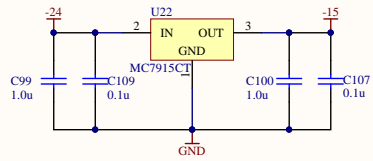
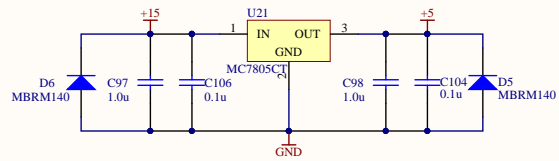
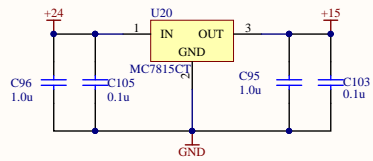
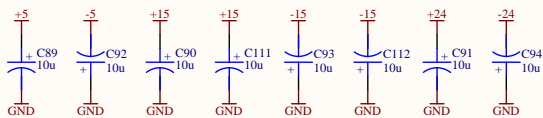
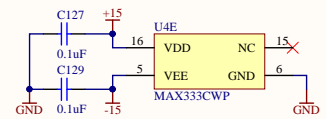
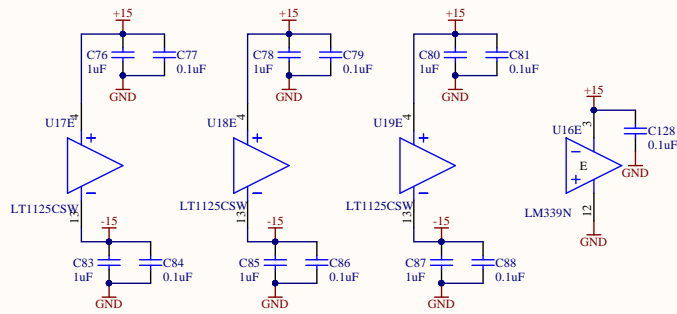
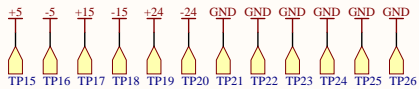
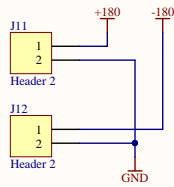
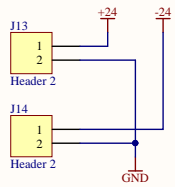
Title		Last Edited: 9/21/2018	
PSL TTFSS Monitoring		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	
Size: B	DCC Number: D040105	Revision: B	Engineer: M. Laxen
File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\TTFSS Monitoring.SchDoc		Date: 9/26/2018	Time: 5:18:39 PM
		Sheet 5 of 7	



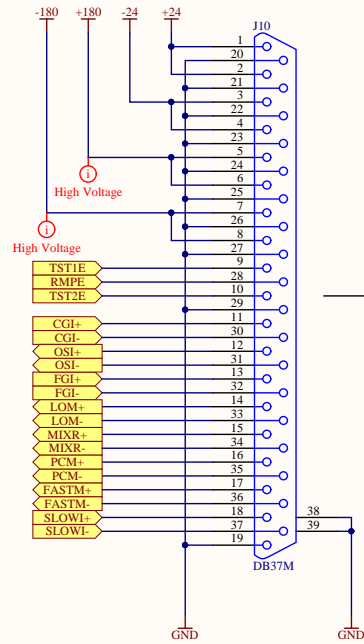
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Title		Last Edited: 9/21/2018	
PSL TTFFSS Monitoring 2		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	
Size: B	DCC Number: D040105	Revision: B	Engineer: M. Laxen
File: C:\Users\Public\Documents\Altium\Projects\FSS_Bypass\TTFFSS Monitoring 2.SchDoc		Date: 9/26/2018	Time: 3:18:39 PM
		Sheet 6 of 7	





D5, D6, D7, and D8 located on top of C104, C106, C108, and C110 respectively.



To FSS Interface Card / FieldBox D1100367