LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number T0900329-v1	July 7, 2009
ELIGO OMC Front End Controls Design Description		
R. Bork, J. Heefner		

California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

1   Introduction

1.1   Purpose

The purpose of this document is to present and describe the various components that are currently used in ELIGO OMC Front End (FE) systems. This document only covers the hardware and software systems associated directly with the front end system. Design details of the hardware and software specific to the OMC controls themselves are covered in other documents.

1.2   Front End (FE) System Block Diagram

The figure below is a simplified block diagram that shows an AdL FE system in relation to a FE CPU and the field devices.
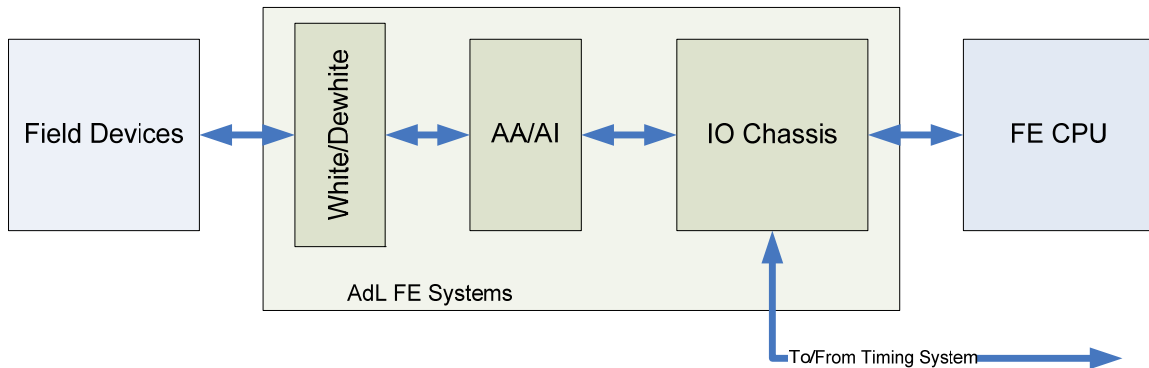

Figure 1: Block Diagram Showing AdL FE System

The basic building blocks used in AdL FE systems are:
- IO Chassis including commercial ADCs, DACs, Binary IO and other modules
- Anti-Alias (AA) and Anti-Image (AI) Filters
- Whitening/Dewhitening Filters

Each of these components is described in the appropriate sections below.

2   Front End System Component Description

2.1   IO Chassis

A block diagram of the IO Chassis is shown in the figure below. The diagram generically shows 2 ADCs and 2 DACs installed in the first 4 slots from the bottom. The actual cards and locations used in the ELIGO OMC controls are documented in the system schematics.
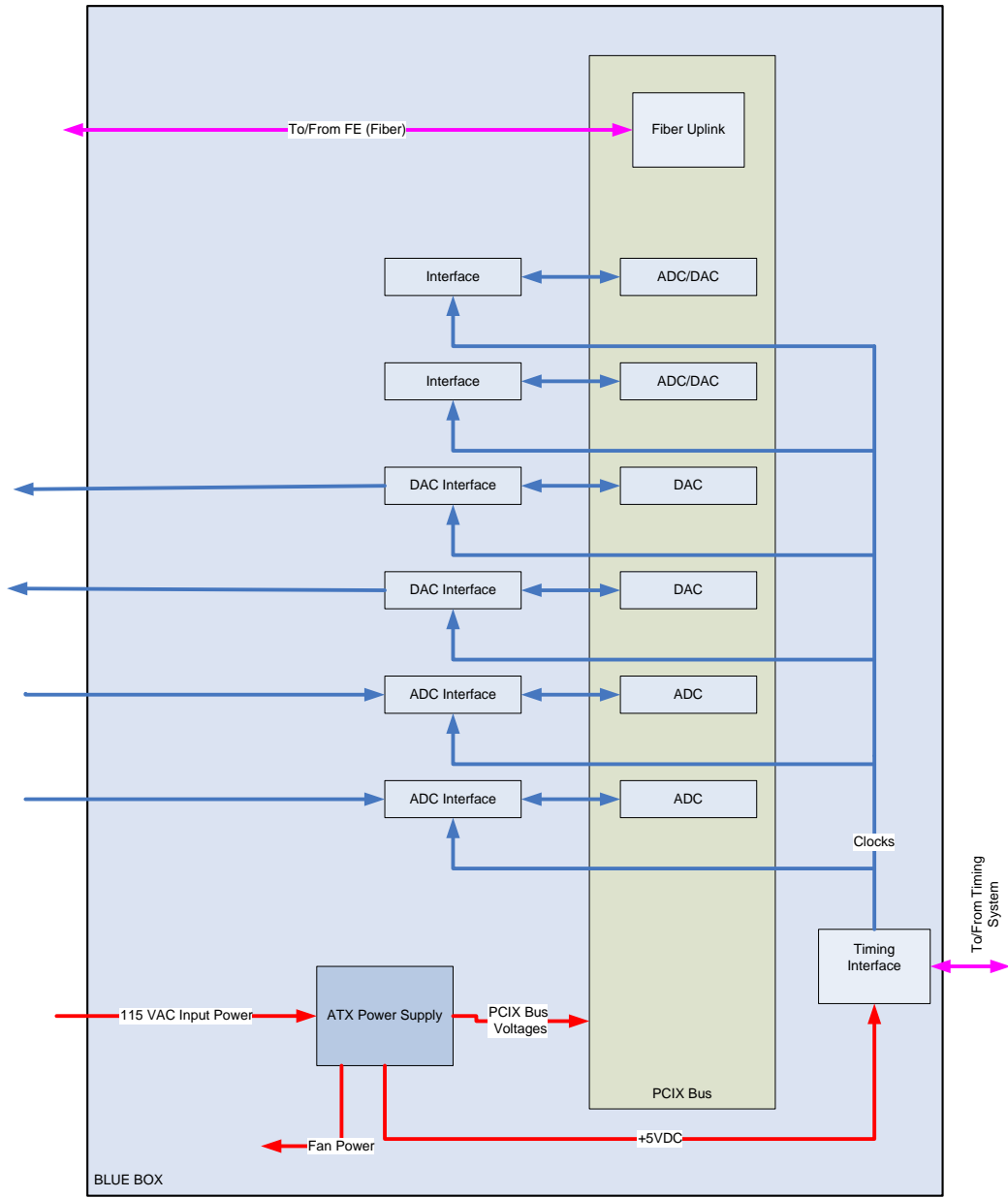
Figure 2:ELIGO OMC FE IO Chassis Block Diagram

A picture of an existing PCIX IO Chassis with some of the components labeled is shown in the figure below.
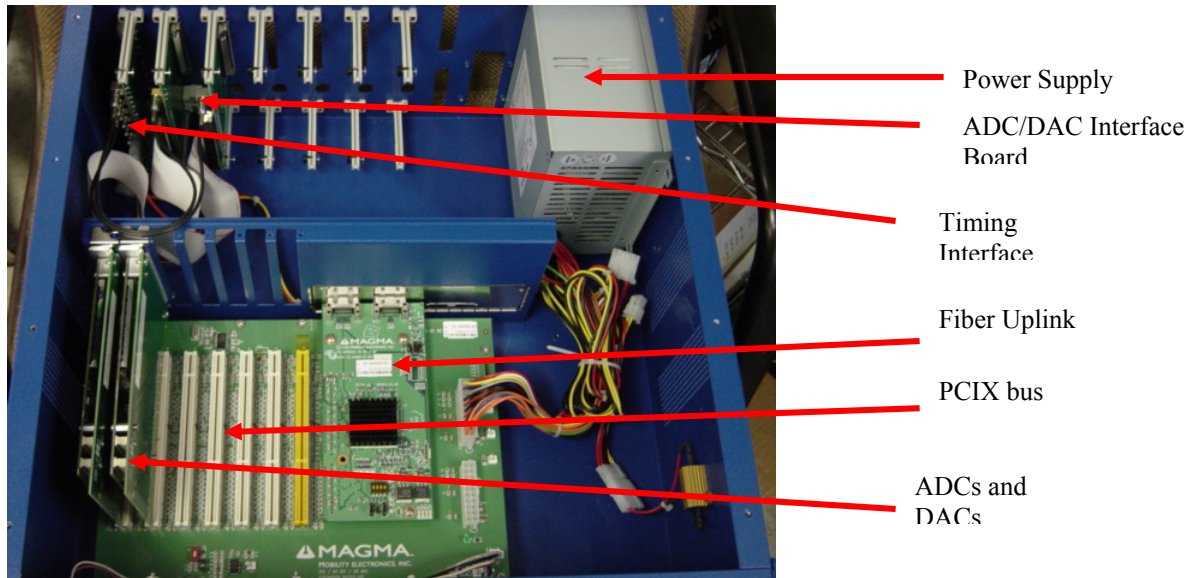
Power Supply

ADC/DAC Interface Board

Timing Interface

Fiber Uplink

PCIX bus

ADCs and DACs

Figure 3: PCIX IO Chassis

2.1.1 PCIX Bus

The IO chassis used in AdL prototype systems at CIT, LASTI and for the ELIGO OMC controls at LHO and LLO uses PCIX bus IO cards.

The datasheet for the PCIX bus board used in the IO chassis can be found at:
http://www.magma.com/products/board-sets/pdf/PE6NE.pdf

As can be seen from the block diagram in Figure 2 above the IO chassis is connected to the front end controls CPU via a fiber cable transmitter/receiver system supplied by Magma.

2.1.2 Timing Interface

The present AdL prototype and ELIGO systems use master and slave timing units designed and provided by LHO that interface to a clock fanout module mounted inside the IO chassis. The Timing Interface Module (D060064-00) takes the differential clock signals from the Master Timing System and converts them to TTL clock signals used by the ADCs and DACs. These signals are distributed inside the IO chassis using SMB cables from the Timing Interface Board to each of the ADC/DAC Interface Boards.

2.1.3 Commercial Modules

2.1.3.1 ADC

The ADC modules presently being used for AdL FE systems are the General Standards model PCI66-16AI64SSA-64-50M.

The datasheet for this module can be viewed at:
http://www.generalstandards.com/specs/pmc66_16ai64ssa_c_spec_092307.pdf

Note that the base module is actually a PMC bus module and can be used in PCIX and PCIe bus systems by attaching it to the appropriate adapter.

The performance of the module was measured in tests at CIT. The test results are documented in LIGO document T070213-00-C. The plot below was taken from this document and shows that the input-referred noise for the ADC using a 65536 SPS sample rate is approximately 4uV/√Hz.
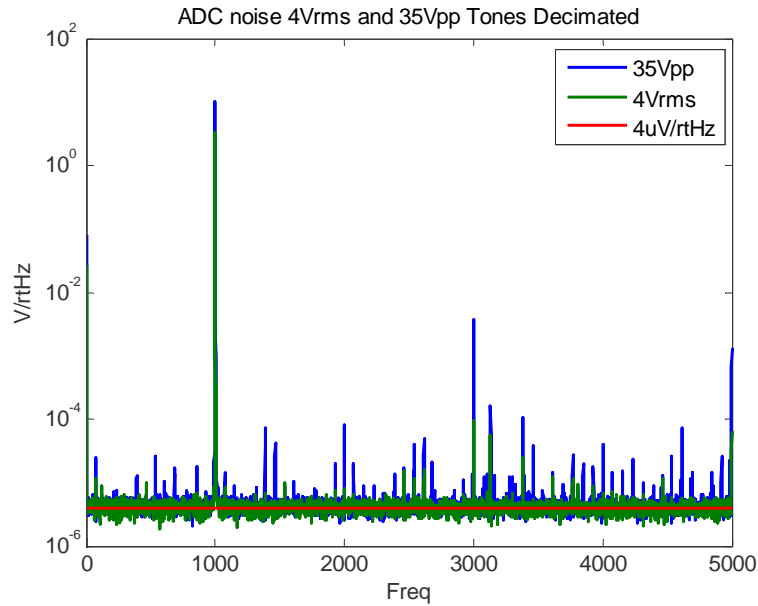

Figure 4: ADC Input-Referred Noise

2.1.3.2   DAC

The DAC modules presently being used for AdL FE systems are the General Standards model PCI66-16AO16-16-FO-DF.

The datasheet for this module can be viewed at:
http://www.generalstandards.com/specs/pmc66_16ao16_spec_022508.pdf

Note that the base module is actually a PMC bus module and can be used in PCIX and PCIe bus systems by attaching it to the appropriate adapter.

The performance of the module was measured in tests at CIT. The test results are documented in LIGO document T070264-00-C. The plot below was taken from this document and shows that the input-referred noise for the DAC using a 65536 SPS sample rate is approximately 700nV/√Hz.
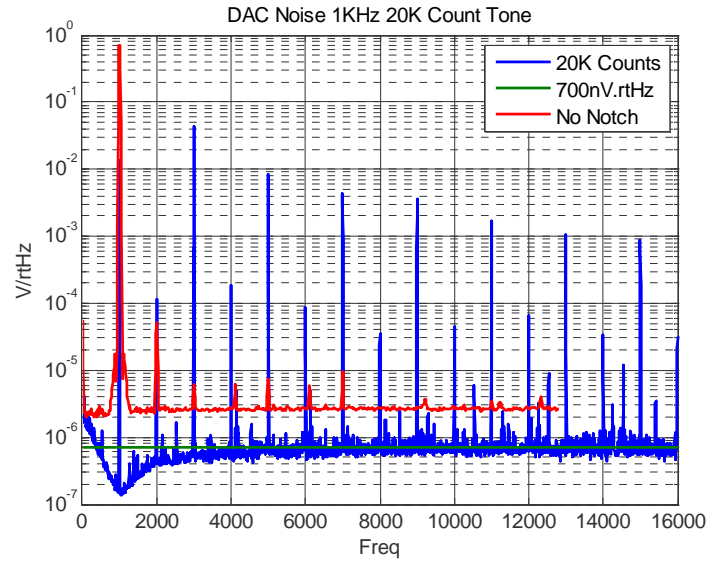
Figure 5: DAC Output-Referred Noise

2.1.3.3 Binary IO

Several binary IO modules are being used in AdL prototype and ELIGO systems or are being evaluated for use in AdL. Each has their own advantages and deficiencies. The first module used in AdL systems is the Accesio model PCI-IIRO-16. This module provides 16 relay contact outputs and 16 isolated binary inputs on a single PCIX bus card. The manual for the card can be viewed at: http://accesio.com/MANUALS/PCI-IIRO-16.PDF. This module is currently being used in the ELIGO OMC FE controls.

Presently being evaluated is a PCIe bus card available from Contec. This card is a model DO-32L-PE and it provides 32 channels of optically isolated open collector outputs. The specifications for the card can e viewed at:
http://www.contec.com/GOOD_SMART.PHP?Product=DO-32L-PE&Search=Search

Contec also makes binary input cards and other output cards in both PCIX and PCIe format.

2.1.4 Custom Interface Modules

2.1.4.1 ADC Interface

A block diagram of the ADC interface module (D060060) is shown in the figure below.
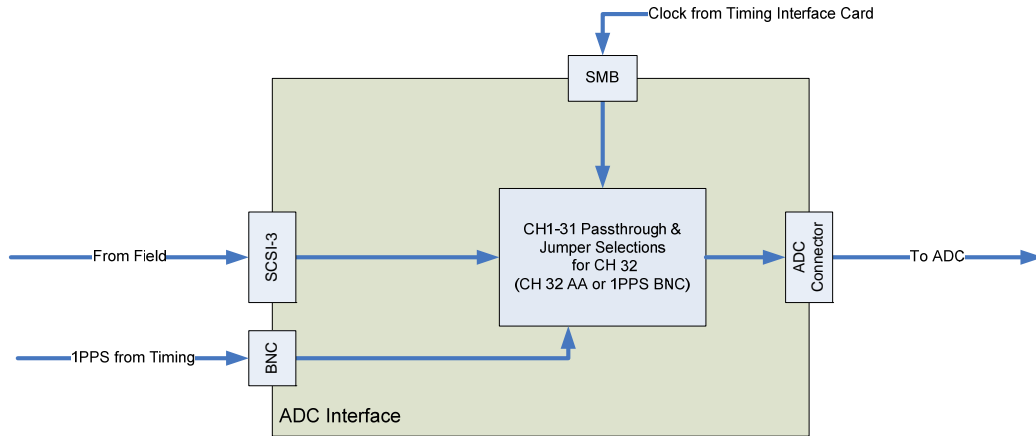
Figure 6: ADC Interface Block Diagram

The function of the ADC interface is to:
- Convert the pinout of the connector used for the commercial ADC to a connector more suitable and compatible with our existing cables and systems
- Allow connection of 1PPS into channel 32 of the ADC via on-board jumpers
- Connect the timing clock into appropriate pins on the ADC

2.1.4.2   DAC Interface

A block diagram of the DAC interface (D060061) module is shown in the figure below.
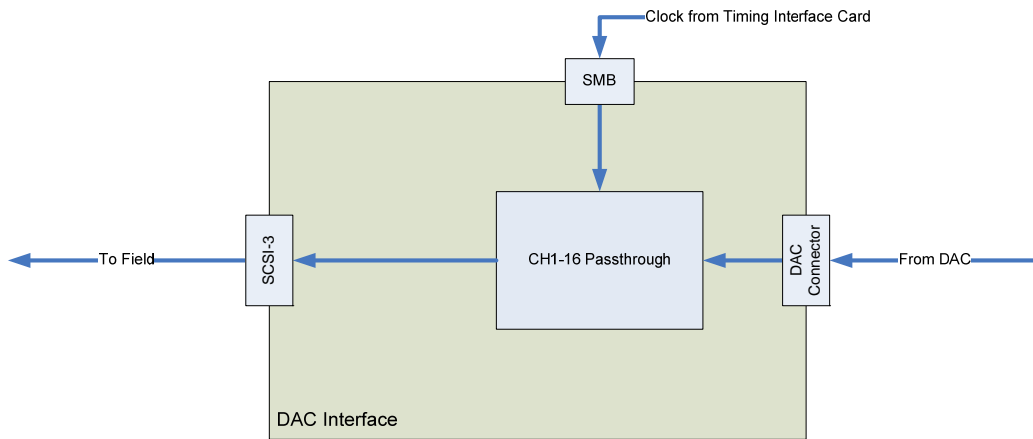

Figure 7: DAC Interface Block Diagram

The function of the DAC interface is to:
- Convert the pinout of the connector used for the commercial DAC to a connector more suitable and compatible with our existing cables and systems
- Connect the timing clock into appropriate pins on the DAC.

2.1.5   Power Supply

The power supply presently envisioned for the IO chassis is a standard ATX power The power supply used for evaluation at CIT was a Powerstream model PSTC-24450. Specifications for this supply can be viewed at:

http://www.powerstream.com/DC_PC.htm

The actual power supply used in the systems can vary, but will be generically equivalent to the model referenced above.

2.2 Anti-Alias and Anti-Image Filtering

At present, the nominal sample frequency for all AdL systems is 65536 SPS. Systems that require a lower sample rate for internal calculation and control are decimated and interpolated as necessary. The standard AA and AI filter used in AdL system is a 3rd order 10KHz Butterworth low pass filter with a single notch at 65536Hz. The schematic for a single channel is shown in the figure below.

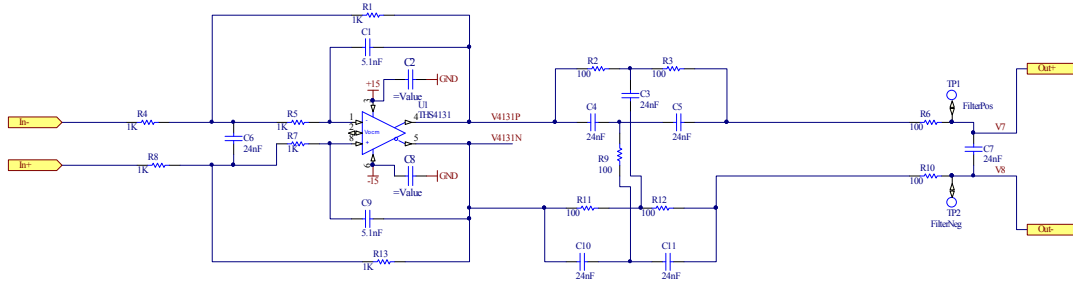3rd order Butterworth, 10KHz, notch at 65536Hz

Figure 8: AA and AI filter Schematic

A plot of the response of the filter is shown below.
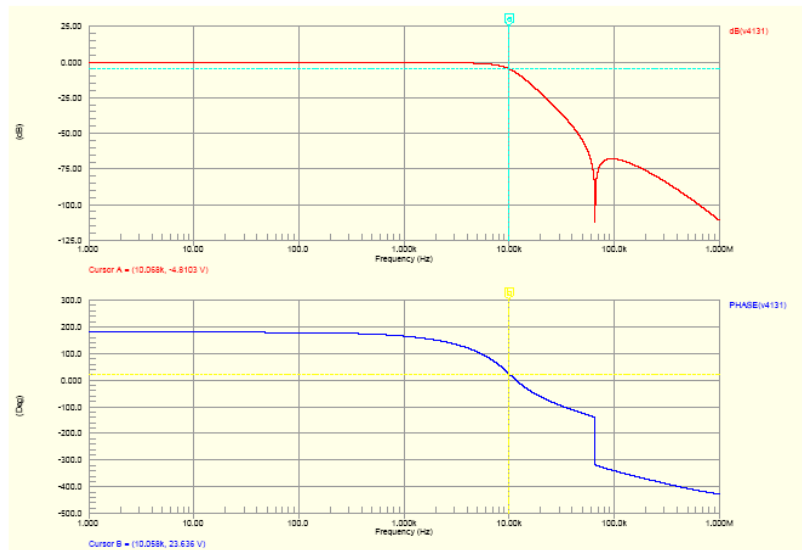
Figure 9: AA and AI Filter Response

The output noise of this filter is below 50nV/√Hz for 10Hz< freq< 50KHz.

Multiple filter boards are typically assembled into 1U or 2U high chassis for use in the system. The figure below is a picture of a typical 32 channel AA chassis.
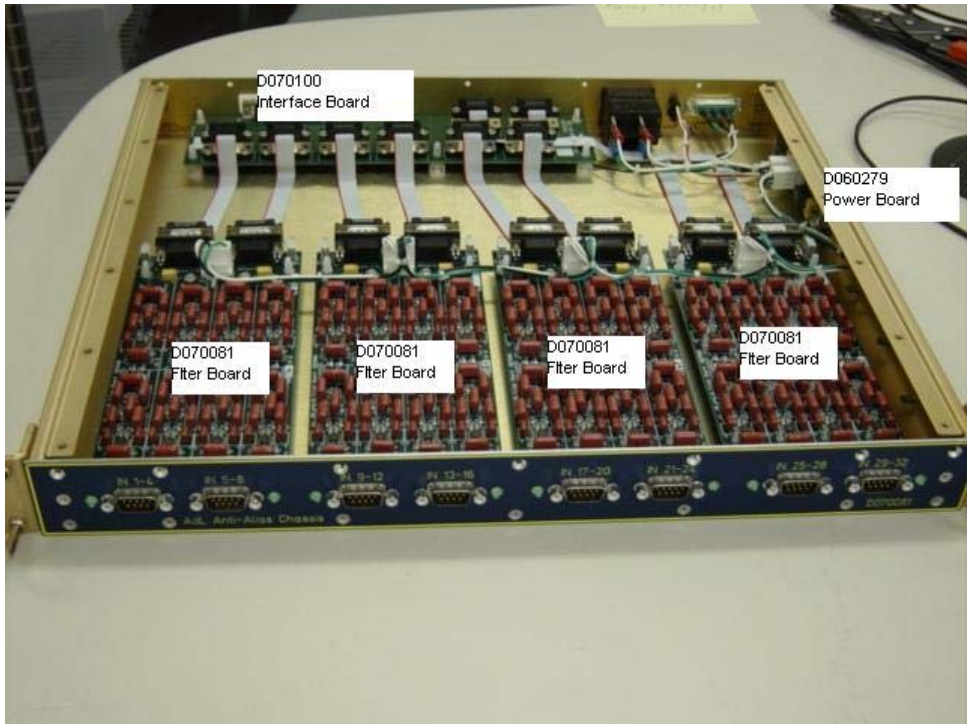
Figure 10: 32 Channel AA Filter Chassis

Other types of chassis are similar and may have an additional board mounted in front (or behind) the filter boards to provide whitening, dewhitening and appropriate connectors for connection to the field devices in specific systems.

3 Front End System Performance

The intention of this section is to document the magnitude and phase response of each hardware and software piece of the front end system. These pieces are:

- The AA and AI Filters
- The decimation and interpolation filters used in the front end software
- The time delay inherent in the sampling process. This includes the conversion times for the ADCs and DACs, the time required for the CPU to perform the IO tasks, the processor time required to perform the decimation and interpolation filtering and all user defined filtering.

3.1 AA and AI Filters

The magnitude and phase response of the AA and AI filters used in the system is shown in figure 9 above. Note that the response of the filter is inverting. The table below lists the nominal gain and phase at various frequencies.

Table 1: Nominal Gain and Phase for AA and AI Filter

Frequency	Nominal Gain	Nominal Phase	Phase from Nominal Inverting Response
10Hz	0 dB	180 deg	0 deg
100Hz	0 dB	179 deg	-1 deg
1KHz	0 dB	165 deg	-15 deg
10KHz	-4.8 dB	23.5 deg	-156.5 deg

3.2 Decimation and Interpolation Filters

The sample frequency for the ADC and the DACs used in the system is 65,536 SPS, but the actual system software runs at 32,768 SPS, therefore x2 decimation and interpolation filters are needed. The same filter function is used as both the decimation filter and the interpolation filter. A plot of the filter function is shown n the figure below.
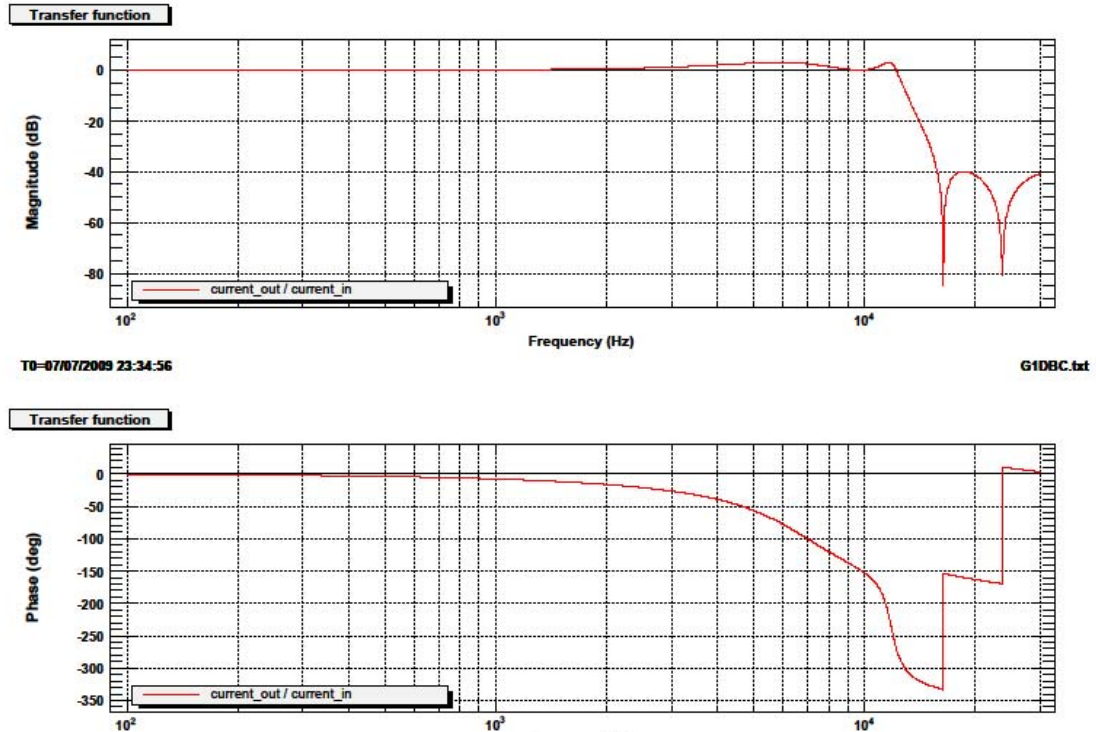

Figure 11: Transfer Function Decimation and Interpolation Filters

The filter function used to create the filter coefficients in FOTON was:
"ellip("LowPass",4,3,43,12187.9)gain(1.41254)" and the sample rate is 65536 SPS.

The table below shows the gain and phase of the filter for various frequencies. Note that the gain and phase is for a single instance of the filter. In the system both the decimation and interpolation filters are utilized so the total phase delay due to decimation and interpolation is double the values shown in the table.

Table 2: Nominal Gain and Phase for Decimation and Interpolation Filter

Frequency	Nominal Gain	Nominal Phase
10Hz	0 dB	-0.1 deg
100Hz	0 dB	-0.8 deg
1KHz	0.1 dB	-7.9 deg
10KHz	0 dB	-153 deg

3.3 Processing Time Delay

The figure below is a plot showing the transfer function through the front end system with and without the AA and AI filters in-line.
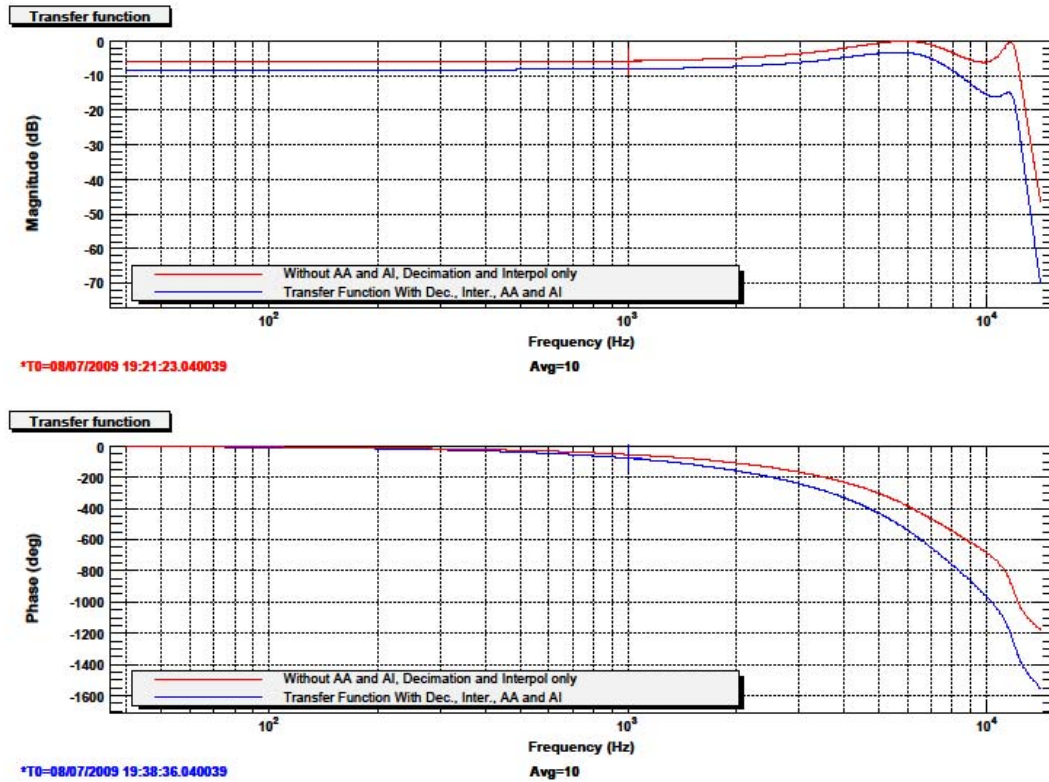
Transfer function

*T0=08/07/2009 19:21:23.040039   Avg=10

Transfer function

*T0=08/07/2009 19:38:36.040039   Avg=10

Figure 12: Transfer Function Through FE System With and Without AA and AI Filters

Note that the gain of the system with the AA and AI filters (BLUE) is 2.3 dB below the gain without the AA and AI filers (RED). This is not correct and is an artifact of measurement and the loading when an AI output filter is connected to the input of the AA filter. The -6.02dB gain is also an artifact that comes from the factor of two range difference between the DAC (20Vp-p) and the ADC (40Vp-p) modules.

The table below shows the phase versus frequency for each case.

Table 2: Phase versus Frequency

Frequency	All Filters In	Interpol and Dec Only
100Hz	-7.9 deg	-5.4 deg
1KHz	-78.3 deg	-53.8 deg
10KHz	-978.3 deg	-693.3 deg

The total processing time including all IO and software filtering can be calculating by subtracting the interpolation and decimation filter phase delays at each frequency and looking at the remaining phase. The table below summarizes this calculation.

Table 3: Process Time Calculation

Frequency	Interpol and Dec Only (A)	Total Phase of Interpol and Dec (B)	A-B	Delay = (A-B)/360*Freq	Delay in # of 32K sample clocks
100Hz	-5.4 deg	-0.8 x 2 = -1.6 deg	-3.8 deg	105.6usec	3.5

| 1KHz | -53.8 deg | -7.9 x 2 = -15.8 deg | -38 deg | 105.6usec | 3.5 |
| 10KHz | -693.3 deg | -153 x 2 = -306 deg | -387.3 deg | 107.6usec | 3.5 |

As can be seen from the calculations in the table above, the total processing delay through the system is 3.5 samples (32,768 SPS).