LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Unit Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

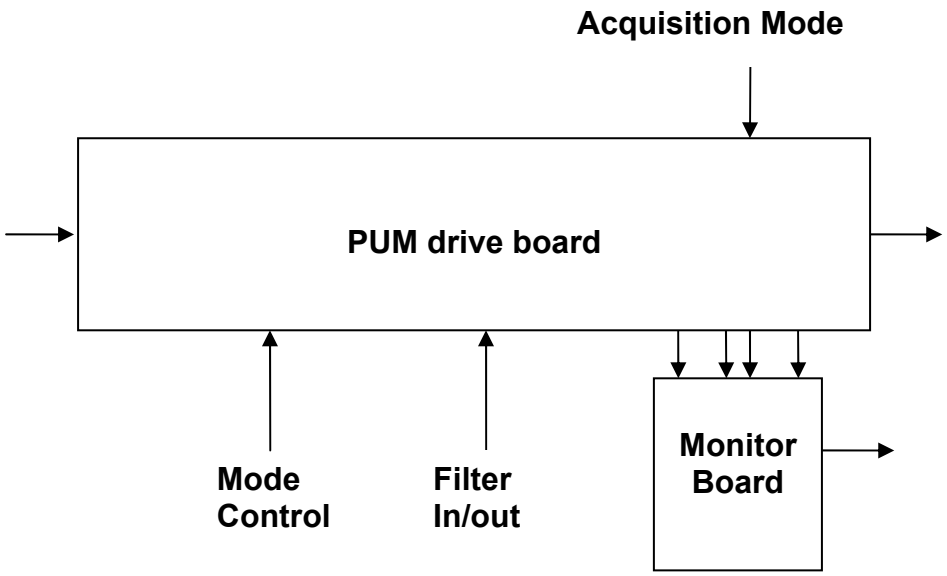
Unit……PUM20P
Test Engineer ……RMC
Date ……24/2/11

Drive Card ID……PUM20P
Monitor Card ID ……..MON84

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

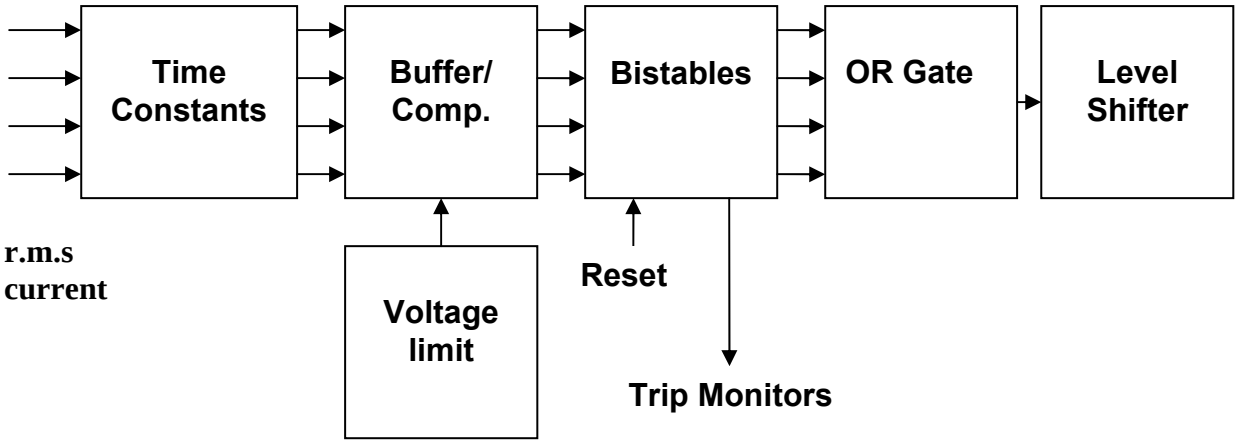
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

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4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

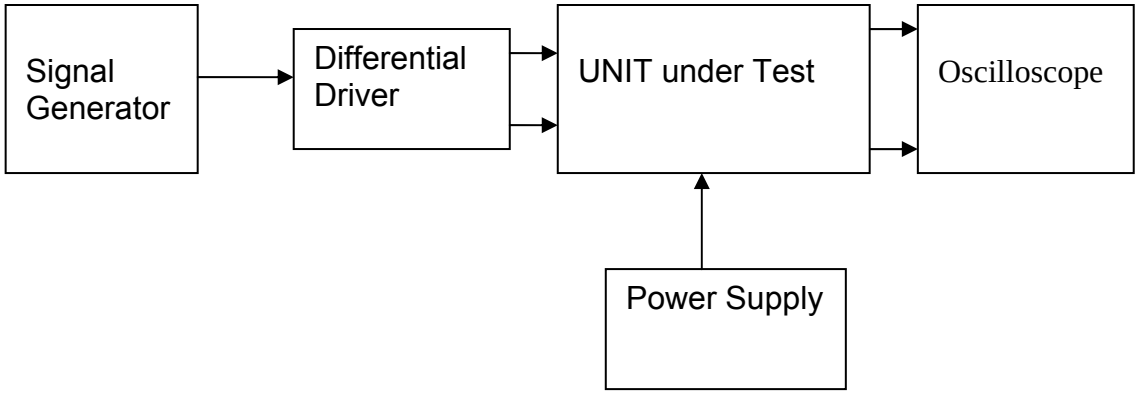
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.017	√	2 mV
+15v TP4	+14.873	√	2 mV
-15v TP6	-15.041	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pick up present

Record Power Supply Currents

Supply	Current
+16.5v	0.702 A
-16.5v	0.522 A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194	2	0.195v +/- 0.01v	√
2	0.194	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.194	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.200	1	0.195v +/- 0.01v	√
2	0.198	4	0.195v +/- 0.01v	√
3	0.198	7	0.195v +/- 0.01v	√
4	0.197	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

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9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.338 v
R.M.S. Current in the load	117 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.7 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. Connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2 seconds

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11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.498	24.9 mA
Ch2	0.495	24.7 mA
Ch3	0.489	24.4 mA
Ch4	0.494	24.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.656	32.8 mA	**16mA**	√
Ch2	0.654	32.7 mA	**16mA**	√
Ch3	0.650	32.5 mA	**16mA**	√
Ch4	0.654	32.7 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.749	37.4 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.749	37.4 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

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11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195	9.75 mA
Ch2	0.196	9.80 mA
Ch3	0.190	9.50 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.422	21.10 mA	**16mA**	√
Ch2	0.423	21.15 mA	**16mA**	√
Ch3	0.416	20.80 mA	**16mA**	√
Ch4	0.420	21.00 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.730	36.50 mA	**16mA**	√
Ch3	0.728	36.40 mA	**16mA**	√
Ch4	0.730	36.50 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749	37.45 mA	**16mA**	√
Ch2	0.749	37.45 mA	**16mA**	√
Ch3	0.748	37.40 mA	**16mA**	√
Ch4	0.750	37.50 mA	**16mA**	√

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Test Engineer ……RMC
Date ……24/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.18	5.91	295 mA
Ch2	4.18	5.91	295 mA
Ch3	4.16	5.88	294 mA
Ch4	4.14	5.85	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.57	7.87	393 mA	**400mA**	
Ch2	5.58	7.89	394 mA	**400mA**	
Ch3	5.56	7.86	393 mA	**400mA**	
Ch4	5.55	7.84	392 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.42	471 mA	**400mA**	√
Ch2	6.69	9.46	473 mA	**400mA**	√
Ch3	6.66	9.42	471 mA	**400mA**	√
Ch4	6.68	9.44	4.72 mA	**400mA**	√

5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	**400mA**	√
Ch2	6.70	9.47	473 mA	**400mA**	√
Ch3	6.69	9.46	473 mA	**400mA**	√
Ch4	6.70	9.47	473 mA	**400mA**	√

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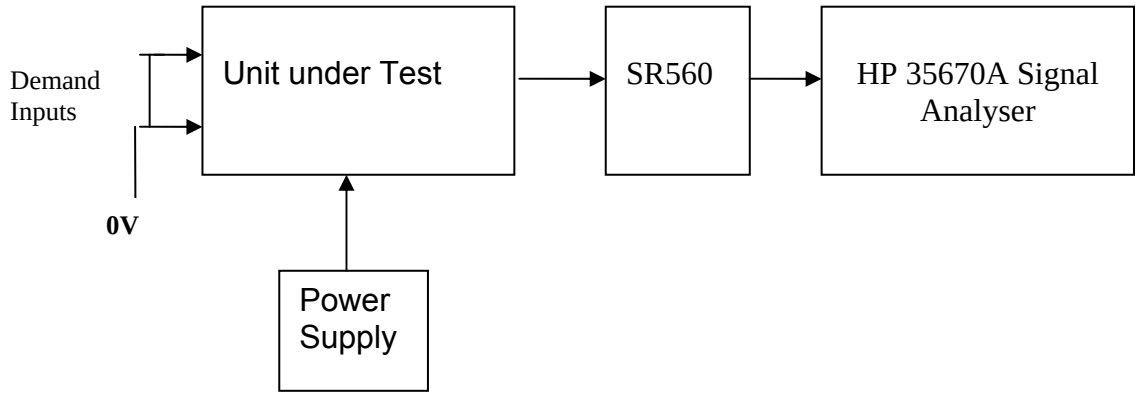
12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-99.0 dB	-159.0 dB
Ch2	-155.1	-99.4 dB	-159.4 dB
Ch3	-155.1	-97.3 dB	-157.3 dB
Ch4	-155.1	-98.7 dB	-158.7 dB

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

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Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.14	2.9μV√Hz	√
2		1.95	2.9μV√Hz	√
3		2.30	2.9μV√Hz	√
4		1.77	2.9μV√Hz	√

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

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14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM20P
Driver board ID	PUM20P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM20P
Monitor board ID	MON84
Monitor board Drawing No/Issue No	DO70480_05_K
Monitor board Serial Number	MON84

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

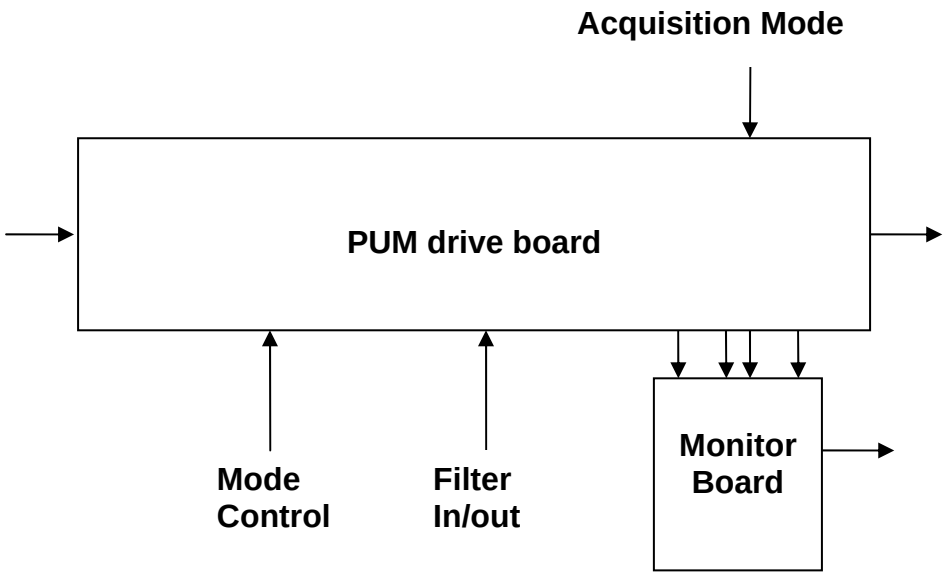
Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

Drive Card ID……PUM2P
Monitor Card ID …… MON198P

Contents

1. Description

Block diagram



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The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

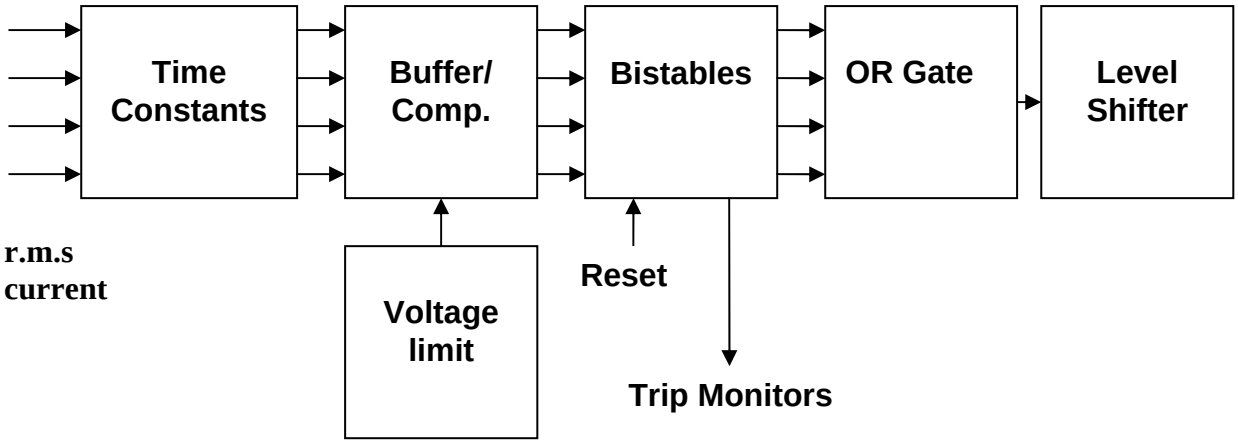
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	287	
Voltage calibrator	Time	1044	
PSU	Farnell	30-2	
PSU	Farnell	30-2	
Scope	Tektronix	2225	
DSA	Agilent	35670	

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

4. Continuity Checks

Continuity to the V, I and R.M.S Monitor (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

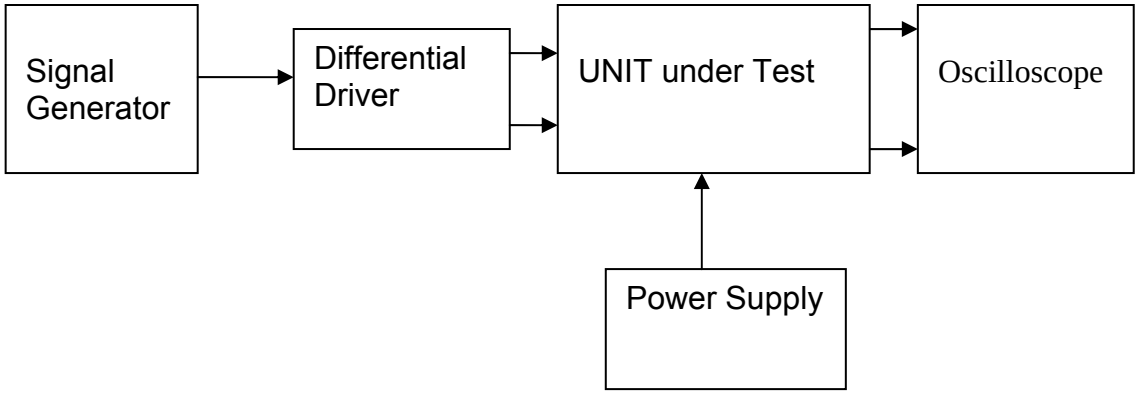
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.011v	√	1mV
+15v TP4	14.95v	√	1.2mV
-15v TP6	-15.08v	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.75A
-16.5v	0.6A

If the supplies are correct, proceed to the next test.

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS √

Channel	Indicator		OK?
	ON	OFF	
Ch1			
Ch2			
Ch3			
Ch4			

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.332v	3	0.33v	√
2	0.332v	6	0.33v	√
3	0.332v	9	0.33v	√
4	0.332v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195v	2	0.195v +/- 0.01v	√
2	0.196v	5	0.195v +/- 0.01v	√
3	0.196v	8	0.195v +/- 0.01v	√
4	0.196v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.200v	1	0.195v +/- 0.01v	√
2	0.200v	4	0.195v +/- 0.01v	√
3	0.202v	7	0.195v +/- 0.01v	√
4	0.198v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

Using the Dynamic Signal Analyser, measure the noise monitor outputs in dBV/√Hz. Correct for the pre-amplifier gain (if used.)

Ch.	Pin	Output	Limit	OK?
1	1	1.66	2.9µV	√
2	2	1.24	2.9µV	√
3	3	1.94	2.9µV	√
4	4	2.42	2.9µV	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.3v
R.M.S. Current in the load	117mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2.2 seconds

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……20/5/10

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.2318	11.59 mA
Ch2	0.2333	11.66 mA
Ch3	0.2319	11.59 mA
Ch4	0.2314	11.57 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.3986	19.93	**16mA**	√
Ch2	0.4009	20.00	**16mA**	√
Ch3	0.3989	19.9	**16mA**	√
Ch4	0.3981	19.9	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.7162	35.81 mA	**16mA**	√
Ch2	0.7172	35.86 mA	**16mA**	√
Ch3	0.7157	35.78 mA	**16mA**	√
Ch4	0.7144	35.72 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.7474	37.37 mA	**16mA**	√
Ch2	0.7480	37.4mA	**16mA**	√
Ch3	0.7471	37.3 mA	**16mA**	√
Ch4	0.7455	37.27 mA	**16mA**	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……20/5/10

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.089	4.45		
Ch2	0.089	4.45		
Ch3	0.090	4.5		
Ch4	0.089	4.45		

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.255	12.75 mA	**16mA**	
Ch2	0.255	12.75 mA	**16mA**	
Ch3	0.257	12.85 mA	**16mA**	
Ch4	0.257	12.85 mA	**16mA**	

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.695	34.75 mA	**16mA**	√
Ch2	0.696	34.8 mA	**16mA**	√
Ch3	0.696	34.8 mA	**16mA**	√
Ch4	0.695	34.76 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.746	37.3 mA	**16mA**	√
Ch2	0.746	37.3 mA	**16mA**	√
Ch3	0.746	37.3 mA	**16mA**	√
Ch4	0.744	37.2 mA	**16mA**	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……20/5/10

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	4.09	5.784	289.2 mA		
Ch2	4.107	5.808	290.4 mA		
Ch3	4.093	5.788	289.4 mA		
Ch4	4.127	5.836	291.8 mA		

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.587	7.901	395 mA	**400mA**	
Ch2	5.580	7.891	394.5 mA	**400mA**	
Ch3	5.563	7.867	393.3 mA	**400mA**	
Ch4	5.593	7.909	395.4 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.628	9.373	468.6 mA	**400mA**	√
Ch2	6.621	9.363	468.1 mA	**400mA**	√
Ch3	6.618	9.359	467.9 mA	**400mA**	√
Ch4	6.614	9.353	467.6 mA	**400mA**	√

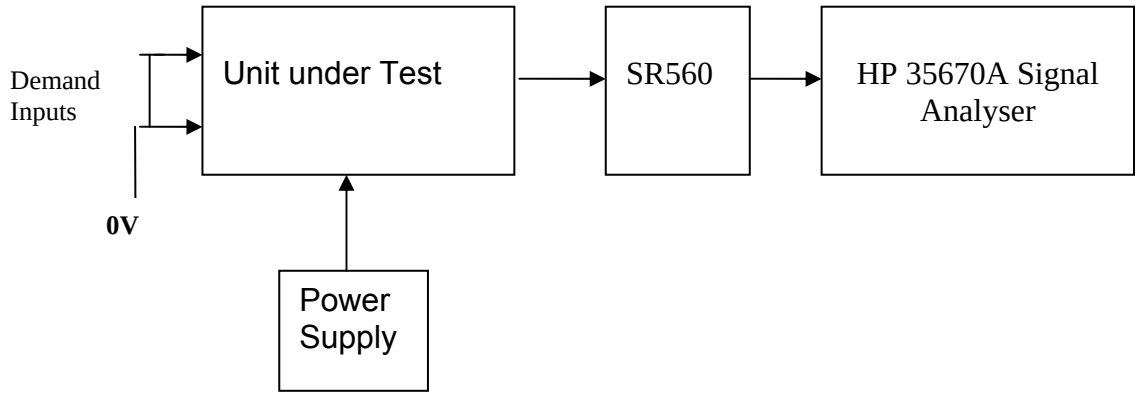
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.673	9.437	471.8 mA	**400mA**	√
Ch2	6.658	9.415	470.7 mA	**400mA**	√
Ch3	6.673	9.437	471.8 mA	**400mA**	√
Ch4	6.640	9.390	469.5 mA	**400mA**	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.6	-158.6
Ch2	-155.1	-100.35	-160.35
Ch3	-155.1	-99.66	-159.66
Ch4	-155.1	-101.2	-161.2

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-12.00	√	-12.00	√	-12.00	√	-12.00	√
-7v	-8.40	√	-8.4	√	-8.40	√	-8.40	√
-5v	-5.99	√	-5.99	√	-6.0	√	-6.0	√
-1v	-1.2	√	-1.2	√	-1.2	√	-1.2	√
0v	0.02	√	-0.017	√	-0.017	√	0.017	√
1v	1.2	√	1.21	√	1.21	√	1.21	√
5v	5.99	√	5.99	√	5.99	√	6.00	√
7v	8.44	√	8.44	√	8.44	√	8.44	√
10v	11.9	√	11.9	√	11.9	√	11.9	√

Unit……PUM2P……Serial No ……
Test Engineer ……RMC
Date ……8/6/10

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. Not fitted

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	PUM2P
Driver board ID	PUM2P
Driver board Drawing No/Issue No	D070483_5_K
Driver board Serial Number	PUM2P
Monitor board ID	MON198P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON198P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

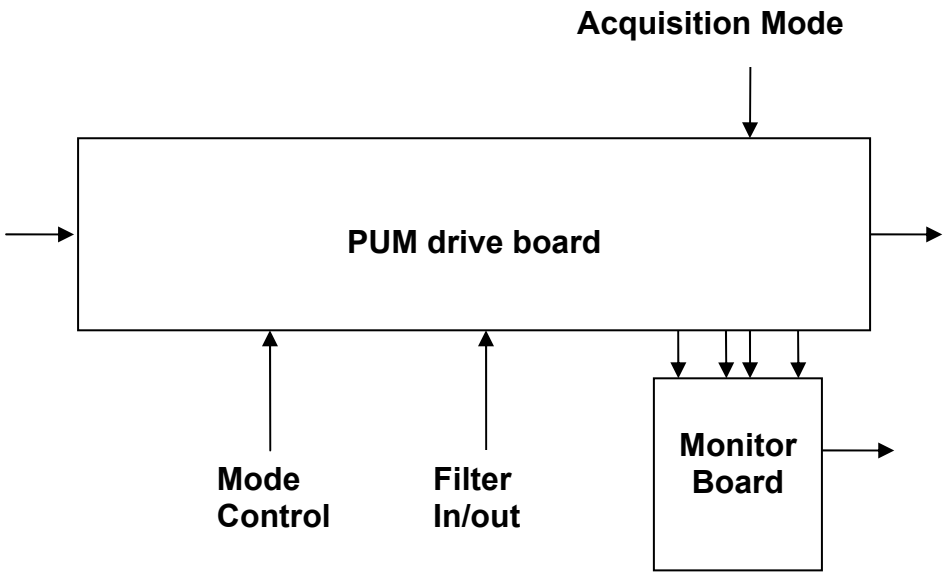
Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……

Drive Card ID……PUM3P
Monitor Card ID …… MON189P

Contents

1. Description

Block diagram



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The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

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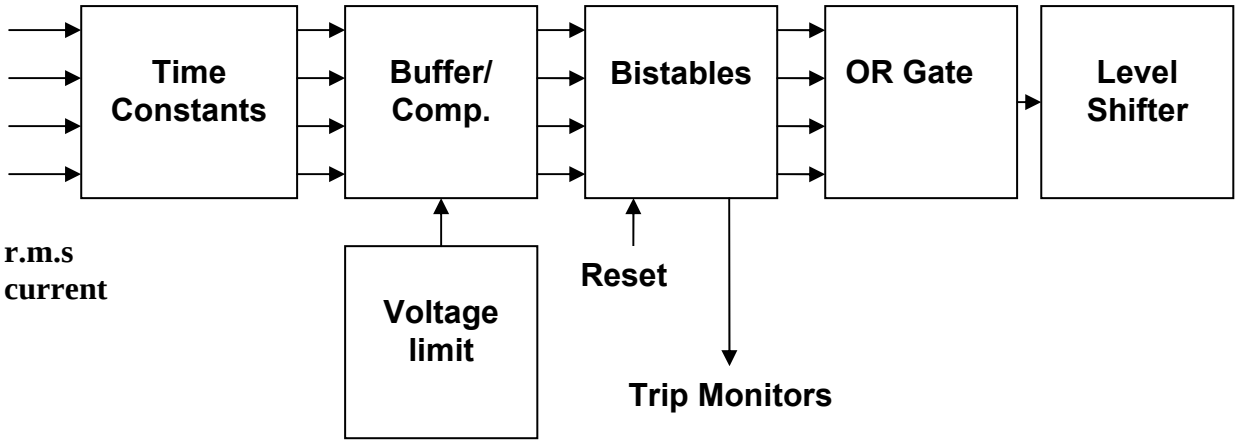

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The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	287	
Voltage calibrator	Time	1044	
PSU	Farnell	30-2	
PSU	Farnell	30-2	
Scope	Tektronix	2225	
DSA	Agilent	35670	

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

4. Continuity Checks

Continuity to the V, I and R.M.S Monitor (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

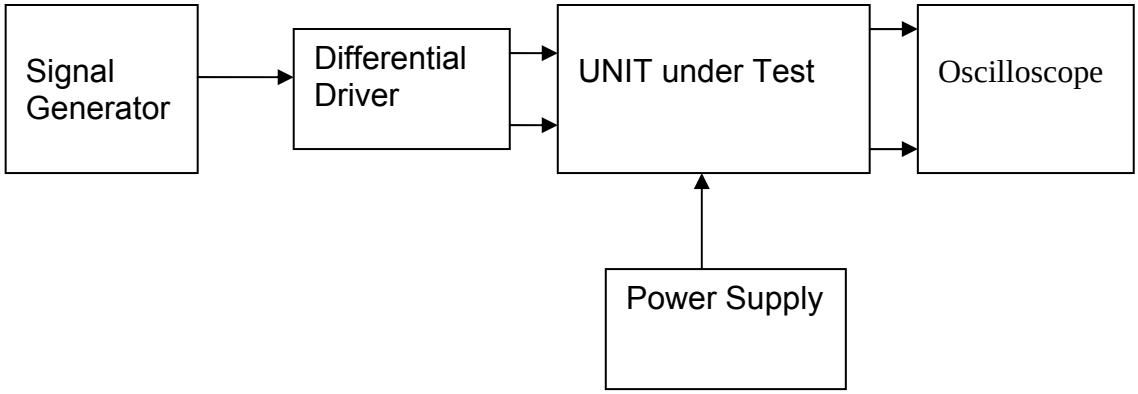
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04v	√	1mV
+15v TP4	14.95v	√	1.2mV
-15v TP6	-14.95v	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.56A
-16.5v	0.5A

If the supplies are correct, proceed to the next test.

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS √

Channel	Indicator		OK?
	ON	OFF	
Ch1			
Ch2			
Ch3			
Ch4			

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33v	3	0.33v	√
2	0.33v	6	0.33v	√
3	0.33v	9	0.33v	√
4	0.33v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194v	2	0.195v +/- 0.01v	√
2	0.195v	5	0.195v +/- 0.01v	√
3	0.195v	8	0.195v +/- 0.01v	√
4	0.195v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.198v	1	0.195v +/- 0.01v	√
2	0.199v	4	0.195v +/- 0.01v	√
3	0.199v	7	0.195v +/- 0.01v	√
4	0.200v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

Using the Dynamic Signal Analyser, measure the noise monitor outputs in dBV/√Hz. Correct for the pre-amplifier gain (if used.)

Ch.	Pin	Output	Limit	OK?
1	1	1.6	2.9µV	√
2	2	1.24	2.9µV	√
3	3	1.49	2.9µV	√
4	4	1.38	2.9µV	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……24/5/10

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v. Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.3v
R.M.S. Current in the load	117mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.5 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2.3 seconds

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……2/6/10

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.233	11.65 mA
Ch2	0.233	11.65 mA
Ch3	0.231	11.55 mA
Ch4	0.230	11.50 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.400	20.00	**16mA**	√
Ch2	0.399	19.9	**16mA**	√
Ch3	0.389	19.4	**16mA**	√
Ch4	0.397	19.85	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.717	35.85 mA	**16mA**	√
Ch2	0.716	35.58 mA	**16mA**	√
Ch3	0.716	35.58 mA	**16mA**	√
Ch4	0.714	35.7 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.747	37.35 mA	**16mA**	√
Ch2	0.745	37.25mA	**16mA**	√
Ch3	0.714	37.7 mA	**16mA**	√
Ch4	0.745	37.25 mA	**16mA**	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……2/6/10

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.089	4.45		
Ch2	0.089	4.45		
Ch3	0.090	4.5		
Ch4	0.088	4.4		

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.256	12.8 mA	**16mA**	
Ch2	0.256	12.8 mA	**16mA**	
Ch3	0.257	12.85 mA	**16mA**	
Ch4	0.255	12.75 mA	**16mA**	

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.648	32.4 mA	**16mA**	√
Ch2	0.646	32.3 mA	**16mA**	√
Ch3	0.646	32.3 mA	**16mA**	√
Ch4	0.646	32.3 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.663	33.15 mA	**16mA**	√
Ch2	0.691	34.55 mA	**16mA**	√
Ch3	0.690	34.5mA	**16mA**	√
Ch4	0.690	34.5 mA	**16mA**	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……20/5/10

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	4.11	5.822	291.1 mA		
Ch2	4.107	5.808	290.4 mA		
Ch3	4.126	5.835	291.7 mA		
Ch4	4.112	5.815	290.7 mA		

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.590	7.905	395.5 mA	**400mA**	
Ch2	5.578	7.888	394.4 mA	**400mA**	
Ch3	5.592	7.908	395.4 mA	**400mA**	
Ch4	5.574	7.908	395.4 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.629	9.374	468.7 mA	**400mA**	√
Ch2	6.627	9.371	468.5 mA	**400mA**	√
Ch3	6.696	9.328	466.4 mA	**400mA**	√
Ch4	6.607	9.343	467.1 mA	**400mA**	√

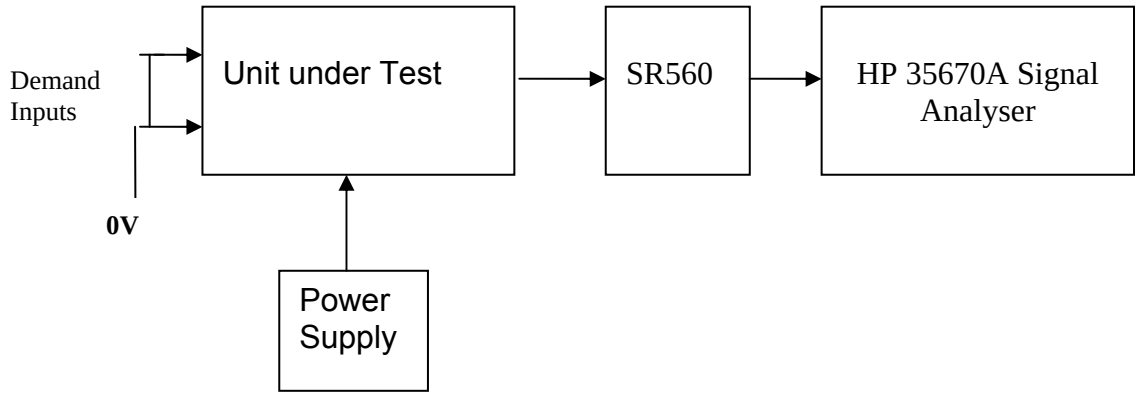
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.657	9.414	470.7 mA	**400mA**	√
Ch2	6.676	9.441	472.0 mA	**400mA**	√
Ch3	6.601	9.335	466.7 mA	**400mA**	√
Ch4	6.655	9.411	470.5 mA	**400mA**	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.9	-158.9
Ch2	-155.1	-101.8	-161.8
Ch3	-155.1	-101.1	-161.1
Ch4	-155.1	-99.8	-159.8

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……25/5/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-12.00	√	-12.00	√	-12.00	√	-12.00	√
-7v	-8.40	√	-8.4	√	-8.40	√	-8.40	√
-5v	-6.00	√	-6.00	√	-6.0	√	-6.0	√
-1v	-1.2	√	-1.2	√	-1.2	√	-1.2	√
0v	0.00	√	0.00	√	0.00	√	0.00	√
1v	1.2	√	1.2	√	1.2	√	1.2	√
5v	6.00	√	6.00	√	6.00	√	6.00	√
7v	8.4	√	8.4	√	8.4	√	8.4	√
10v	12.0	√	12.0	√	12.0	√	12.0	√

Unit……PUM3P……Serial No ……
Test Engineer ……RMC
Date ……8/6/10

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. Not fitted

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	PUM3P
Driver board ID	PUM3P
Driver board Drawing No/Issue No	D070483_5_K
Driver board Serial Number	PUM3P
Monitor board ID	MON189P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON189P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

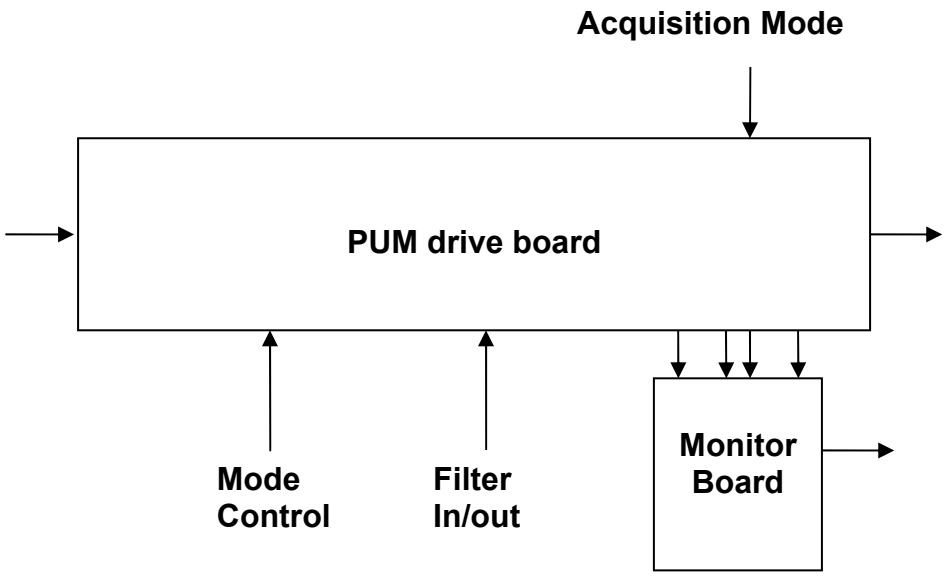
Unit……PUM4P……Serial No ……
Test Engineer ……RMC

Drive Card ID……PUM4P
Monitor Card ID …… MON188P

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

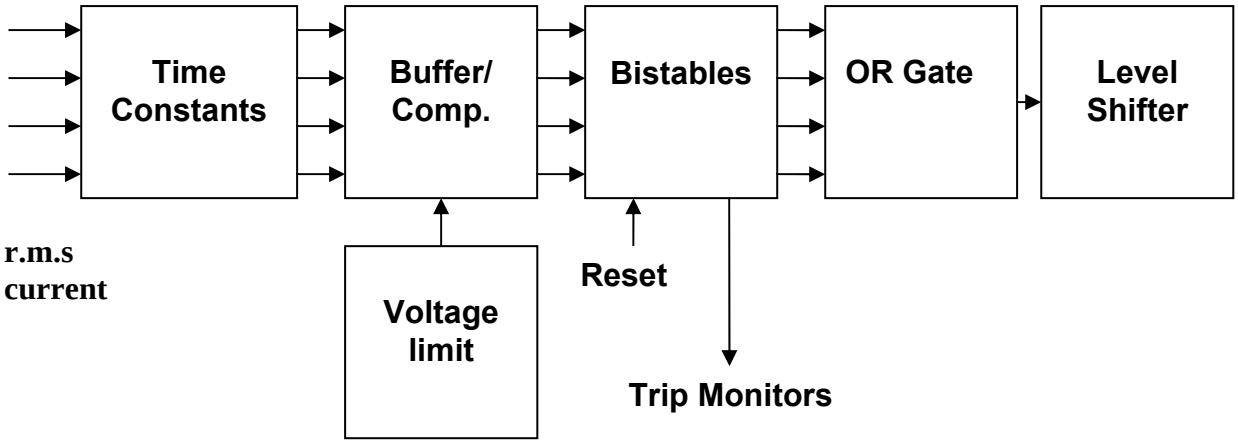
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 3/6/10

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	287	
Voltage calibrator	Time	1044	
PSU	Farnell	30-2	
PSU	Farnell	30-2	
Scope	Tektronix	2225	
DSA	Agilent	35670	

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 3/6/10

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 25/5/10

4. Continuity Checks

Continuity to the V, I and R.M.S Monitor (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

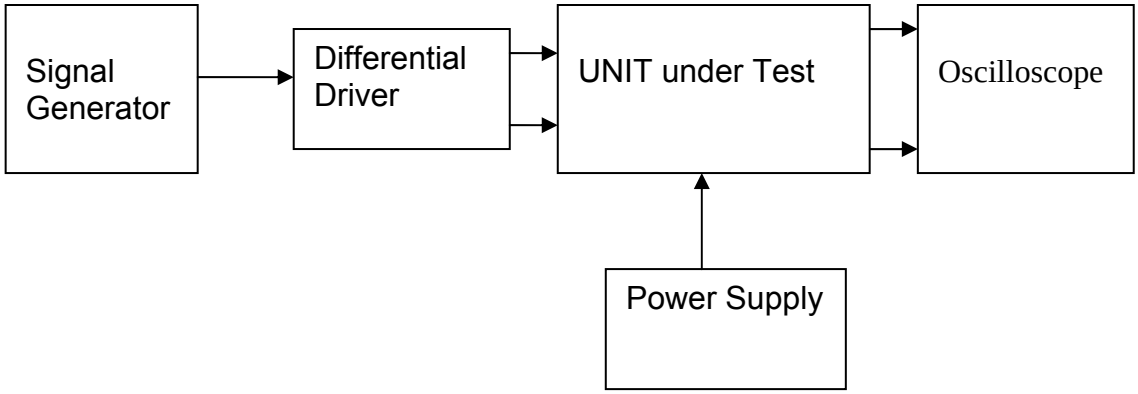
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 24/5/10

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.035v	√	1mV
+15v TP4	14.95v	√	1.2mV
-15v TP6	-15.09v	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.82A
-16.5v	0.5A

If the supplies are correct, proceed to the next test.

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 24/5/10

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS √

Channel	Indicator		OK?
	ON	OFF	
Ch1			
Ch2			
Ch3			
Ch4			

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 25/5/10

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.331v	3	0.33v	√
2	0.332v	6	0.33v	√
3	0.332v	9	0.33v	√
4	0.332v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.1952v	2	0.195v +/- 0.01v	√
2	0.1956v	5	0.195v +/- 0.01v	√
3	0.1956v	8	0.195v +/- 0.01v	√
4	0.1955v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.2004v	1	0.195v +/- 0.01v	√
2	0.1987v	4	0.195v +/- 0.01v	√
3	0.1970v	7	0.195v +/- 0.01v	√
4	0.1964v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

Using the Dynamic Signal Analyser, measure the noise monitor outputs in dBV/√Hz. Correct for the pre-amplifier gain (if used.)

Ch.	Pin	Output	Limit	OK?
1	1	1.6	2.9µV	√
2	2	1.69	2.9µV	√
3	3	1.59	2.9µV	√
4	4	2.57	2.9µV	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 25/5/10

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 24/5/10

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v. Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.34v
R.M.S. Current in the load	117mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.0 seconds

Disconnect the signal generator, and wait for the capacitors to discharge. Cycle the power supply. Adjust the signal generator to 10v. Connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2.4 seconds

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 26/5/10

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.231	11.5 mA
Ch2	0.233	11.6 mA
Ch3	0.230	11.5 mA
Ch4	0.231	11.5 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.398	19.9	**16mA**	√
Ch2	0.400	20.0	**16mA**	√
Ch3	0.397	19.8	**16mA**	√
Ch4	0.398	19.9	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.715	35.7 mA	**16mA**	√
Ch2	0.716	35.8 mA	**16mA**	√
Ch3	0.714	35.7 mA	**16mA**	√
Ch4	0.713	35.6 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.25 mA	**16mA**	√
Ch2	0.747	37.35mA	**16mA**	√
Ch3	0.746	37.30 mA	**16mA**	√
Ch4	0.743	37.15 mA	**16mA**	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.090	4.5		
Ch2	0.089	4.45		
Ch3	0.088	4.4		
Ch4	0.090	4.5		

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.257	12.85 mA	**16mA**	
Ch2	0.256	12.8 mA	**16mA**	
Ch3	0.253	12.65 mA	**16mA**	
Ch4	0.258	12.9 mA	**16mA**	

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.695	34.75 mA	**16mA**	√
Ch2	0.696	34.8 mA	**16mA**	√
Ch3	0.694	34.7 mA	**16mA**	√
Ch4	0.694	34.7 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.25 mA	**16mA**	√
Ch2	0.746	37.3 mA	**16mA**	√
Ch3	0.745	37.25mA	**16mA**	√
Ch4	0.743	37.15 mA	**16mA**	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 20/5/10

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	4.108	5.809	290 mA		
Ch2	4.085	5.777	288 mA		
Ch3	4.097	5.794	289 mA		
Ch4	4.064	5.747	278 mA		

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.584	7.896	394.8 mA	**400mA**	
Ch2	5.545	7.841	392.0 mA	**400mA**	
Ch3	5.573	7.881	394.0 mA	**400mA**	
Ch4	5.542	7.837	391.8 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.633	9.38	469 mA	**400mA**	√
Ch2	6.600	9.33	466.5 mA	**400mA**	√
Ch3	6.628	9.37	468.5 mA	**400mA**	√
Ch4	6.604	9.34	466.9 mA	**400mA**	√

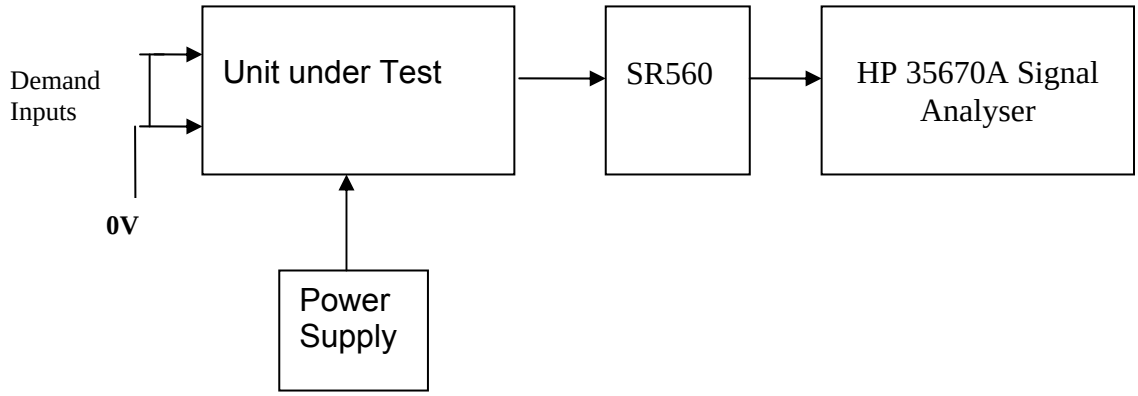
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.663	9.423	471.1 mA	**400mA**	√
Ch2	6.637	9.386	469.3 mA	**400mA**	√
Ch3	6.657	9.414	470.7 mA	**400mA**	√
Ch4	6.677	9.442	472.1 mA	**400mA**	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 25/5/10

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-100.13	-160.13
Ch2	-155.1	-101	-161.0
Ch3	-155.1	-101.6	-161.6
Ch4	-155.1	-101.5	-161.5

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 25/5/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-11.99	√	-12.00	√	-12.01	√	-12.01	√
-7v	-8.38	√	-8.37	√	-8.39	√	-8.40	√
-5v	-5.99	√	-6.00	√	-6.00	√	-6.00	√
-1v	-1.212	√	-1.218	√	-1.212	√	-1.212	√
0v	0.00	√	0.00	√	0.00	√	0.00	√
1v	1.217	√	1.217	√	1.217	√	1.217	√
5v	5.91	√	5.96	√	5.98	√	6.00	√
7v	8.39	√	8.40	√	8.40	√	8.40	√
10v	11.83	√	11.93	√	11.97	√	11.98	√

Unit……PUM4P……Serial No ……
Test Engineer ……RMC
Date …… 8/6/10

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. Not fitted

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	PUM4P
Driver board ID	PUM4P
Driver board Drawing No/Issue No	D070483_5_K
Driver board Serial Number	PUM4P
Monitor board ID	MON188P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON188P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

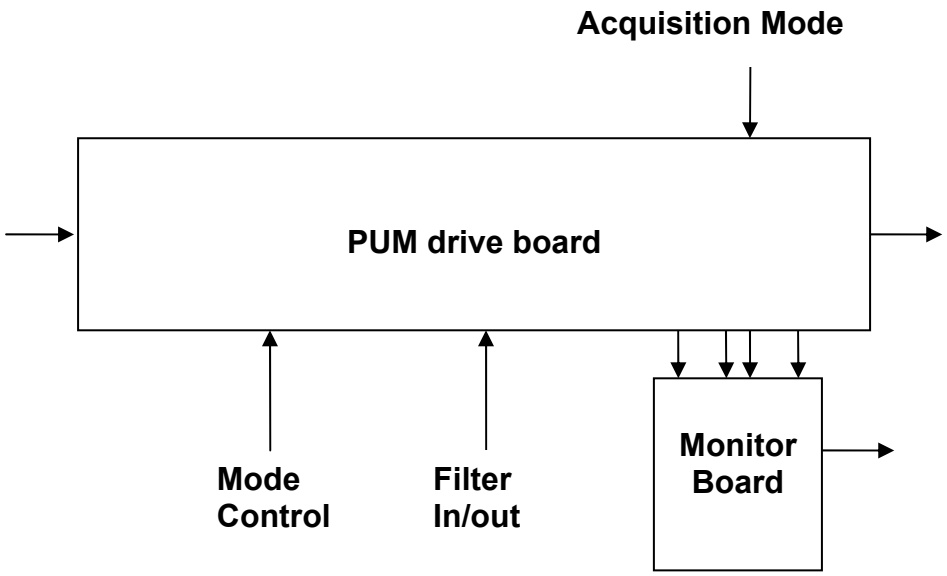
Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

Drive Card ID……PUM5P
Monitor Card ID ……..MON267

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

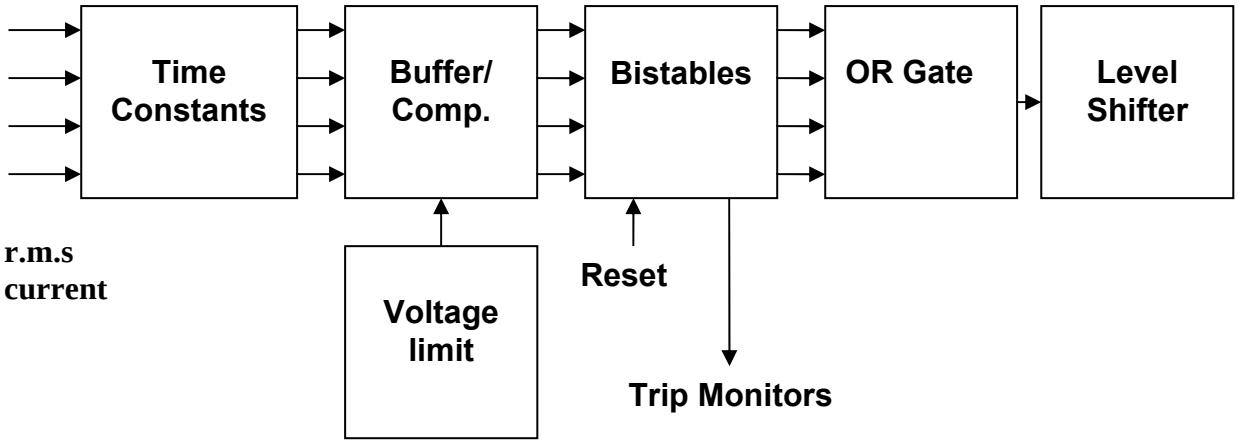
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
Power supply	TTI	EL302RD
Power supply	Farnell	LT30-1
Oscilloscope	Tektronix	2225
Function Generator	Agient	33250A

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

4. Continuity Checks

Continuity to the PD in from SAT

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

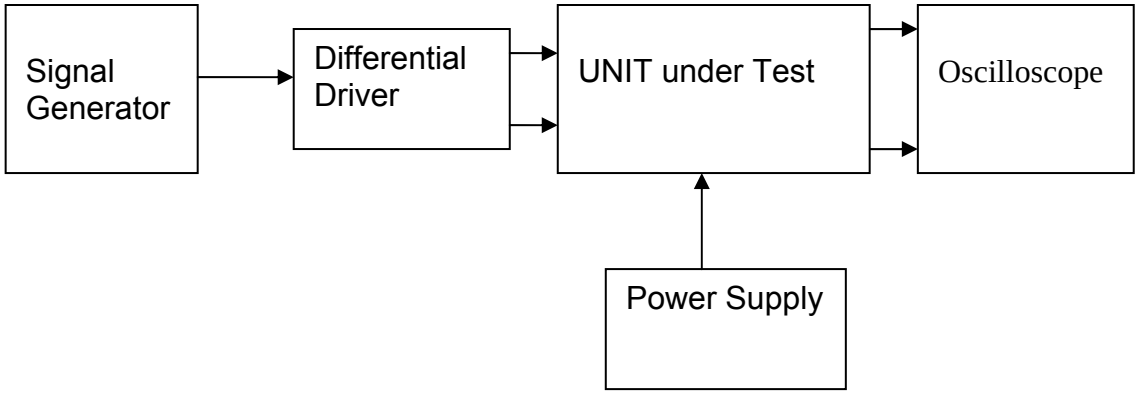
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.057v	√	2mV
+15v TP4	14.94v	√	2mV
-15v TP6	-15.15v	√	6mV

Differential readings – high common mode

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.510 A
-16.5v	0.466 A

If the supplies are correct, proceed to the next test.

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.333v	3	0.33v	√
2	0.333v	6	0.33v	√
3	0.333v	9	0.33v	√
4	0.333v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195 v	2	0.195v +/- 0.01v	√
2	0.195 v	5	0.195v +/- 0.01v	√
3	0.195 v	8	0.195v +/- 0.01v	√
4	0.196 v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.198 v	1	0.195v +/- 0.01v	√
2	0.201 v	4	0.195v +/- 0.01v	√
3	0.198 v	7	0.195v +/- 0.01v	√
4	0.198 v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.35v
R.M.S. Current in the load	117 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.5 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2 seconds

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.491 v	24.5 mA
Ch2	0.494 v	24.7 mA
Ch3	0.501 v	25.0 mA
Ch4	0.495 v	24.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.651 v	32.55 mA	**16mA**	√
Ch2	0.654 v	32.7 mA	**16mA**	√
Ch3	0.657 v	32.8 mA	**16mA**	√
Ch4	0.654 v	32.7 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749 v	37.45 mA	**16mA**	√
Ch2	0.750 v	37.5 mA	**16mA**	√
Ch3	0.750 v	37.5 mA	**16mA**	√
Ch4	0.750 v	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749 v	37.45 mA	**16mA**	√
Ch2	0.750 v	37.5 mA	**16mA**	√
Ch3	0.750 v	37.5 mA	**16mA**	√
Ch4	0.750 v	37.5 mA	**16mA**	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.192 v	9.6 mA
Ch2	0.193 v	9.65 mA
Ch3	0.200 v	10.0 mA
Ch4	0.194 v	9.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.417 v	20.85 mA	**16mA**	√
Ch2	0.420 v	21.0 mA	**16mA**	√
Ch3	0.429 v	21.45 mA	**16mA**	√
Ch4	0.420 v	21.0 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.728 v	36.4 mA	**16mA**	√
Ch2	0.729 v	36.45 mA	**16mA**	√
Ch3	0.730 v	36.5 mA	**16mA**	√
Ch4	0.727 v	36.35 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748 v	37.4 mA	**16mA**	√
Ch2	0.749 v	37.45 mA	**16mA**	√
Ch3	0.749 v	37.45 mA	**16mA**	√
Ch4	0.749 v	37.45 mA	**16mA**	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.18	5.91	295 mA
Ch2	4.16	5.88	294 mA
Ch3	4.13	5.84	292 mA
Ch4	4.15	5.86	293 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.57	7.87	393 mA	**400mA**	
Ch2	5.56	7.86	393 mA	**400mA**	
Ch3	5.55	7.85	392 mA	**400mA**	
Ch4	5.55	7.85	392 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**400mA**	√
Ch2	6.66	9.42	470 mA	**400mA**	√
Ch3	6.67	9.43	471 mA	**400mA**	√
Ch4	6.66	9.42	470 mA	**400mA**	√

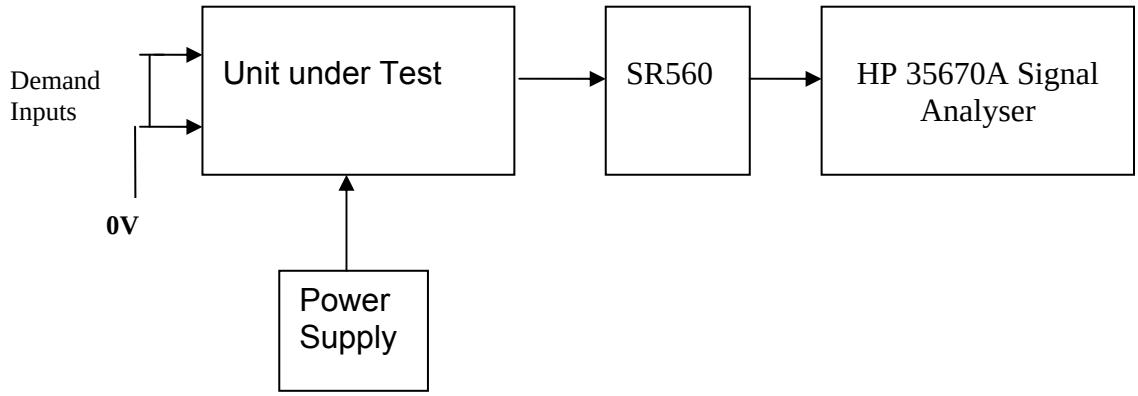
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.475	473 mA	**400mA**	√
Ch2	6.70	9.475	473 mA	**400mA**	√
Ch3	6.70	9.475	473 mA	**400mA**	√
Ch4	6.68	9.44	472 mA	**400mA**	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-102.9	-162.9
Ch2	-155.1	-100.0	-160.0
Ch3	-155.1	-99.33	-159.3
Ch4	-155.1	-99.9	-159.9

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.4	2.9μV√Hz	√
2		2.0	2.9μV√Hz	√
3		1.6	2.9μV√Hz	√
4		2.0	2.9μV√Hz	√

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM5P
Test Engineer ……RMC
Date ……11/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √ (left hand only)

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM5
Driver board ID	PUM5P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM5P
Monitor board ID	MON267
Monitor board Drawing No/Issue No	D070480_5_K
Monitor board Serial Number	MON267

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

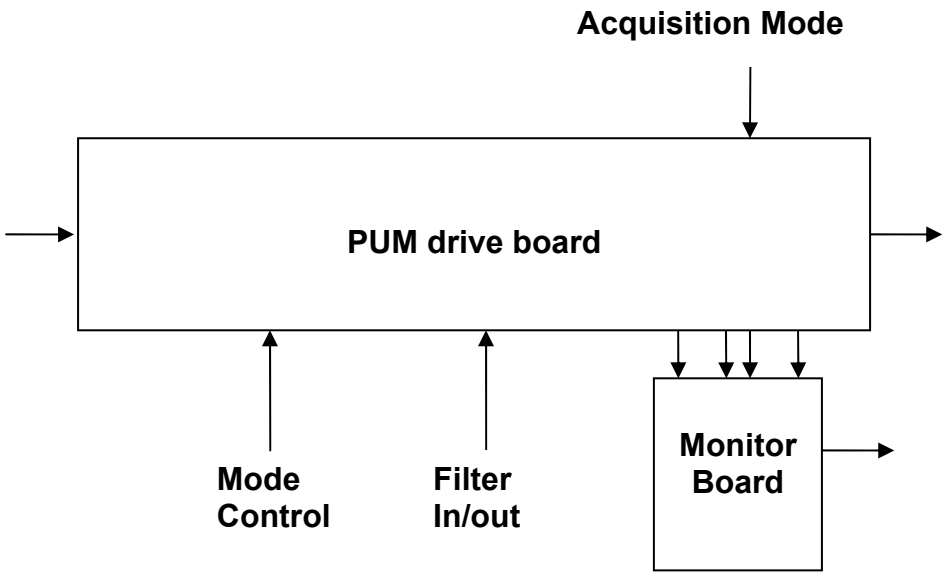
Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

Drive Card ID……...PUM6P
Monitor Card ID ……..MON268.

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

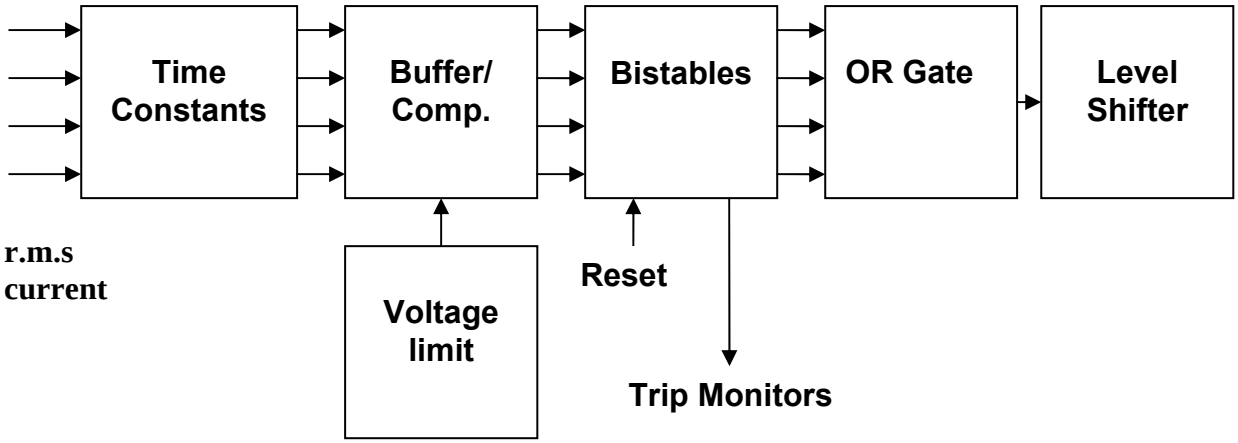
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

WIRE ADDED to connect reset pulse to pin 5 on J7 11/1/11

Links:

Check that the links W4 is present on each channel.

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

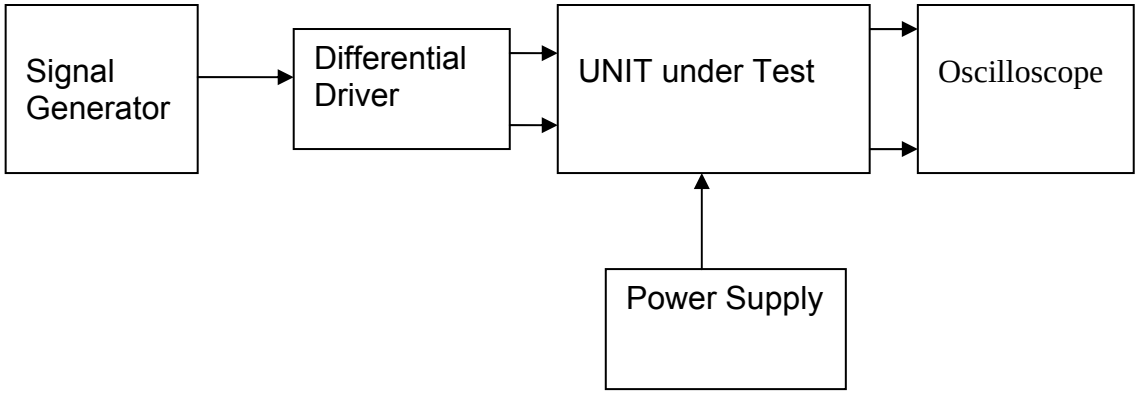
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05 v	√	1.2 mV
+15v TP4	14.91 v	√	1.2 mV
-15v TP6	-15.15 v	√	2.5 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.767 A
-16.5v	0.526 A

If the supplies are correct, proceed to the next test.

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.332	3	0.33v	√
2	0.332	6	0.33v	√
3	0.332	9	0.33v	√
4	0.332	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.195	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	1	0.195v +/- 0.01v	√
2	0.196	4	0.195v +/- 0.01v	√
3	0.195	7	0.195v +/- 0.01v	√
4	0.199	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.34 v
R.M.S. Current in the load	117 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.5 seconds

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.492	24.6 mA
Ch2	0.498	24.9 mA
Ch3	0.496	24.8 mA
Ch4	0.494	24.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.6 mA	**16mA**	√
Ch2	0.656	32.8 mA	**16mA**	√
Ch3	0.655	32.75 mA	**16mA**	√
Ch4	0.653	32.6 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.194	9.7 mA
Ch3	0.195	9.75 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.422	21.1 mA	**16mA**	√
Ch2	0.422	21.1 mA	**16mA**	√
Ch3	0.422	21.1 mA	**16mA**	√
Ch4	0.419	20.95 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.730	36.6 mA	**16mA**	√
Ch2	0.730	36.6 mA	**16mA**	√
Ch3	0.729	36.45 mA	**16mA**	√
Ch4	0.729	36.45 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.749	37.45 mA	**16mA**	√
Ch3	0.749	37.45 mA	**16mA**	√
Ch4	0.749	37.45 mA	**16mA**	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.17	5.89	294 mA
Ch2	4.18	5.91	295 mA
Ch3	4.15	5.87	293 mA
Ch4	4.22	5.96	284 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.57	7.87	393 mA	**400mA**	
Ch2	5.58	7.89	394 mA	**400mA**	
Ch3	5.56	7.86	393 mA	**400mA**	
Ch4	5.62	7.94	397 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**400mA**	√
Ch2	6.68	9.44	472 mA	**400mA**	√
Ch3	6.67	9.43	471 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

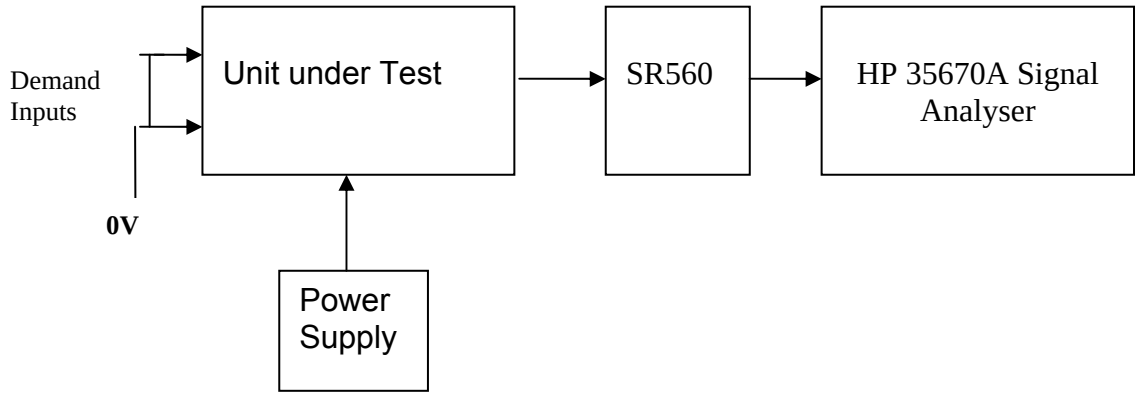
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**400mA**	√
Ch2	6.71	9.49	474 mA	**400mA**	√
Ch3	6.70	9.47	473 mA	**400mA**	√
Ch4	6.72	9.50	475 mA	**400mA**	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.9	-158.9
Ch2	-155.1	-100.5	-160.5
Ch3	-155.1	-100.7	-160.7
Ch4	-155.1	-101.1	-161.1

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.07	2.9μV√Hz	√
2		1.75	2.9μV√Hz	√
3		1.98	2.9μV√Hz	√
4		1.57	2.9μV√Hz	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM6P
Engineer …….....RMC
Date ……12/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. (Left side only)

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM6P
Driver board ID	PUM6P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM6P
Monitor board ID	MON268
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON268

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

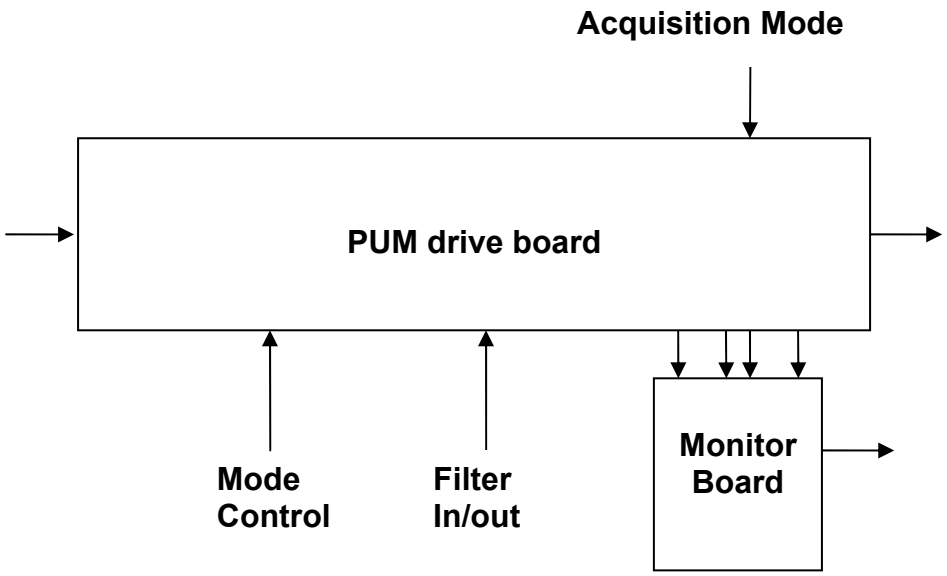
Unit……PUM7P
Test Engineer ……RMC
Date ……12/1/11

Drive Card ID……PUM7P
Monitor Card ID ……..MON269

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

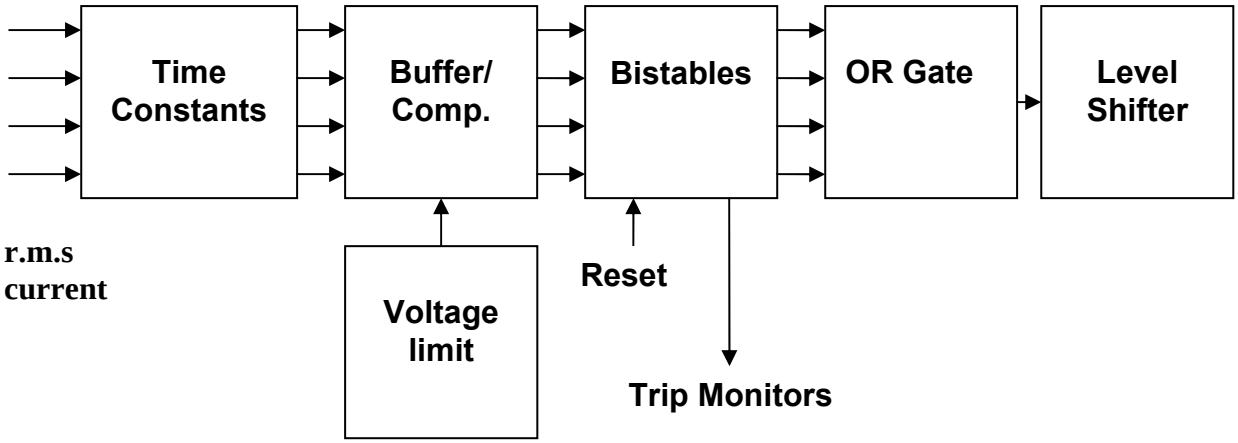
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM7P
Test Engineer ……RMC
Date ……12/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM7P
Test Engineer ……RMC
Date ……12/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

WIRE ADDED to connect reset pulse to pin 5 on J7 11/1/11

Links:

Check that the links W4 is present on each channel.

Unit……PUM7P
Test Engineer ……RMC
Date ……12/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

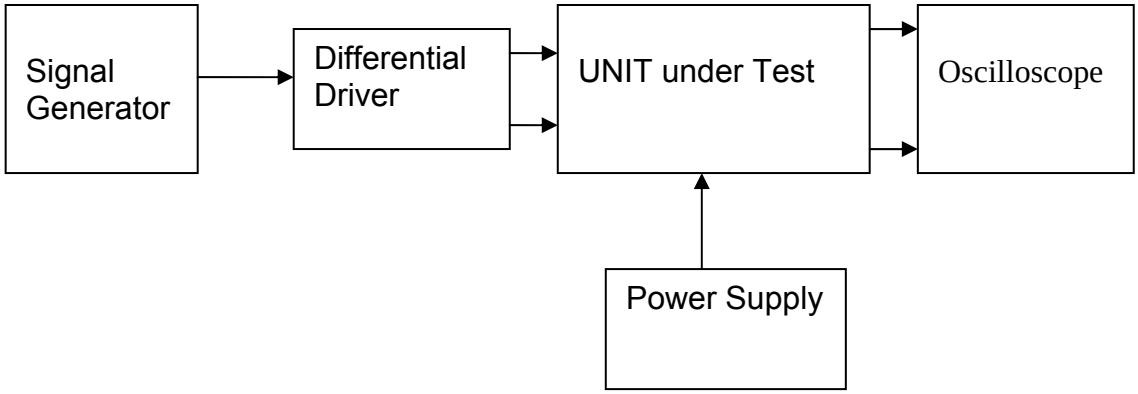
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05 v	√	1.2 mV
+15v TP4	14.93 v	√	1.2 mV
-15v TP6	-15.01 v	√	5 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.568 A
-16.5v	0.522 A

If the supplies are correct, proceed to the next test.

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.335	3	0.33v	√
2	0.334	6	0.33v	√
3	0.335	9	0.33v	√
4	0.334	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.196	2	0.195v +/- 0.01v	√
2	0.197	5	0.195v +/- 0.01v	√
3	0.197	8	0.195v +/- 0.01v	√
4	0.197	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.197	1	0.195v +/- 0.01v	√
2	0.199	4	0.195v +/- 0.01v	√
3	0.198	7	0.195v +/- 0.01v	√
4	0.198	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.338
R.M.S. Current in the load	116.9

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.2 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.8 seconds

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.498	24.9 mA
Ch2	0.494	24.7 mA
Ch3	0.496	24.8 mA
Ch4	0.498	24.9 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.655	32.75 mA	**16mA**	√
Ch2	0.653	32.65 mA	**16mA**	√
Ch3	0.655	32.75 mA	**16mA**	√
Ch4	0.656	32.8 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5	**16mA**	√
Ch2	0.749	37.4	**16mA**	√
Ch3	0.751	37.5	**16mA**	√
Ch4	0.752	37.6	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5	**16mA**	√
Ch2	0.7598	37.9	**16mA**	√
Ch3	0.750	37.5	**16mA**	√
Ch4	0.751	37.5	**16mA**	√

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.197	9.58 mA
Ch2	0.194	9.7 mA
Ch3	0.195	9.75 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.424	21.2 mA	**16mA**	√
Ch2	0.422	21.1 mA	**16mA**	√
Ch3	0.423	21.1 mA	**16mA**	√
Ch4	0.422	21.1 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.729	36.45 mA	**16mA**	√
Ch3	0.730	36.50 mA	**16mA**	√
Ch4	0.731	36.55 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.40 mA	**16mA**	√
Ch2	0.748	37.40 mA	**16mA**	√
Ch3	0.749	73.45 mA	**16mA**	√
Ch4	0.750	37.50 mA	**16mA**	√

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.13	5.84	293 mA
Ch2	4.14	5.85	292 mA
Ch3	4.15	5.86	294 mA
Ch4	4.15	5.86	294 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.55	7.84	392 mA	**400mA**	
Ch2	5.55	7.84	392 mA	**400mA**	
Ch3	5.55	7.84	392 mA	**400mA**	
Ch4	5.55	7.84	392 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**400mA**	√
Ch2	6.67	9.43	471 mA	**400mA**	√
Ch3	6.68	9.44	472 mA	**400mA**	√
Ch4	6.66	9.42	471 mA	**400mA**	√

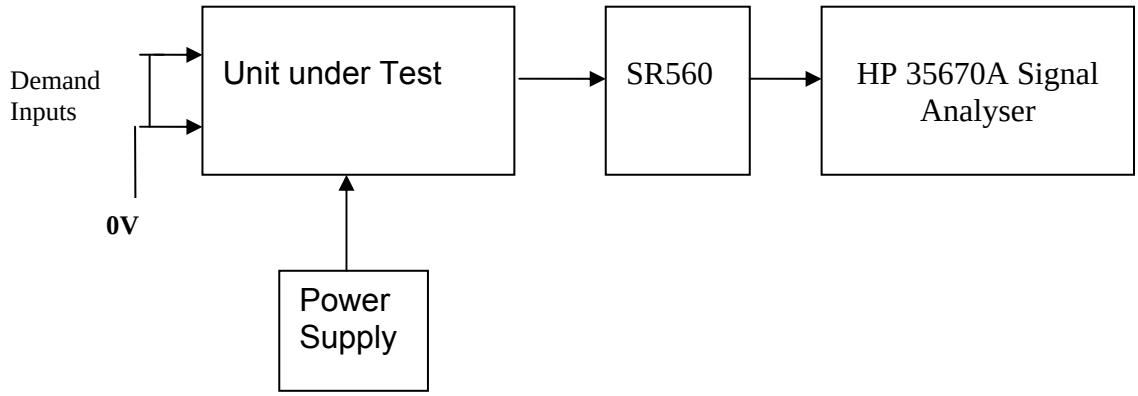
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**400mA**	√
Ch2	6.70	9.47	473 mA	**400mA**	√
Ch3	6.71	9.49	474 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.62	-158.6
Ch2	-155.1	-98.78	-158.8
Ch3	-155.1	-99.21	-159.2
Ch4	-155.1	-94.90	-154.9

Ch4 out of spec by 0.2dB

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM7P
Test Engineer ……RMC
Date ……17/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.79	2.9μV√Hz	√
2		1.87	2.9μV√Hz	√
3		1.88	2.9μV√Hz	√
4		1.98	2.9μV√Hz	√

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM7P
Test Engineer ……RMC
Date ……12/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM7P
Driver board ID	PUM07P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM07P
Monitor board ID	MON269
Monitor board Drawing No/Issue No	D070480_5_K
Monitor board Serial Number	MON269

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

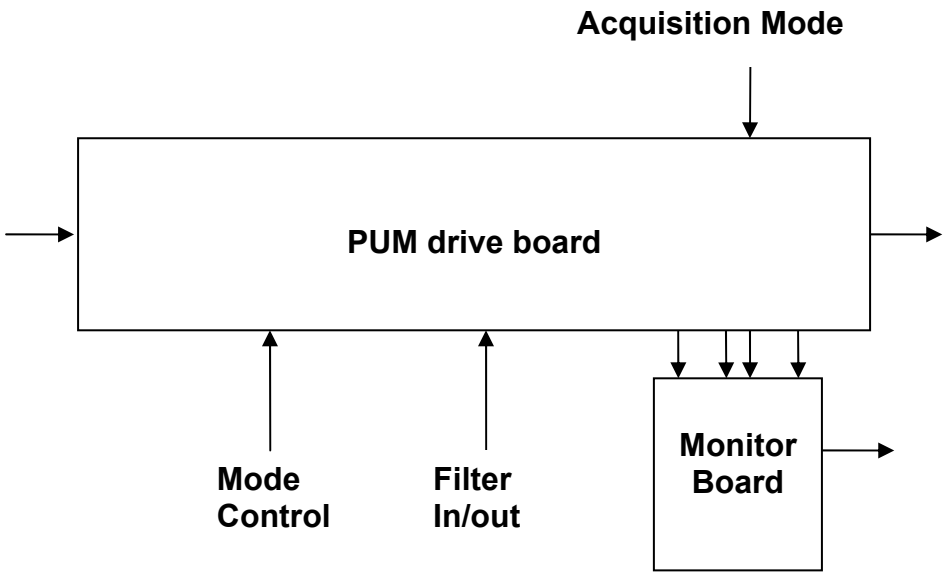
Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

Drive Card ID……PUM8P
Monitor Card ID ……..MON270

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

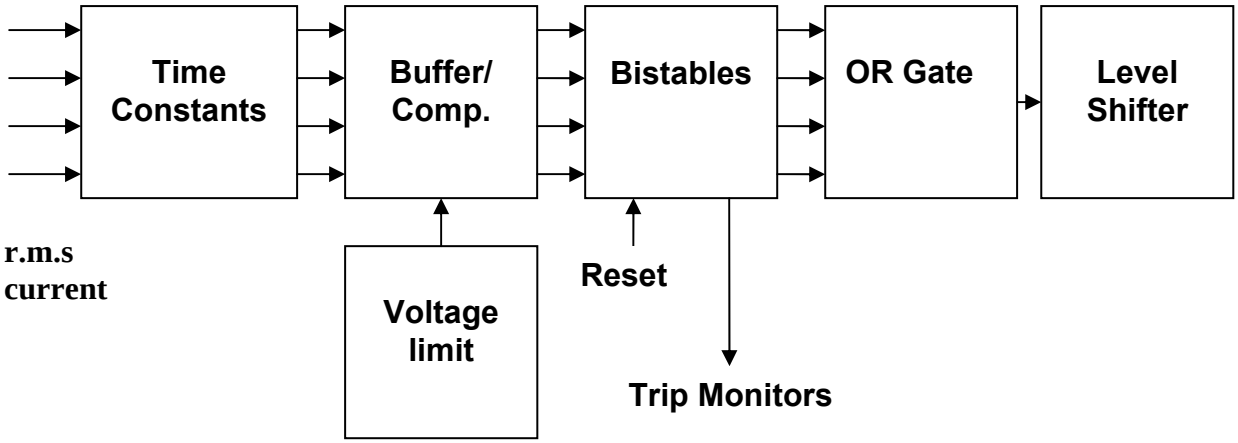
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

OK

Pin 2 on J7 connected to reset pulse

Links:
Check that the links W4 is present on each channel.

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

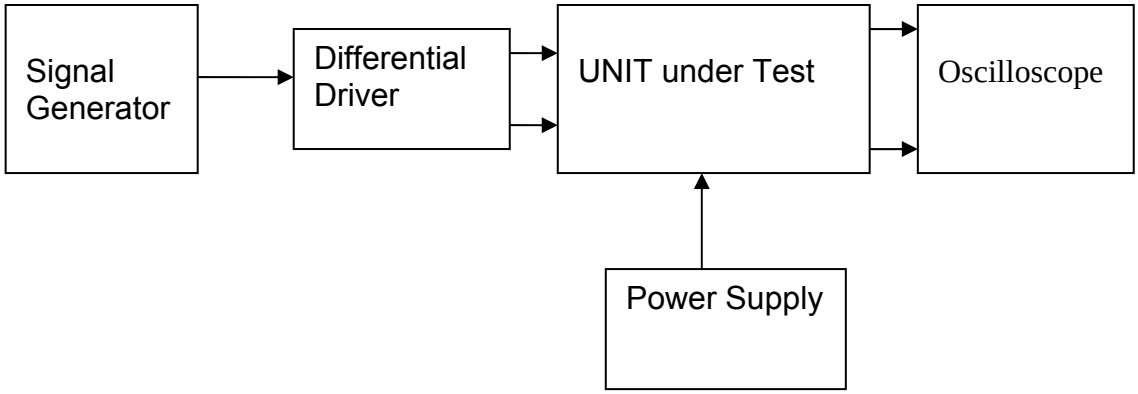
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.05	√	1.5 mV
+15v TP4	14.90	√	1.5 mV
-15v TP6	-15.00	√	5 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.546 A
-16.5v	0.487 A

If the supplies are correct, proceed to the next test.

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.331	6	0.33v	√
3	0.331	9	0.33v	√
4	0.331	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194	2	0.195v +/- 0.01v	√
2	0.194	5	0.195v +/- 0.01v	√
3	0.194	8	0.195v +/- 0.01v	√
4	0.194	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	1	0.195v +/- 0.01v	√
2	0.199	4	0.195v +/- 0.01v	√
3	0.197	7	0.195v +/- 0.01v	√
4	0.198	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.366
R.M.S. Current in the load	118 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.7seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.7 seconds

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.496	24.8 mA
Ch2	0.492	24.6 mA
Ch3	0.498	24.9 mA
Ch4	0.496	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.65	32.5 mA	**16mA**	√
Ch2	0.65	32.5 mA	**16mA**	√
Ch3	0.65	32.5 mA	**16mA**	√
Ch4	0.65	32.5 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	**16mA**	√
Ch2	0.75	37.5 mA	**16mA**	√
Ch3	0.75	37.5 mA	**16mA**	√
Ch4	0.75	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	**16mA**	√
Ch2	0.75	37.5 mA	**16mA**	√
Ch3	0.75	37.5 mA	**16mA**	√
Ch4	0.75	37.5 mA	**16mA**	√

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.193	9.65 mA
Ch3	0.196	9.8 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.420	21 mA	**16mA**	√
Ch2	0.420	21 mA	**16mA**	√
Ch3	0.423	21 mA	**16mA**	√
Ch4	0.421	21 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.729	36.45 mA	**16mA**	√
Ch3	0.729	36.45 mA	**16mA**	√
Ch4	0.73	36.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.749	37.45 mA	**16mA**	√
Ch3	0.748	37.4 mA	**16mA**	√
Ch4	0.75	37.5 mA	**16mA**	√

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.19	5.92	296
Ch2	4.13	5.84	292
Ch3	4.15	5.86	293
Ch4	4.17	5.89	294

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.59	7.90	395	**400mA**	
Ch2	5.54	7.83	391	**400mA**	
Ch3	5.55	7.84	392	**400mA**	
Ch4	5.57	7.78	393	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.42	470	**400mA**	√
Ch2	6.66	9.42	470	**400mA**	√
Ch3	6.66	9.42	470	**400mA**	√
Ch4	6.68	9.44	472	**400mA**	√

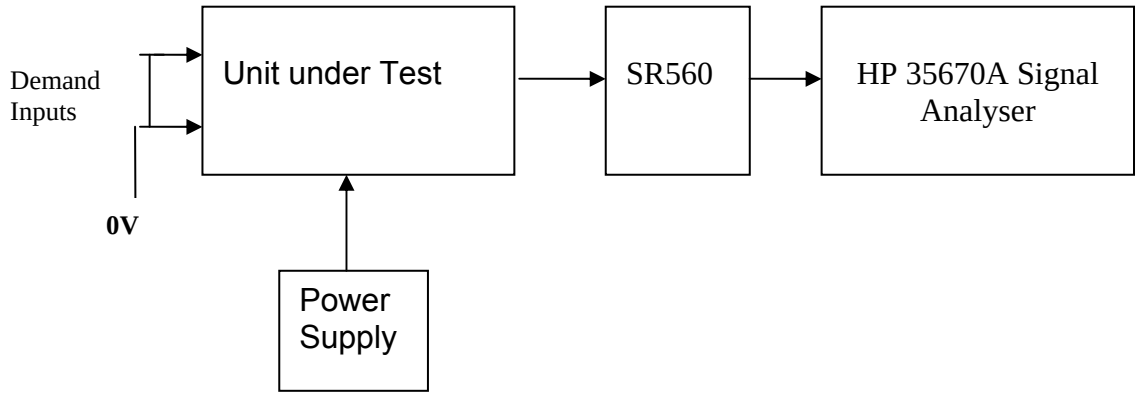
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473	**400mA**	√
Ch2	6.69	9.46	473	**400mA**	√
Ch3	6.68	9.44	472	**400mA**	√
Ch4	6.70	9.47	473	**400mA**	√

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.6	-158.8
Ch2	-155.1	-97.4	-157.4
Ch3	-155.1	-97.4	-157.4
Ch4	-155.1	-97.3	-157.3

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……...PUM8P
Test Engineer ……RMC
Date ……18/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.17	2.9μV√Hz	√
2		1.83	2.9μV√Hz	√
3		2.53	2.9μV√Hz	√
4		1.83	2.9μV√Hz	√

Unit……...PUM8P
Test Engineer ……RMC
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……...PUM8P
Test Engineer ……RMC
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14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM8P
Driver board ID	PUM 08P
Driver board Drawing No/Issue No	D070463_07_K
Driver board Serial Number	PUM 08P
Monitor board ID	MON270
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON270

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

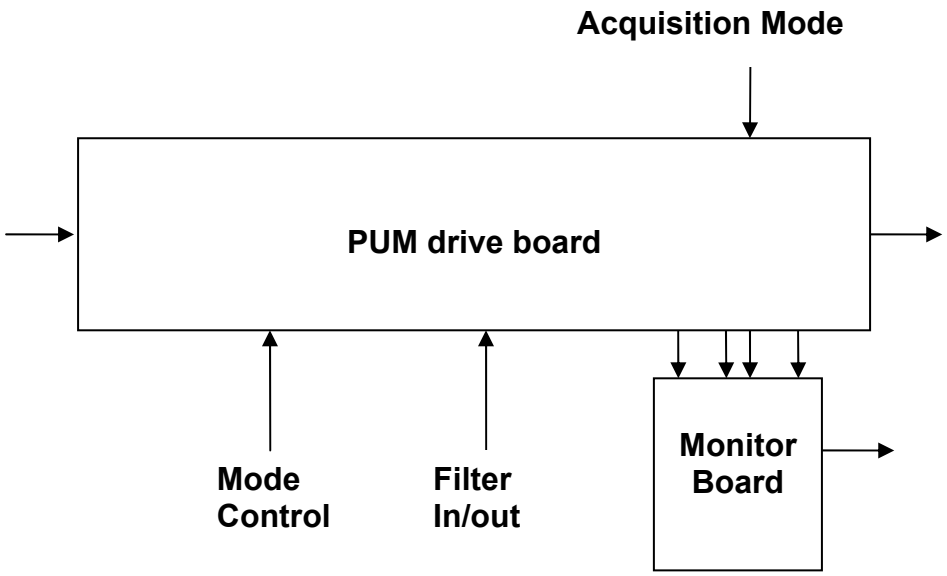
Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

Drive Card ID……PUM9P
Monitor Card ID ……..MON265

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

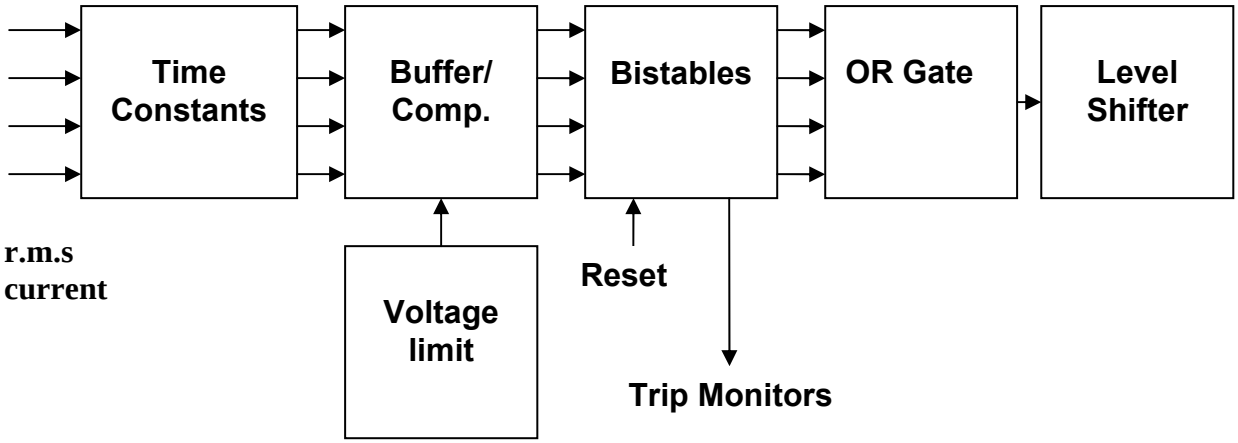
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Wire added to link pin 2 on J7 with the reset pulse.

Channel 3 IC3 and IC4 changed due to offsets

Chanel 1 IC3 and IC4 changed because of output noise

Channel 4 IC4 changed because of oscillation

Links:

Check that the links W4 is present on each channel.

√Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

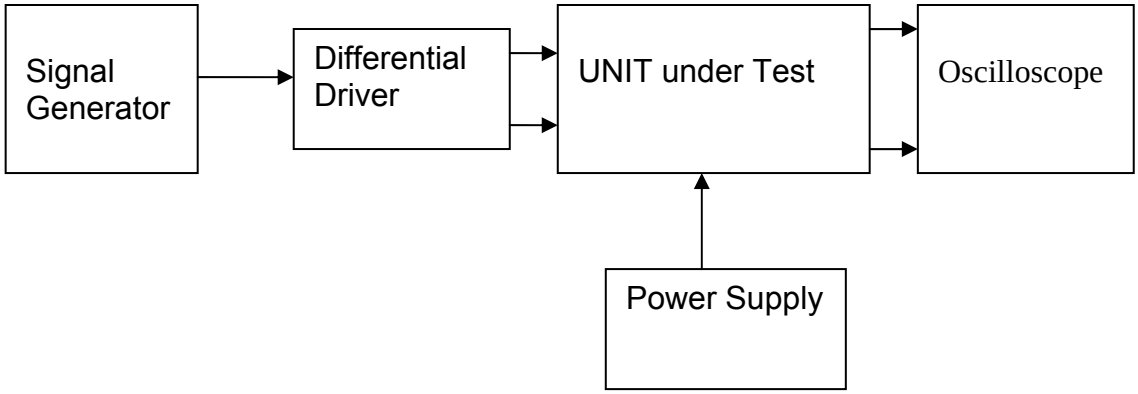
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.02 v	√	1.2 mV
+15v TP4	+14.96 v	√	2 mV
-15v TP6	-15.10 v	√	5 mV

All Outputs smooth DC, no oscillation?	√

Pick up at about 50KHz intermittently seen – thought to be environmental

Record Power Supply Currents

Supply	Current
+16.5v	0.566 A
-16.5v	0.519 A

If the supplies are correct, proceed to the next test.

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.331 v	3	0.33v	√
2	0.332 v	6	0.33v	√
3	0.332 v	9	0.33v	√
4	0.331 v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195 v	2	0.195v +/- 0.01v	√
2	0.195 v	5	0.195v +/- 0.01v	√
3	0.195 v	8	0.195v +/- 0.01v	√
4	0.195 v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.197 v	1	0.195v +/- 0.01v	√
2	0.198 v	4	0.195v +/- 0.01v	√
3	0.197 v	7	0.195v +/- 0.01v	√
4	0.197 v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.33 v
R.M.S. Current in the load	116.5 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	2.7 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.4 seconds

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.488 v	24.4 mA
Ch2	0.497 v	24.8 mA
Ch3	0.499 v	24.9 mA
Ch4	0.494 v	24.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.649 v	32.4 mA	**16mA**	√
Ch2	0.655 v	32.7 mA	**16mA**	√
Ch3	0.656 v	32.8 mA	**16mA**	√
Ch4	0.654 v	32.7 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749 v	37.45 mA	**16mA**	√
Ch2	0.751 v	37.5 mA	**16mA**	√
Ch3	0.750 v	37.5 mA	**16mA**	√
Ch4	0.751 v	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748 v	37.4 mA	**16mA**	√
Ch2	0.751 v	37.5 mA	**16mA**	√
Ch3	0.750 v	37.5 mA	**16mA**	√
Ch4	0.751 v	37.5 mA	**16mA**	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.191 v	9.55 mA
Ch2	0.195 v	9.75 mA
Ch3	0.196 v	9.80 mA
Ch4	0.195 v	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.417 v	20.85 mA	**16mA**	√
Ch2	0.422 v	21.10 mA	**16mA**	√
Ch3	0.423 v	21.15 mA	**16mA**	√
Ch4	0.421 v	21.05 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.727 v	36.5 mA	**16mA**	√
Ch2	0.730 v	36.5 mA	**16mA**	√
Ch3	0.729 v	36.4 mA	**16mA**	√
Ch4	0.730 v	36.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.747 v	37.3 mA	**16mA**	√
Ch2	0.750 v	37.5 mA	**16mA**	√
Ch3	0.748 v	37.4 mA	**16mA**	√
Ch4	0.749 v	37.4 mA	**16mA**	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……19/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.155	5.876	293 mA
Ch2	4.176	5.905	295 mA
Ch3	4.191	5.926	296 mA
Ch4	4.197	5.935	296 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.553	7.853	392 mA	**400mA**	√
Ch2	5.577	7.887	394 mA	**400mA**	√
Ch3	5.582	7.894	394 mA	**400mA**	√
Ch4	5.584	7.896	395 mA	**400mA**	√

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.418	471 mA	**400mA**	√
Ch2	6.68	9.446	472 mA	**400mA**	√
Ch3	6.68	9.446	472 mA	**400mA**	√
Ch4	6.66	9.418	471 mA	**400mA**	√

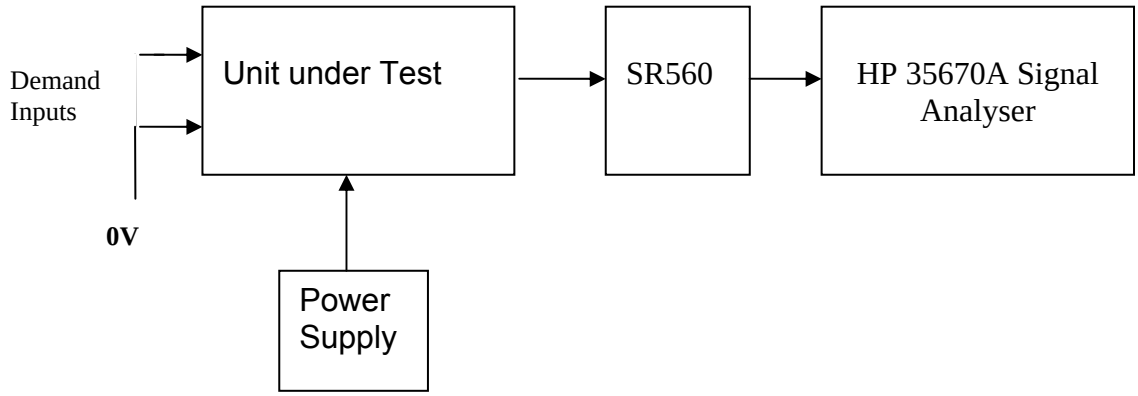
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.461	473 mA	**400mA**	√
Ch2	6.71	9.489	474 mA	**400mA**	√
Ch3	6.70	9.475	473 mA	**400mA**	√
Ch4	6.69	9.461	473 mA	**400mA**	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……2/3/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-101.5	-161.5
Ch2	-155.1	-100.8	-160.8
Ch3	-155.1	-99.9	-159.9
Ch4	-155.1	-100.1	-160.1

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……...PUM9P
Test Engineer ……RMC
Date ……2/3/11

Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.91	2.9μV√Hz	√
2		1.87	2.9μV√Hz	√
3		2.00	2.9μV√Hz	√
4		1.98	2.9μV√Hz	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……2/3/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……...PUM9P
Test Engineer ……RMC
Date ……2/3/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM9P
Driver board ID	PUM9P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM9P
Monitor board ID	Mon265
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	Mon265

10. Check the security of any modification wires. √

11. Visually inspect. √
12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

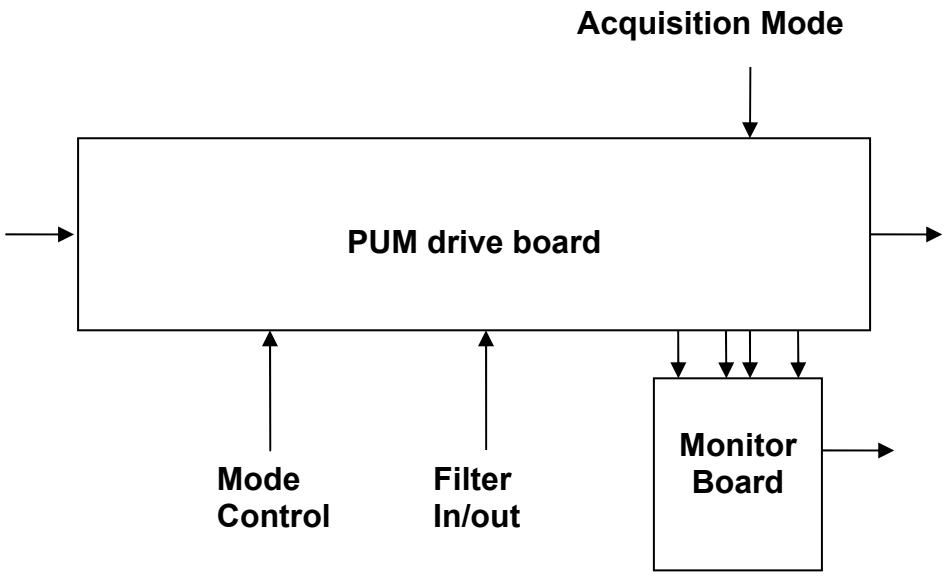
Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

Drive Card ID……PUM10P
Monitor Card ID ……..Mon266

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

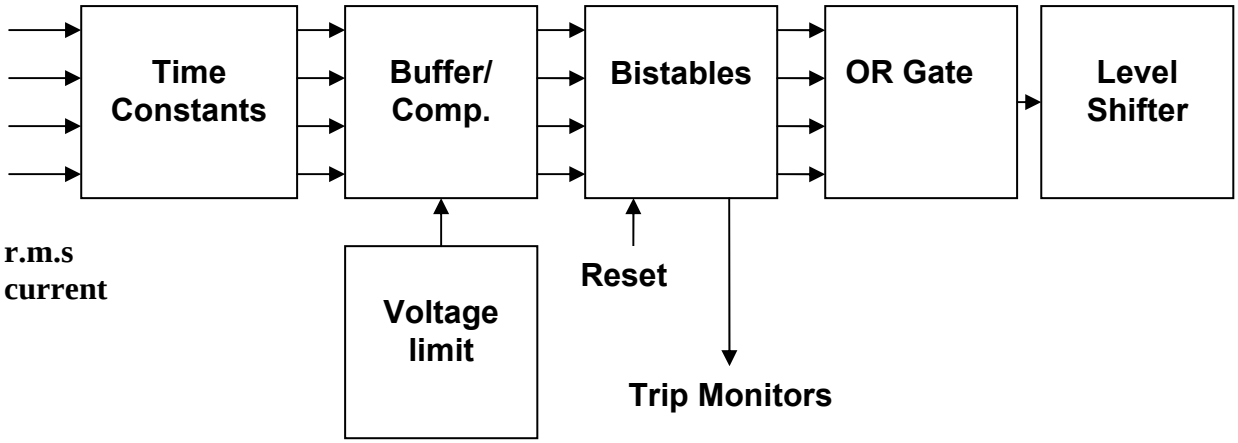
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Wire added to link pin 2 on J7 with the reset pulse.

IC 15 (40106) in trip circuit failed during test.

Replaced. Some unconnected pads lifted during removal.

Works well on retest (23/2/11)

Links:

Check that the links W4 is present on each channel.

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

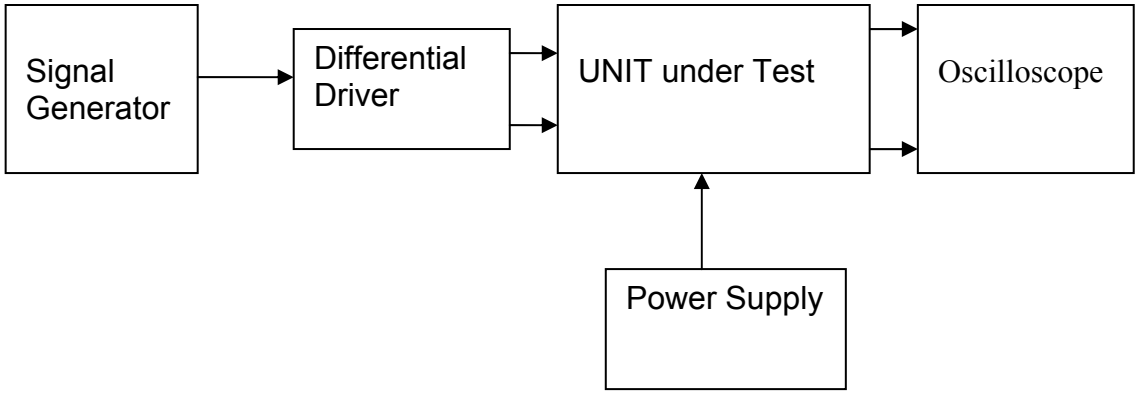
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.01 v	√	2 mV
+15v TP4	+14.92 v	√	2 mV
-15v TP6	-14.88 v	√	5 mV

All Outputs smooth DC, no oscillation?	No oscillations

Common mode pick up present.

Record Power Supply Currents

Supply	Current
+16.5v	0.696 A
-16.5v	0.442 A

If the supplies are correct, proceed to the next test.

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.331	3	0.33v	√
2	0.331	6	0.33v	√
3	0.331	9	0.33v	√
4	0.330	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194	2	0.195v +/- 0.01v	√
2	0.194	5	0.195v +/- 0.01v	√
3	o.194	8	0.195v +/- 0.01v	√
4	o.193	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	o.198	1	0.195v +/- 0.01v	√
2	0.199	4	0.195v +/- 0.01v	√
3	0.198	7	0.195v +/- 0.01v	√
4	0.197	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11 – retest 23/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

40106 failed during test. Replaced. Results below are for retest.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.36 v
R.M.S. Current in the load	118 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.
Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.7 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.7 seconds

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.493	24.6 mA
Ch2	0.496	24.8 mA
Ch3	0.496	24.8 mA
Ch4	0.493	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.652	32.6 mA	**16mA**	√
Ch2	0.655	32.7 mA	**16mA**	√
Ch3	0.655	32.7 mA	**16mA**	√
Ch4	0.653	32.6 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.195	9.75 mA
Ch3	0.195	9.75 mA
Ch4	0.194	9.70 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.420	21.0 mA	**16mA**	√
Ch2	0.422	21.1 mA	**16mA**	√
Ch3	0.422	21.1 mA	**16mA**	√
Ch4	0.422	21.1 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	39.6 mA	**16mA**	√
Ch2	0.725	36.2 mA	**16mA**	√
Ch3	0.730	36.5 mA	**16mA**	√
Ch4	0.730	36.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.749	37.4 mA	**16mA**	√
Ch3	0.749	37.4 mA	**16mA**	√
Ch4	0.749	37.4 mA	**16mA**	√

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.19	5.92	296 mA
Ch2	4.18	5.91	295 mA
Ch3	4.19	5.92	296 mA
Ch4	4.19	5.92	296 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.56	7.86	393 mA	**400mA**	
Ch2	5.58	7.89	394 mA	**400mA**	
Ch3	5.58	7.89	394 mA	**400mA**	
Ch4	5.59	7.90	395 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.42	471 mA	**400mA**	√
Ch2	6.68	9.44	472 mA	**400mA**	√
Ch3	6.68	9.44	472 mA	**400mA**	√
Ch4	6.68	9.44	472 mA	**400mA**	√

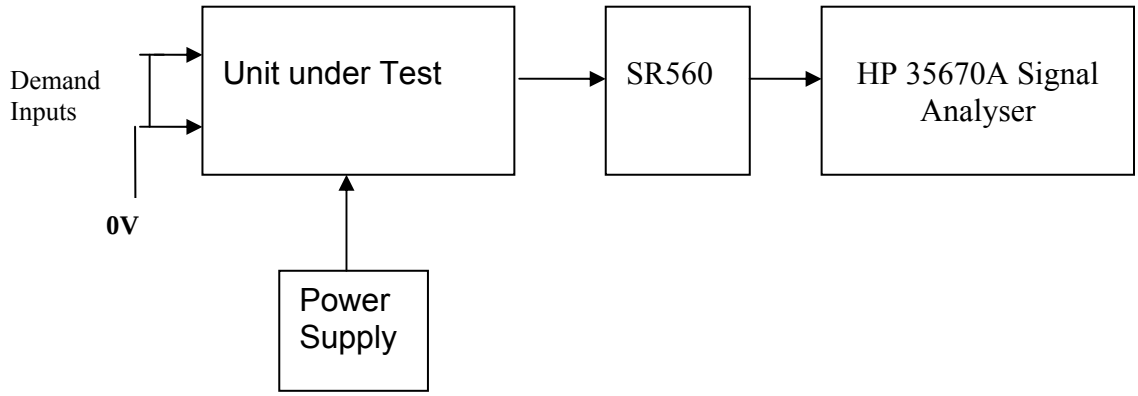
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	**400mA**	√
Ch2	6.71	9.49	474 mA	**400mA**	√
Ch3	6.71	9.49	474 mA	**400mA**	√
Ch4	6.72	9.50	475 mA	**400mA**	√

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-99.8	-159.8
Ch2	-155.1	-98.2	-158.2
Ch3	-155.1	-100.3	-160.3
Ch4	-155.1	-98.5	-158.5

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV/√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.92	2.9μV√Hz	√
2		1.74	2.9μV√Hz	√
3		1.66	2.9μV√Hz	√
4		1.32	2.9μV√Hz	√

Note high levels of 50 Hz interference made it necessary to make differential measurements.

Unit……PUM10P
Test Engineer ……RMC
Date ……23/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM10P
Test Engineer ……RMC
Date ……25/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM10P
Driver board ID	PUM10P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM10P
Monitor board ID	MON266
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON266

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

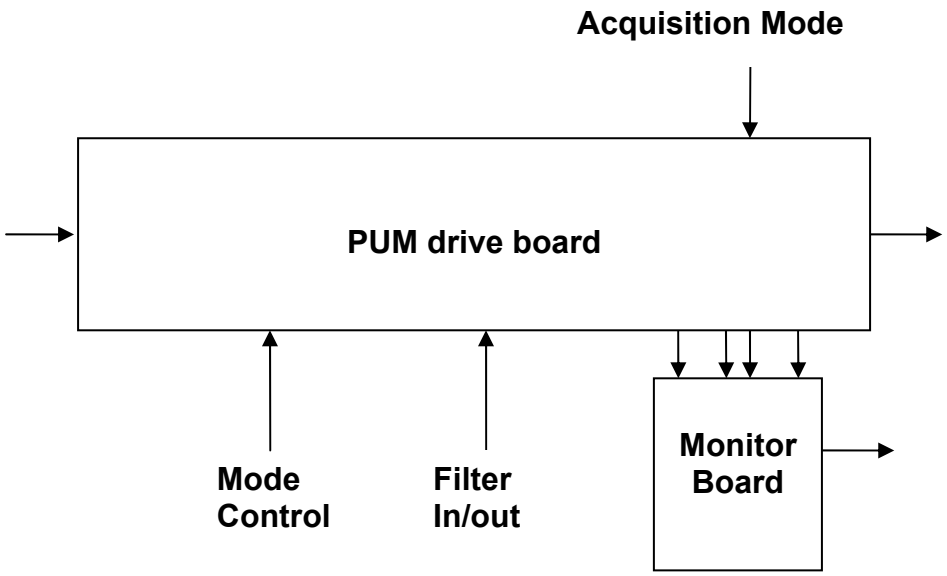
Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

Drive Card ID……PUM11P
Monitor Card ID ……..MON263

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

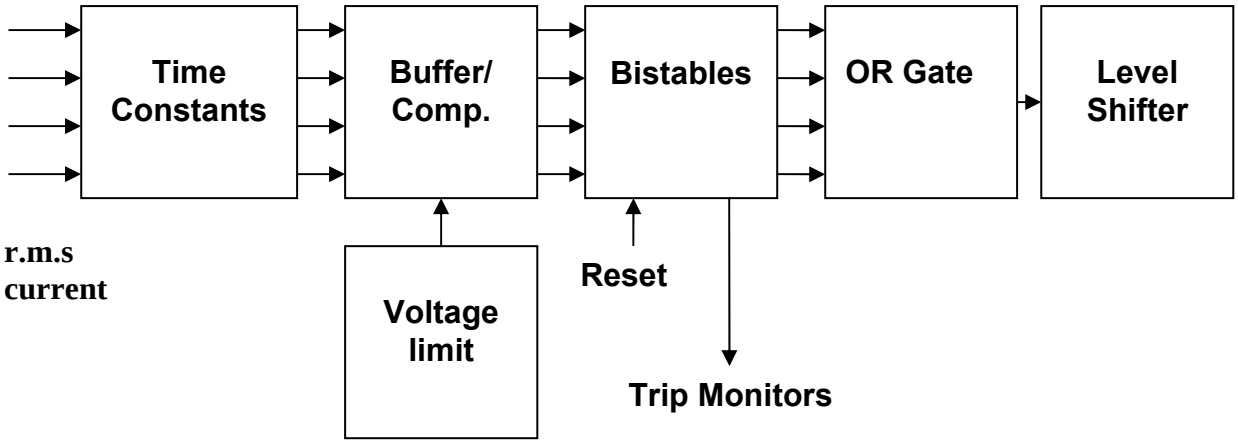
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Wire added to link pin 2 on J7 with the reset pulse.

Links:

Check that the links W4 is present on each channel.

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

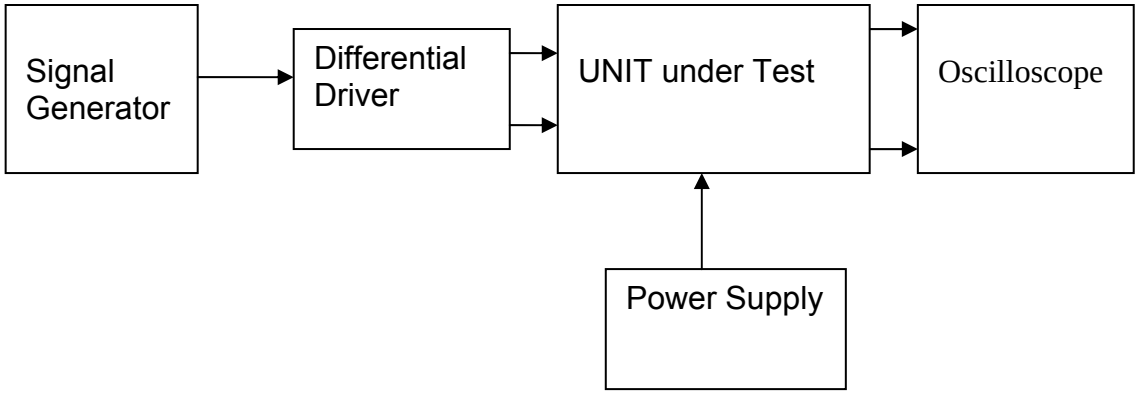
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM11P
Test Engineer ……RMC
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.03	√	1.2 uV
+15v TP4	+14.92	√	1.15 uV
-15v TP6	-15.07	√	4 uV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.72 A
-16.5v	0.46 A

If the supplies are correct, proceed to the next test.

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.332 v	3	0.33v	√
2	0.332 v	6	0.33v	√
3	0.331 v	9	0.33v	√
4	0.331 v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195 v	2	0.195v +/- 0.01v	√
2	0.196 v	5	0.195v +/- 0.01v	√
3	0.195 v	8	0.195v +/- 0.01v	√
4	0.195 v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.200 v	1	0.195v +/- 0.01v	√
2	0.194 v	4	0.195v +/- 0.01v	√
3	0.195 v	7	0.195v +/- 0.01v	√
4	0.195 v	10	0.195v +/- 0.01v	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.31 v
R.M.S. Current in the load	115.5 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.7 seconds

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.498 v	24.9 mA
Ch2	0.496 v	24.8 mA
Ch3	0.498 v	24.9 mA
Ch4	0.493 v	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.655v	32.75 mA	**16mA**	√
Ch2	0.655 v	32.75 mA	**16mA**	√
Ch3	0.656 v	32.80 mA	**16mA**	√
Ch4	0.653 v	32.60 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751 v	37.5 mA	**16mA**	√
Ch2	0.751 v	37.5 mA	**16mA**	√
Ch3	0.752 v	37.6 mA	**16mA**	√
Ch4	0.751 v	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751 v	37.5 mA	**16mA**	√
Ch2	0.750 v	37.5 mA	**16mA**	√
Ch3	0.751 v	37.5 mA	**16mA**	√
Ch4	0.750 v	37.5 mA	**16mA**	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195 v	9.75 mA
Ch2	0.195 v	9.75 mA
Ch3	0.196 v	9.80 mA
Ch4	0.191 v	9.55 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.421 v	21.05 mA	**16mA**	√
Ch2	0.421 v	21.05 mA	**16mA**	√
Ch3	0.423 v	21.15 mA	**16mA**	√
Ch4	0.416 v	20.80 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729 v	36.4 mA	**16mA**	√
Ch2	0.730 v	36.5 mA	**16mA**	√
Ch3	0.730 v	36.5 mA	**16mA**	√
Ch4	0.729 v	36.4 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749 v	37.4 mA	**16mA**	√
Ch2	0.749 v	37.4 mA	**16mA**	√
Ch3	0.749 v	37.4 mA	**16mA**	√
Ch4	0.749 v	37.4 mA	**16mA**	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.15	5.868	393 mA
Ch2	4.17	5.897	295 mA
Ch3	4.14	5.854	292 mA
Ch4	4.18	5.911	295 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.55	7.848	392 mA	**400mA**	
Ch2	5.57	7.877	393 mA	**400mA**	
Ch3	5.55	7.848	392 mA	**400mA**	
Ch4	5.58	7.891	394 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.432	471 mA	**400mA**	√
Ch2	6.67	9.432	471 mA	**400mA**	√
Ch3	6.67	9.432	471 mA	**400mA**	√
Ch4	6.67	9.432	471 mA	**400mA**	√

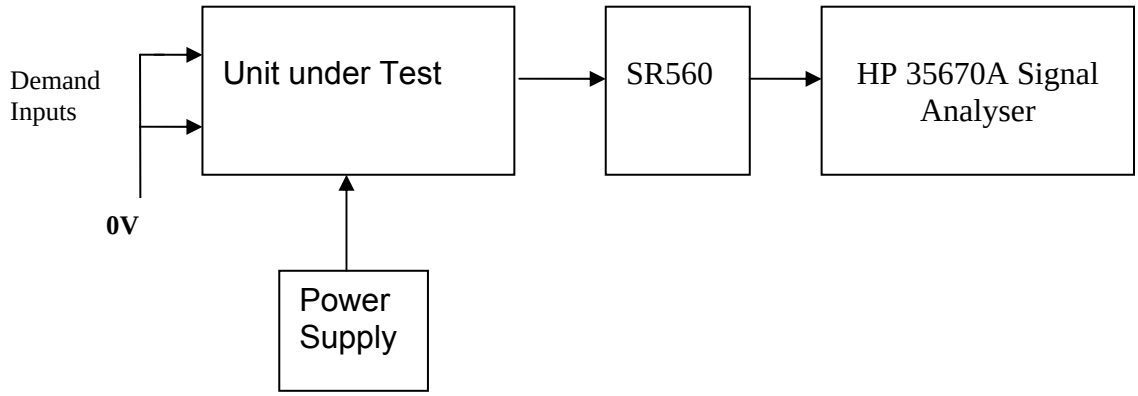
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.461	473 mA	**400mA**	√
Ch2	6.69	9.461	473 mA	**400mA**	√
Ch3	6.70	9.475	473 mA	**400mA**	√
Ch4	6.70	9.475	473 mA	**400mA**	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-99.1	-159.1
Ch2	-155.1	-100.2	-160.2
Ch3	-155.1	-100.9	-160.9
Ch4	-155.1	-99.3	-159.3

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.86	2.9μV√Hz	√
2		1.56	2.9μV√Hz	√
3		1.77	2.9μV√Hz	√
4		1.89	2.9μV√Hz	√

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Some fluctuations observed on positive inputs on channels 3 & 4, probably due to a test equipment contact around 3v and 9v.

Problem did not recur on repeated retests.

Unit……PUM11P
Test Engineer ……RMC
Date ……26/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections.

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM11P
Driver board ID	PUM11P
Driver board Drawing No/Issue No	D070480_05_K
Driver board Serial Number	PUM11P
Monitor board ID	Mon263
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	Mon263

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

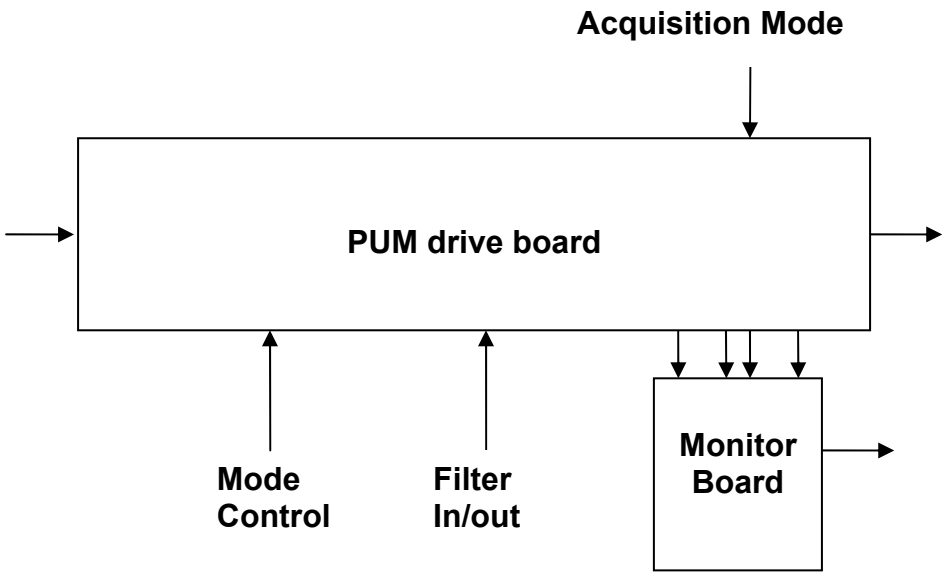
Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

Drive Card ID……PUM12P
Monitor Card ID ……..Mon264P

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

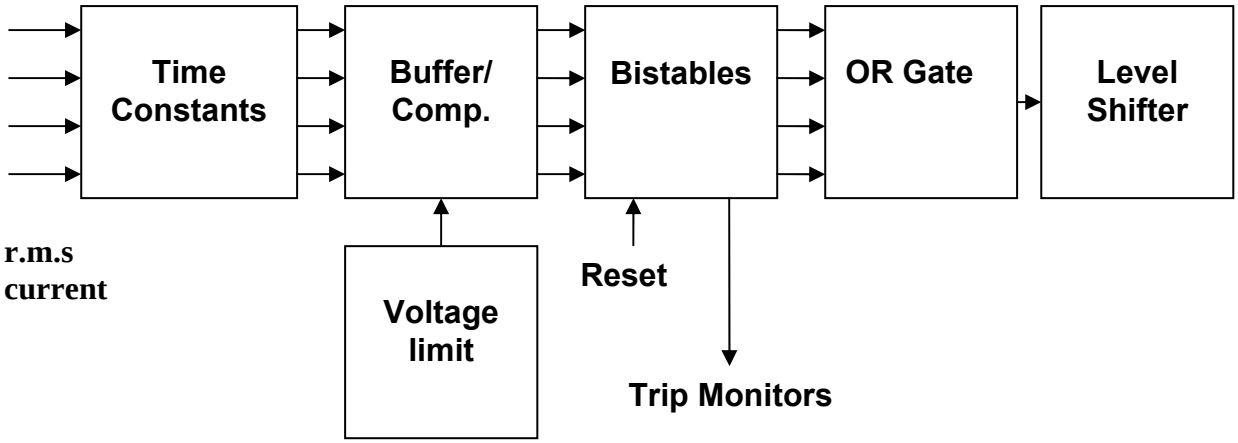
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Wire added to link pin 2 on J7 with the reset pulse.

Links:

Check that the links W4 is present on each channel.

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

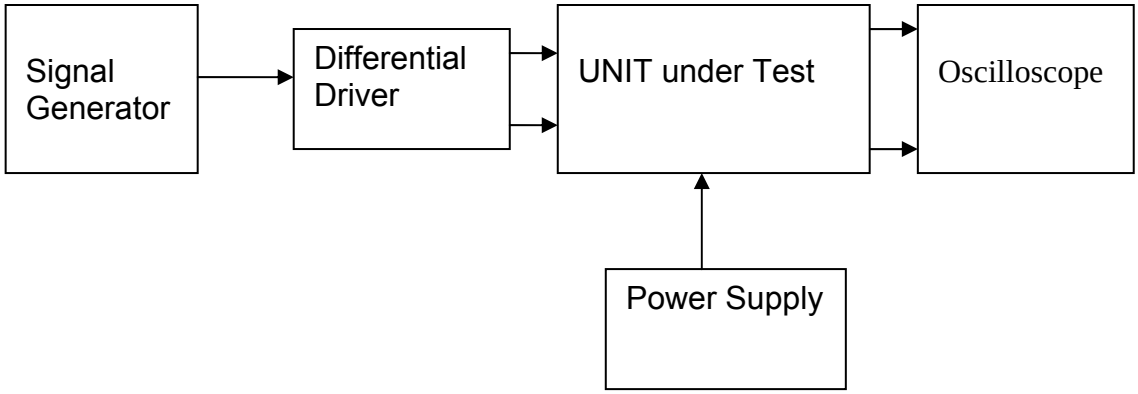
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.03 v	√	1.4 mV
+15v TP4	+14.89 v	√	1.5 mV
-15v TP6	-15.157 v	√	6 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.574 A
-16.5v	0.527 A

If the supplies are correct, proceed to the next test.

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.331	3	0.33v	√
2	0.332	6	0.33v	√
3	0.332	9	0.33v	√
4	0.332	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.196	2	0.195v +/- 0.01v	√
2	0.196	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.197	1	0.195v +/- 0.01v	√
2	0.196	4	0.195v +/- 0.01v	√
3	0.197	7	0.195v +/- 0.01v	√
4	0.199	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.34 v
R.M.S. Current in the load	117 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.6 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.7 seconds

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494 v	24.7 mA
Ch2	0.493 v	24.65 mA
Ch3	0.496 v	24.8 mA
Ch4	0.492 v	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654 v	32.70 mA	**16mA**	√
Ch2	0.653 v	32.65 mA	**16mA**	√
Ch3	0.655 v	32.75 mA	**16mA**	√
Ch4	0.653 v	32.65 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751 v	37.55 mA	**16mA**	√
Ch2	0.751 v	37.55 mA	**16mA**	√
Ch3	0.751 v	37.55 mA	**16mA**	√
Ch4	0.751 v	37.55 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751 v	37.55 mA	**16mA**	√
Ch2	0.751 v	37.55 mA	**16mA**	√
Ch3	0.751 v	37.55 mA	**16mA**	√
Ch4	0.751 v	37.55 mA	**16mA**	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194 v	9.70 mA
Ch2	0.192 v	9.60 mA
Ch3	0.197 v	9.85 mA
Ch4	0.195 v	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	o.421 v	21.5 mA	**16mA**	√
Ch2	0.418 v	20.9 mA	**16mA**	√
Ch3	0.424 v	21.2 mA	**16mA**	√
Ch4	0.424 v	21.2 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.730 v	36.5 mA	**16mA**	√
Ch2	0.730 v	36.5 mA	**16mA**	√
Ch3	0.730 v	36.5 mA	**16mA**	√
Ch4	0.731 v	36.6 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749 v	37.4 mA	**16mA**	√
Ch2	0.749 v	37.4 mA	**16mA**	√
Ch3	0.749 v	37.4 mA	**16mA**	√
Ch4	0.750 v	37.5 mA	**16mA**	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.13	5.89	292 mA
Ch2	4.16	5.88	294 mA
Ch3	4.14	5.85	293 mA
Ch4	4.14	5.85	293 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.54	7.83	392 mA	**400mA**	
Ch2	5.55	7.85	392.5	**400mA**	
Ch3	5.55	7.85	392.5	**400mA**	
Ch4	5.54	7.83	392 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.65	9.40	470 mA	**400mA**	√
Ch2	6.58	9.30	465 mA	**400mA**	√
Ch3	6.66	9.41	471 mA	**400mA**	√
Ch4	6.68	9.44	472 mA	**400mA**	√

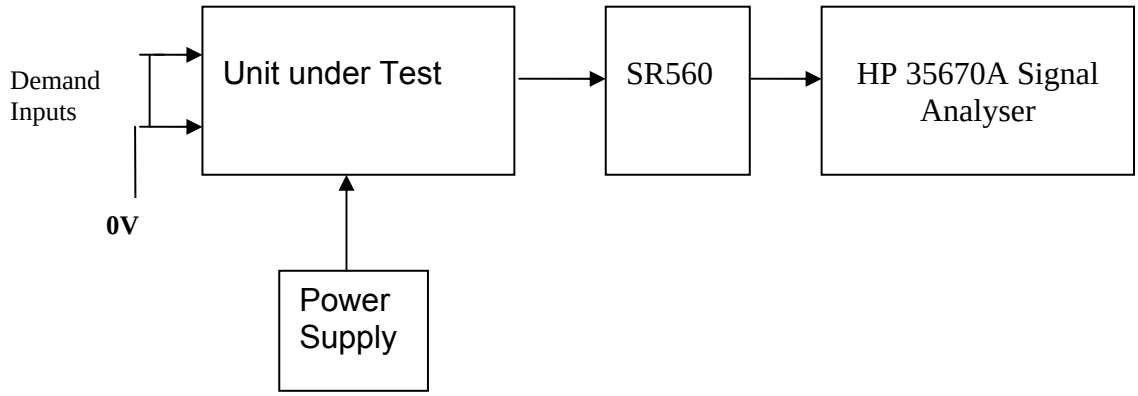
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.41	471 mA	**400mA**	√
Ch2	6.69	9.46	473 mA	**400mA**	√
Ch3	6.67	9.43	471 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.5	-158.5
Ch2	-155.1	-99.8	-159.8
Ch3	-155.1	-98.2	-158.2
Ch4	-155.1	-98.9	-158.9

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.6	2.9μV√Hz	√
2		1.4	2.9μV√Hz	√
3		1.7	2.9μV√Hz	√
4		1.6	2.9μV√Hz	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM12P
Test Engineer ……RMC
Date ……27/1/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM12P
Driver board ID	PUM12P
Driver board Drawing No/Issue No	D070483_7_K
Driver board Serial Number	PUM12P
Monitor board ID	MON264
Monitor board Drawing No/Issue No	D070480_5_K
Monitor board Serial Number	MON264

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

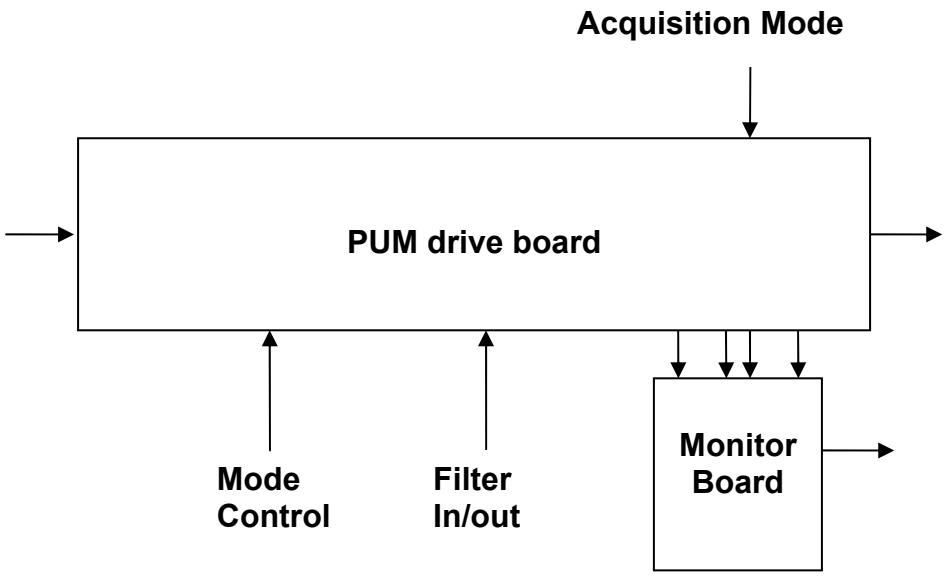
Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

Drive Card ID……PUM13P
Monitor Card ID ……..MON84

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

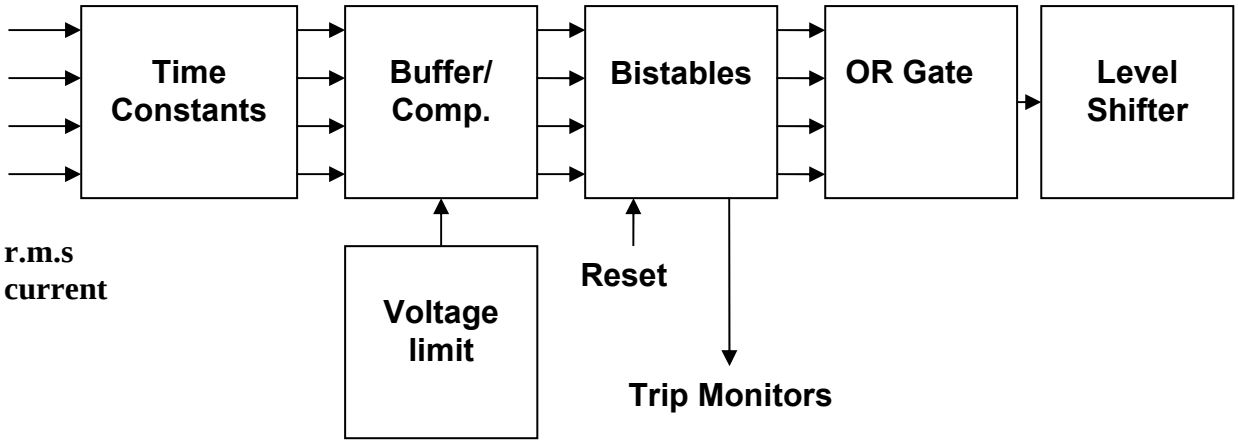
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Ok

On initial tests, channel 1 of the original monitor board was found to be noisy. The monitor board (Mon 61) was removed, and replaced by MON78.
Relevant tests (Section 8 and the noise monitor part of section 12) were re-run.

Buffer IC10 channel 1 on driver board was found to be noisy and changed.

Links:
Check that the links W4 is present on each channel.

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

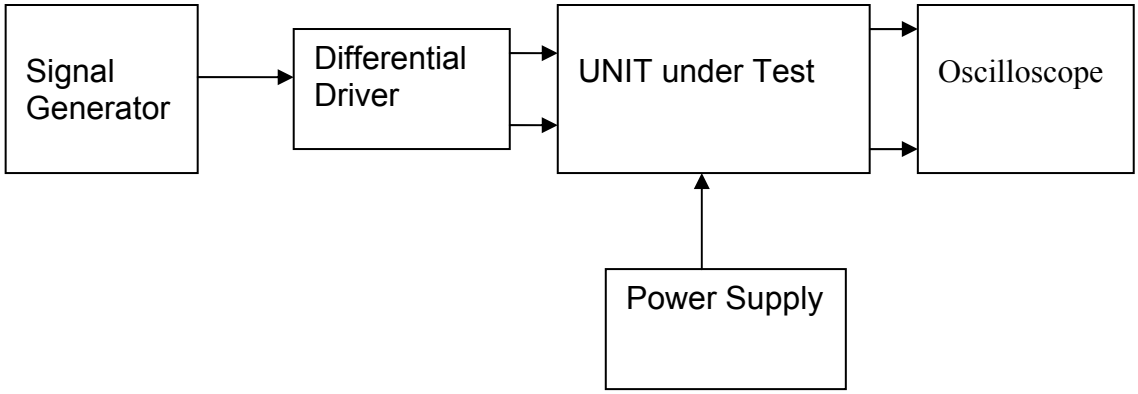
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.039	√	2 mV
+15v TP4	14.79	√	2 mV
-15v TP6	-15.08	√	7 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.574 A
-16.5v	0.528 A

If the supplies are correct, proceed to the next test.

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.195	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.199	1	0.195v +/- 0.01v	√
2	0.201	4	0.195v +/- 0.01v	√
3	0.195	7	0.195v +/- 0.01v	√
4	0.201	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.26 v
R.M.S. Current in the load	113 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.2 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.5 seconds

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494	24.70 mA
Ch2	0.493	24.65 mA
Ch3	0.497	24.85 mA
Ch4	0.501	25.05 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.6 mA	**16mA**	√
Ch2	0.654	32.7 mA	**16mA**	√
Ch3	0.656	32.8 mA	**16mA**	√
Ch4	0.658	32.9 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	**16mA**	√
Ch2	0.75	37.5 mA	**16mA**	√
Ch3	0.75	37.5 mA	**16mA**	√
Ch4	0.75	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	**16mA**	√
Ch2	0.75	37.5 mA	**16mA**	√
Ch3	0.75	37.5 mA	**16mA**	√
Ch4	0.75	37.5 mA	**16mA**	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.194	9.70 mA
Ch3	0.194	9.70 mA
Ch4	0.197	9.85 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.420	21 mA	**16mA**	√
Ch2	0.421	21 mA	**16mA**	√
Ch3	0.421	21 mA	**16mA**	√
Ch4	0.423	21 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.728	36.35 mA	**16mA**	√
Ch2	0.731	36.55 mA	**16mA**	√
Ch3	0.726	36.3 mA	**16mA**	√
Ch4	0.730	36.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.15 v	5.87 v	293 mA
Ch2	4.14 v	5.85 v	292 mA
Ch3	4.16 v	5.88 v	294 mA
Ch4	4.13 v	5.84 v	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.55 v	7.85 v	392 mA	**400mA**	
Ch2	5.55 v	7.85 v	392 mA	**400mA**	
Ch3	5.46 v	7.72 v	386 mA	**400mA**	
Ch4	5.53 v	7.82 v	391 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66 v	9.42 v	470 mA	**400mA**	√
Ch2	6.68 v	9.44 v	472 mA	**400mA**	√
Ch3	6.67 v	9.43 v	471 mA	**400mA**	√
Ch4	6.66 v	9.42 v	470 mA	**400mA**	√

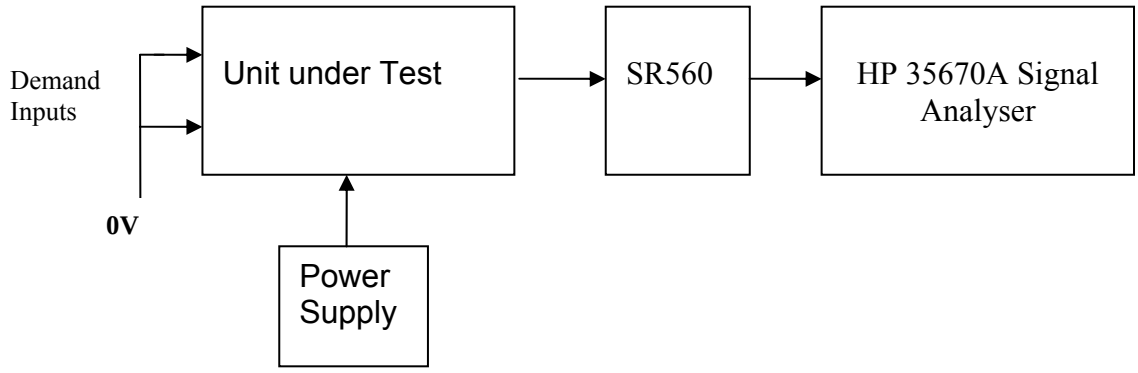
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.68 v	9.44 v	472 mA	**400mA**	√
Ch2	6.72 v	9.50 v	465 mA	**400mA**	√
Ch3	6.70 v	9.47 v	473 mA	**400mA**	√
Ch4	6.69 v	9.46 v	473 mA	**400mA**	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-101.5 dB	-161.5 dB
Ch2	-155.1	-99.49 dB	-159.5 dB
Ch3	-155.1	-99.86 dB	-159.8 dB
Ch4	-155.1	-100.6 dB	-161.6 dB

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.88	2.9μV√Hz	√
2		1.71	2.9μV√Hz	√
3		1.75	2.9μV√Hz	√
4		1.91	2.9μV√Hz	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM13P
Test Engineer ……RMC
Date ……21/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM13P
Driver board ID	PUM13P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM13P
Monitor board ID	MON178
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON178

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

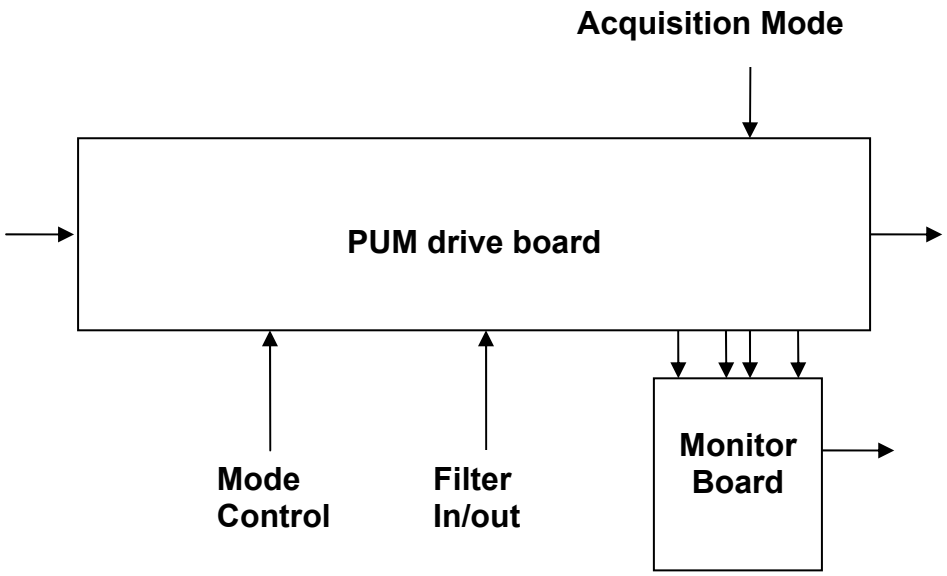
Unit……PUM14P
Test Engineer ……..RMC
Date ……..3/2/11

Drive Card ID……PUM14P
Monitor Card ID ……..MON193

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

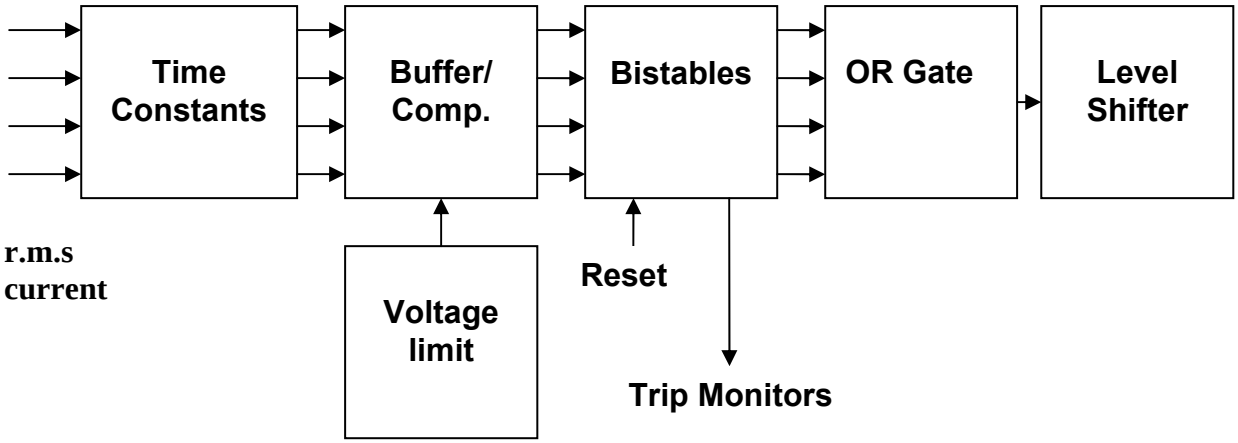
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

ok

Links:

Check that the links W4 is present on each channel.

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4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

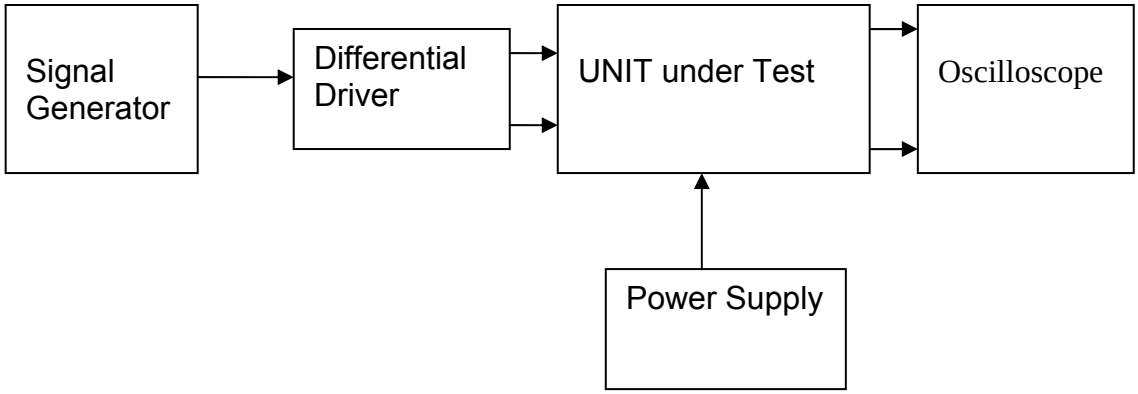
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+12.04	√	2 mV
+15v TP4	+14.93	√	2 mV
-15v TP6	-15.02	√	5 mV

All Outputs smooth DC, no oscillation?	OK

Some pick up.

Record Power Supply Currents

Supply	Current
+16.5v	0.553
-16.5v	0.482

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.195	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	1	0.195v +/- 0.01v	√
2	0.195	4	0.195v +/- 0.01v	√
3	0.196	7	0.195v +/- 0.01v	√
4	0.198	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

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9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.37 v
R.M.S. Current in the load	18.5 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.5 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2 seconds

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11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.495	24.7 mA
Ch2	0.499	24.9 mA
Ch3	0.501	25.0 mA
Ch4	0.496	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654	32.7 mA	**16mA**	√
Ch2	0.657	32.8 mA	**16mA**	√
Ch3	0.658	32.9 mA	**16mA**	√
Ch4	0.655	32.7 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

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11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195	9.75 mA
Ch2	0.196	9.8 mA
Ch3	0.196	9.8 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.421	21.0 mA	**16mA**	√
Ch2	0.423	21.1 mA	**16mA**	√
Ch3	0.422	21.1 mA	**16mA**	√
Ch4	0.422	21.1 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.4 mA	**16mA**	√
Ch2	0.730	36.5 mA	**16mA**	√
Ch3	0.729	36.4 mA	**16mA**	√
Ch4	0.730	36.4 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.749	37.4 mA	**16mA**	√
Ch3	0.748	37.4 mA	**16mA**	√
Ch4	0.749	37.4 mA	**16mA**	√

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11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.17 v	5.89	294 mA
Ch2	4.17 v	5.89	294 mA
Ch3	4.16 v	5.88	294 mA
Ch4	4.20 v	5.93	297 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.57 v	7.87	394 mA	**400mA**	
Ch2	5.57 v	7.87	394 mA	**400mA**	
Ch3	5.57 v	7.87	394 mA	**400mA**	
Ch4	5.59 v	7.90	395 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67 v	9.43	471 mA	**400mA**	√
Ch2	6.68 v	9.44	472 mA	**400mA**	√
Ch3	6.68 v	9.44	472 mA	**400mA**	√
Ch4	6.68 v	9.44	472 mA	**400mA**	√

5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70 v	9.47	474 mA	**400mA**	√
Ch2	6,71 v	9.48	474 mA	**400mA**	√
Ch3	6.71 v	9.48	474 mA	**400mA**	√
Ch4	6.70 v	9.47	474 mA	**400mA**	√

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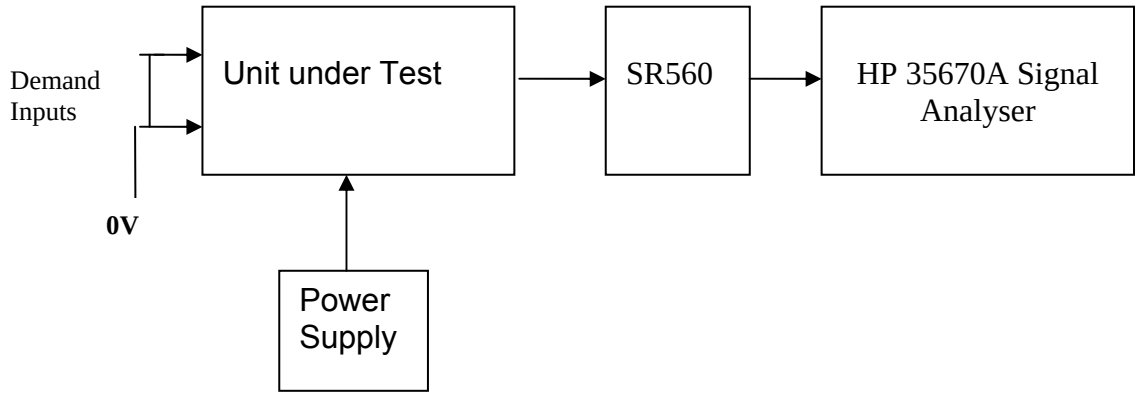
12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-99 dB	-159 dB
Ch2	-155.1	-96.8	-156.8
Ch3	-155.1	-98.7	-158.7
Ch4	-155.1	-96.8	-156.8

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

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Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.7	2.9μV√Hz	√
2		1.4	2.9μV√Hz	√
3		1.7	2.9μV√Hz	√
4		1.5	2.9μV√Hz	√

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

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14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM14P
Driver board ID	PUM14P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM14P
Monitor board ID	MON193
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON193

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

Unit……PUM15P
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Drive Card ID……PUM15P
Monitor Card ID ……..MON195

Contents

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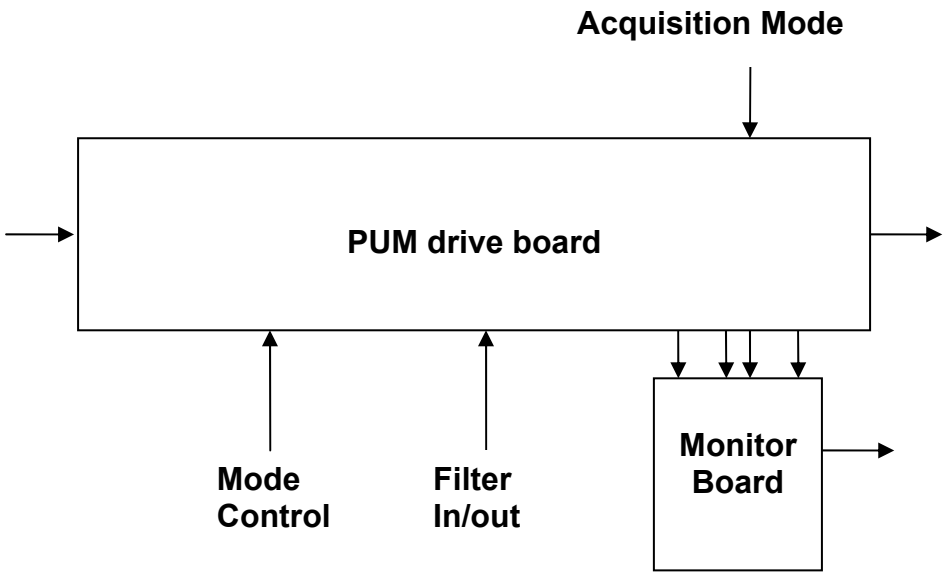
Block diagram



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The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

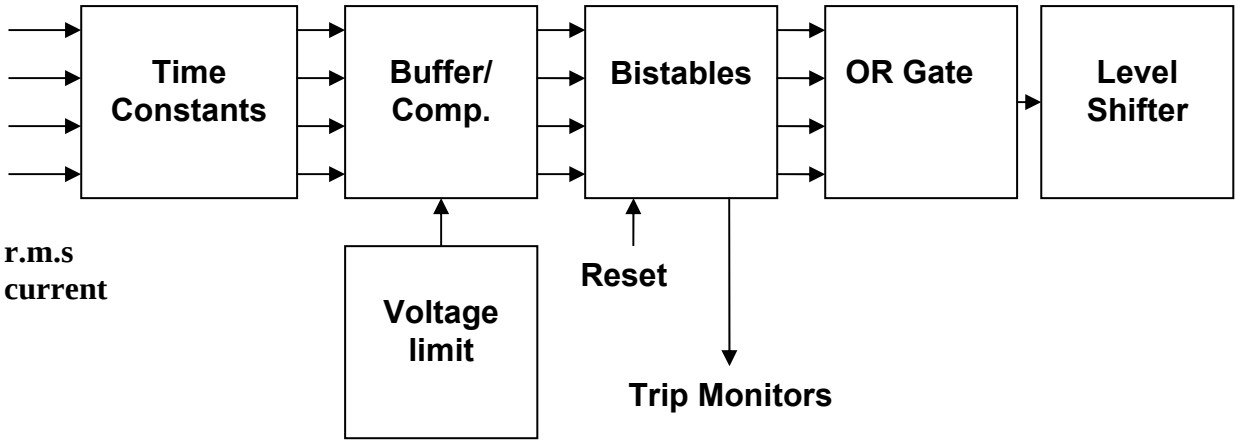
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

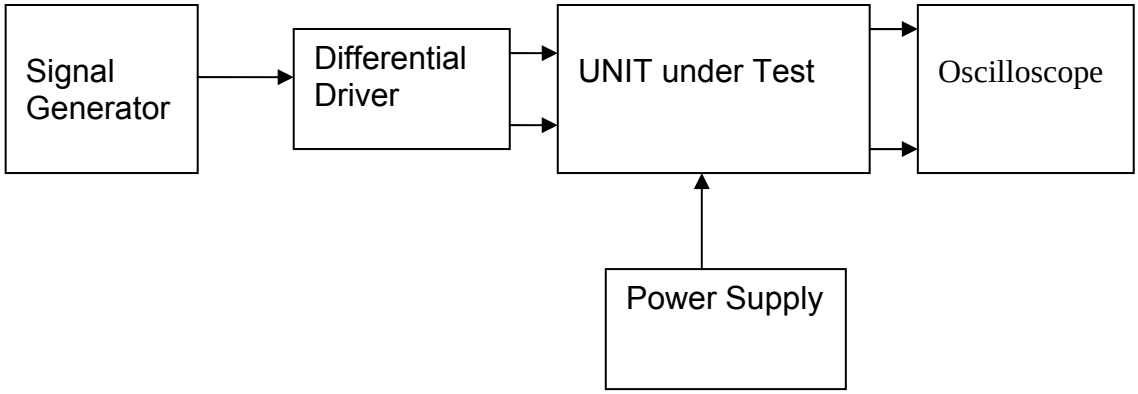
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+11.99	√	2 mV
+15v TP4	+14.92	√	2 mV
-15v TP6	-15.02	√	5 mV

All Outputs smooth DC, no oscillation?	√

Some external interference present

Record Power Supply Currents

Supply	Current
+16.5v	0.564
-16.5v	0.502

If the supplies are correct, proceed to the next test.

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.196	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.194	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.196	1	0.195v +/- 0.01v	√
2	0.198	4	0.195v +/- 0.01v	√
3	0.198	7	0.195v +/- 0.01v	√
4	0.195	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.33 v
R.M.S. Current in the load	116.5 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.5 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2.2 seconds

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.502	25.1 mA
Ch2	0.498	24.9 mA
Ch3	0.493	24.6 mA
Ch4	0.493	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.658	32.9 mA	**16mA**	√
Ch2	0.656	32.8 mA	**16mA**	√
Ch3	0.653	32.6 mA	**16mA**	√
Ch4	0.653	32.6 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.749	37.4 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.749	37.4 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.198	9.90 mA
Ch2	0.197	9.85 mA
Ch3	0.194	9.70 mA
Ch4	0.194	9.70 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.425	21.25 mA	**16mA**	√
Ch2	0.424	21.20 mA	**16mA**	√
Ch3	0.420	21.00 mA	**16mA**	√
Ch4	0.421	21.05 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.729	36.45 mA	**16mA**	√
Ch3	0.729	36.45 mA	**16mA**	√
Ch4	0.730	36.50 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749	37.45 mA	**16mA**	√
Ch2	0.748	37.40 mA	**16mA**	√
Ch3	0.749	37.45 mA	**16mA**	√
Ch4	0.750	37.50 mA	**16mA**	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12	5.82	291 mA
Ch2	4.15	5.86	293 mA
Ch3	4.14	5.85	292 mA
Ch4	4.11	5.81	290 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.53	7.82	391 mA	**400mA**	
Ch2	5.55	7.85	392 mA	**400mA**	
Ch3	5.55	7.85	392 mA	**400mA**	
Ch4	5.52	7.80	390 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.68	9.44	472 mA	**400mA**	√
Ch2	6.67	9.43	471 mA	**400mA**	√
Ch3	6.68	9.44	472 mA	**400mA**	√
Ch4	6.67	9.43	471 mA	**400mA**	√

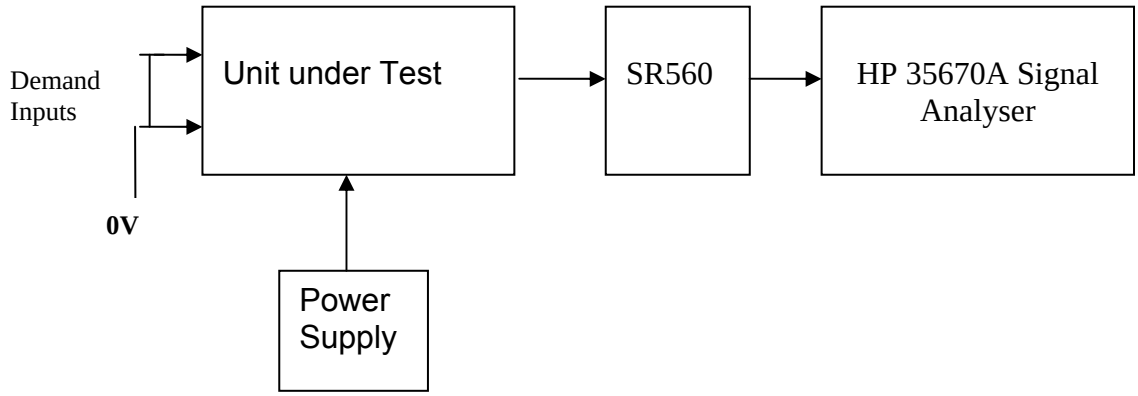
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**400mA**	√
Ch2	6.70	9.47	473 mA	**400mA**	√
Ch3	6.71	9.49	474 mA	**400mA**	√
Ch4	6.70	9.47	473 mA	**400mA**	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.5	-158.5
Ch2	-155.1	-100	-160
Ch3	-155.1	-100.7	-160.7
Ch4	-155.1	-99.7	-159.7

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.55	2.9μV√Hz	√
2		1.87	2.9μV√Hz	√
3		1.74	2.9μV√Hz	√
4		1.88	2.9μV√Hz	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM15P
Test Engineer ……RMC
Date ……3/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM15P
Driver board ID	PUM15P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM15P
Monitor board ID	MON195
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON195

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

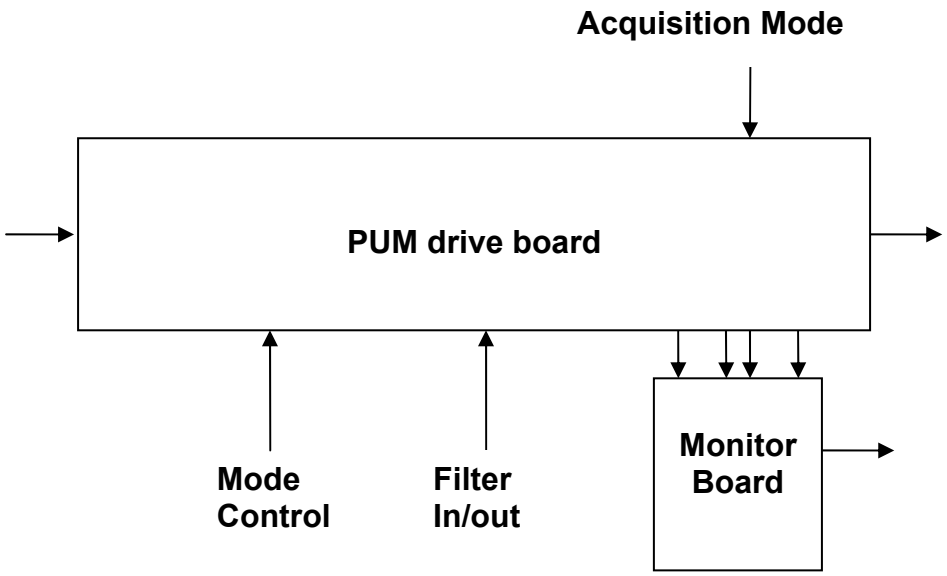
Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

Drive Card ID……PUM16P
Monitor Card ID ……..MON180

Contents

1. Description

Block diagram



Description
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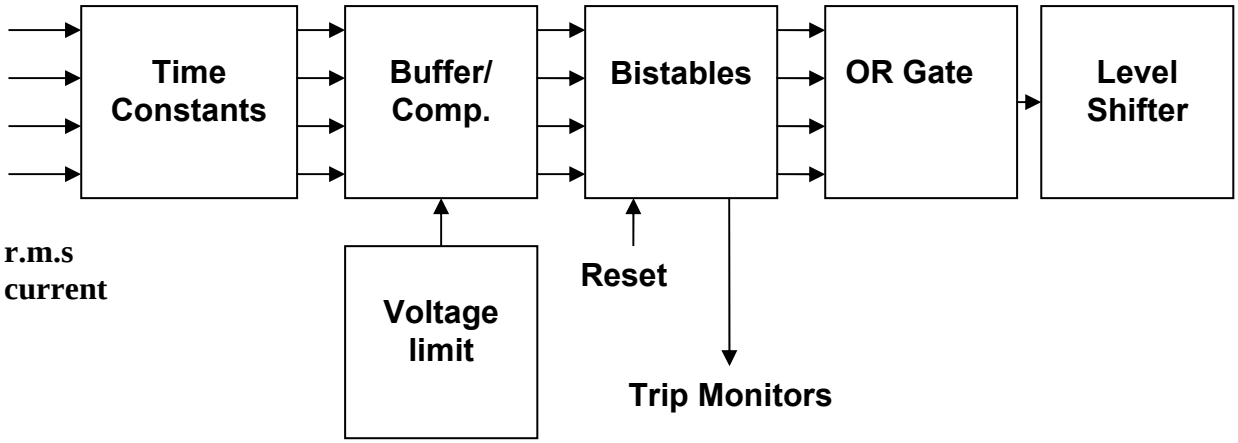
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

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Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
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Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

OK

Wire added to link pin 2 on J7 with the reset pulse.

Links:
Check that the links W4 is present on each channel.

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

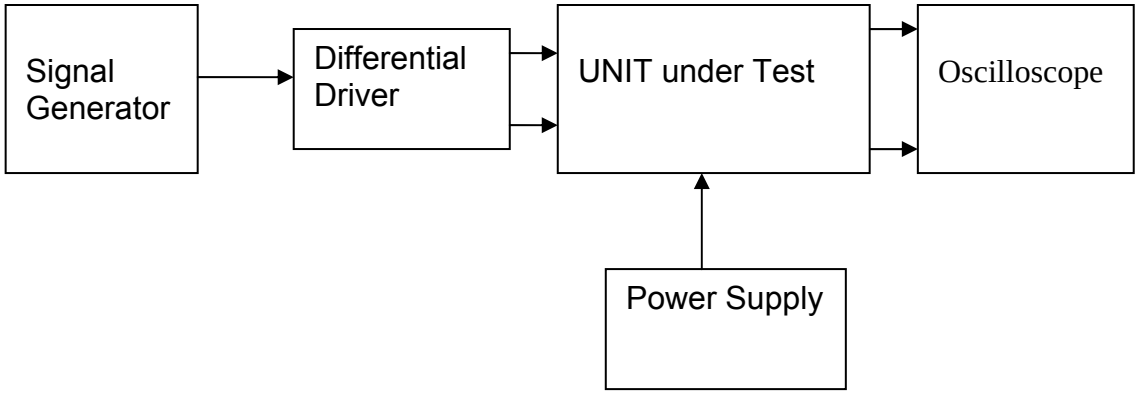
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.08 v	√	2 mV
+15v TP4	14.96 v	√	2 mV
-15v TP6	-15.01 v	√	5 mV

All Outputs smooth DC, no oscillation?	√

Around 2mV of interference present.

Record Power Supply Currents

Supply	Current
+16.5v	0.582A
-16.5v	0.536A

If the supplies are correct, proceed to the next test.

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.331	3	0.33v	√
2	0.332	6	0.33v	√
3	0.332	9	0.33v	√
4	0.332	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.195	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.198	1	0.195v +/- 0.01v	√
2	0.196	4	0.195v +/- 0.01v	√
3	0.202	7	0.195v +/- 0.01v	√
4	0.195	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v. Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.385 v
R.M.S. Current in the load	119.25 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.5 seconds

Disconnect the signal generator, and wait for the capacitors to discharge. Cycle the power supply. Adjust the signal generator to 10v. Connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.8 seconds

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.501	25 mA
Ch2	0.500	25 mA
Ch3	0.498	24.9 mA
Ch4	0.496	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.657	32.8 mA	**16mA**	√
Ch2	0.657	32.8 mA	**16mA**	√
Ch3	0.656	32.8 mA	**16mA**	√
Ch4	0.655	32.7 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.751	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.751	37.5 mA	**16mA**	√
Ch4	0.751	37.5 mA	**16mA**	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.196	9.8 mA
Ch2	0.195	9.75 mA
Ch3	0.192	9.6 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.422	21.1 mA	**16mA**	√
Ch2	0.421	21.0 mA	**16mA**	√
Ch3	0.423	21.1 mA	**16mA**	√
Ch4	0.422	21.1 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.4 mA	**16mA**	√
Ch2	0.729	36.4 mA	**16mA**	√
Ch3	0.730	36.5 mA	**16mA**	√
Ch4	0.730	36.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.749	37.4 mA	**16mA**	√
Ch3	0.749	37.4 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12	5.82	291.0 mA
Ch2	4.11	5.81	290.6 mA
Ch3	4.15	5.87	293.4 mA
Ch4	4.17	5.89	294.8 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.58	7.89	394 mA	**400mA**	
Ch2	5.53	7.82	391 mA	**400mA**	
Ch3	5.56	7.86	393 mA	**400mA**	
Ch4	5.57	7.87	393 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.41	470 mA	**400mA**	√
Ch2	6.68	9.44	472 mA	**400mA**	√
Ch3	6.68	9.44	472 mA	**400mA**	√
Ch4	6.68	9.44	472 mA	**400mA**	√

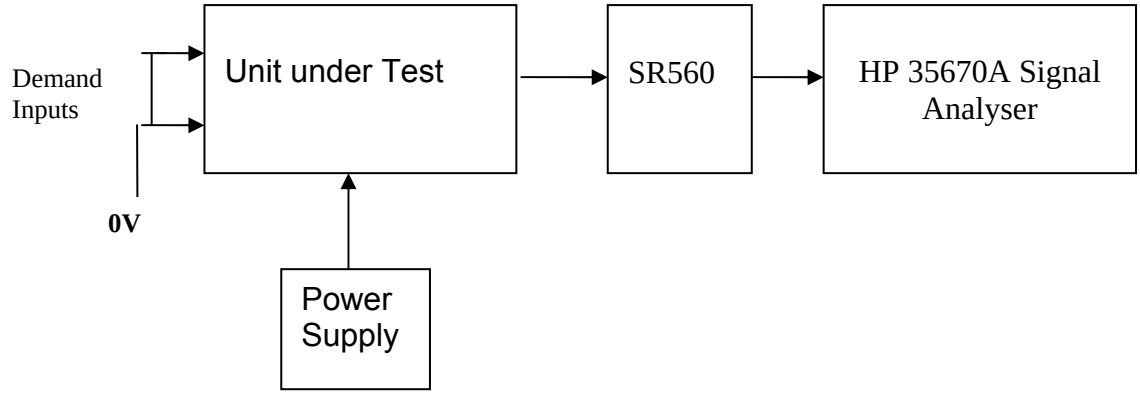
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	**400mA**	√
Ch2	6.71	9.49	474 mA	**400mA**	√
Ch3	6.71	9.49	474 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.9	-158.9
Ch2	-155.1	-99.9	-159.9
Ch3	-155.1	-100.18	-160.18
Ch4	-155.1	-100.28	-160.28

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV/√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.82	2.9μV√Hz	√
2		1.87	2.9μV√Hz	√
3		1.77	2.9μV√Hz	√
4		1.79	2.9μV√Hz	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM16P
Test Engineer ……RMC
Date ……..8/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM16P
Driver board ID	PUM16P
Driver board Drawing No/Issue No	D070483_07_p
Driver board Serial Number	PUM16P
Monitor board ID	MON180
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	Mon180

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

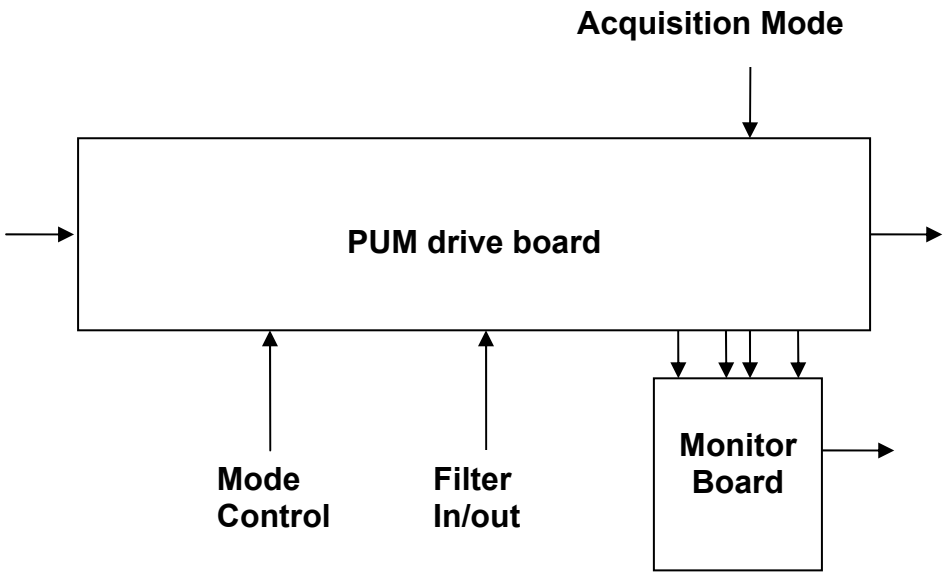
Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

Drive Card ID……PUM17P
Monitor Card ID ……..MON147

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

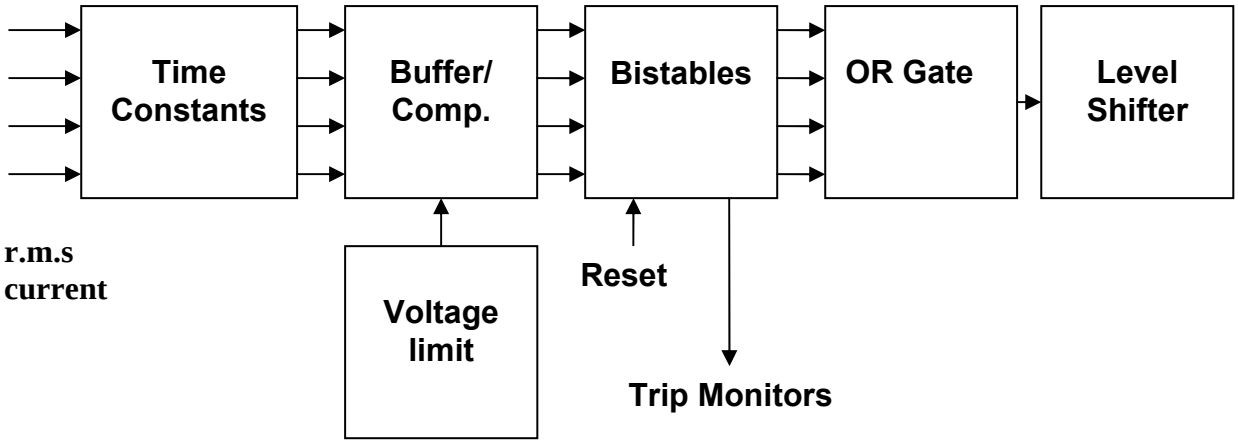
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Reset wire present between J7/2 and J7/18

Links:

Check that the links W4 is present on each channel.

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

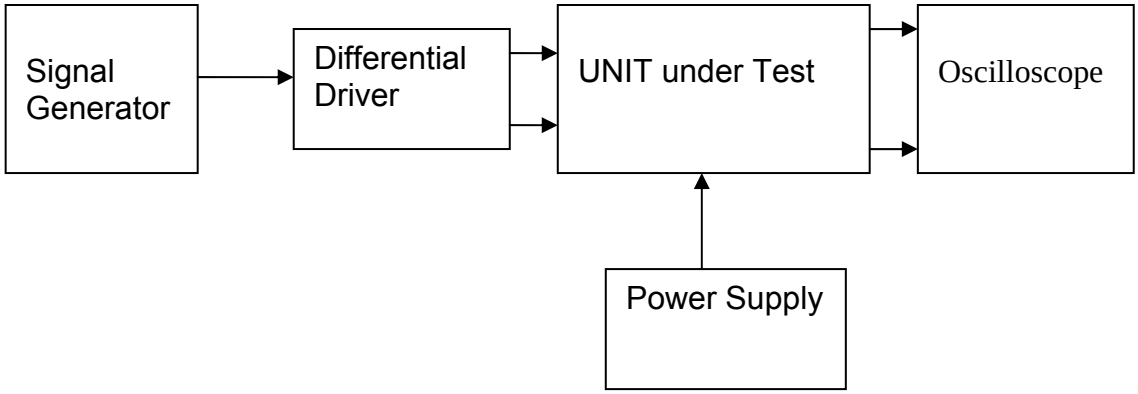
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.01	√	1 mV
+15v TP4	14.78	√	1mV
-15v TP6	-15.078	√	6 mV

All Outputs smooth DC, no oscillation?	√

Some pick up present

Record Power Supply Currents

Supply	Current
+16.5v	0.705
-16.5v	0.526

If the supplies are correct, proceed to the next test.

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194	2	0.195v +/- 0.01v	√
2	0.194	5	0.195v +/- 0.01v	√
3	0.194	8	0.195v +/- 0.01v	√
4	0.194	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.197	1	0.195v +/- 0.01v	√
2	0.199	4	0.195v +/- 0.01v	√
3	0.199	7	0.195v +/- 0.01v	√
4	0.200	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.318
R.M.S. Current in the load	115.9 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.9 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.6 seconds

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494	24.7 mA
Ch2	0.491	24.5 mA
Ch3	0.490	24.5 mA
Ch4	0.497	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.65 mA	**16mA**	√
Ch2	0.652	32.6 mA	**16mA**	√
Ch3	0.651	32.5 mA	**16mA**	√
Ch4	0.655	32.75 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.749	37.4 mA	**16mA**	√
Ch4	0.749	37.4 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.749	34.4 mA	**16mA**	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.191	9.55 mA
Ch3	0.192	9.6 mA
Ch4	0.196	9.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.421	21.0 mA	**16mA**	√
Ch2	0.417	20.8 mA	**16mA**	√
Ch3	0.419	20.9 mA	**16mA**	√
Ch4	0.423	21.15 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.730	36.5 mA	**16mA**	√
Ch2	0.729	36.45	**16mA**	√
Ch3	0.728	36.4 mA	**16mA**	√
Ch4	0.729	36.45	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749	37.45 mA	**16mA**	√
Ch2	0.749	37.45 mA	**16mA**	√
Ch3	0.748	37.4 mA	**16mA**	√
Ch4	0.748	37.4 mA	**16mA**	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.14	5.85	292 mA
Ch3	4.16	5.88	294 mA
Ch4	4.14	5.85	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.55	7.85	392 mA	**400mA**	
Ch2	5.55	7.85	392 mA	**400mA**	
Ch3	5.56	7.86	393 mA	**400mA**	
Ch4	5.54	7.83	391 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**400mA**	√
Ch2	6.67	9.43	471 mA	**400mA**	√
Ch3	6.67	9.43	471 mA	**400mA**	√
Ch4	6.66	9.42	471 mA	**400mA**	√

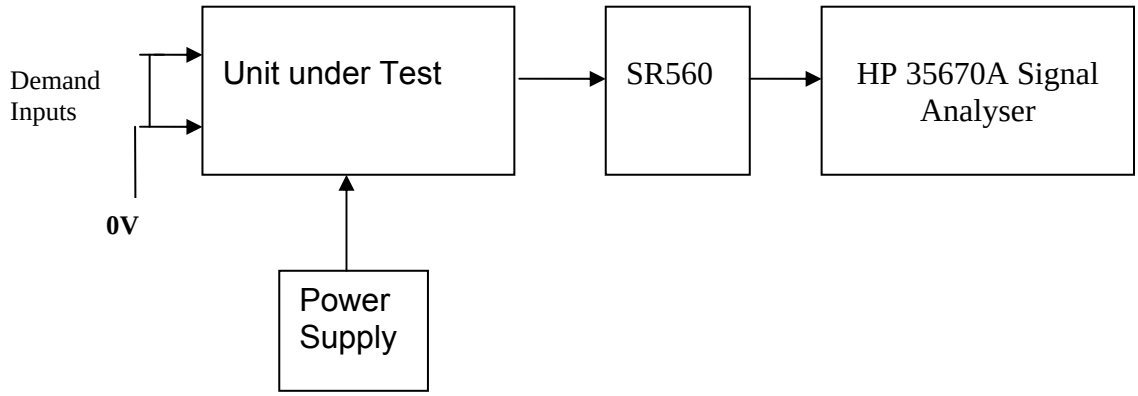
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**400mA**	√
Ch2	6.70	9.47	473 mA	**400mA**	√
Ch3	6.70	9.47	473 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-98.8	-158.8
Ch2	-155.1	-100.69	-160.6
Ch3	-155.1	-98.66	-158.6
Ch4	-155.1	-98.4	-158.4

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9μV√Hz	√
2		1.53	2.9μV√Hz	√
3		1.56	2.9μV√Hz	√
4		1.97	2.9μV√Hz	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM17P
Test Engineer ……RMC
Date ……9/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM17P
Driver board ID	D070483_07_K
Driver board Drawing No/Issue No	PUM17P
Driver board Serial Number	PUM17P
Monitor board ID	MON147
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON147

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

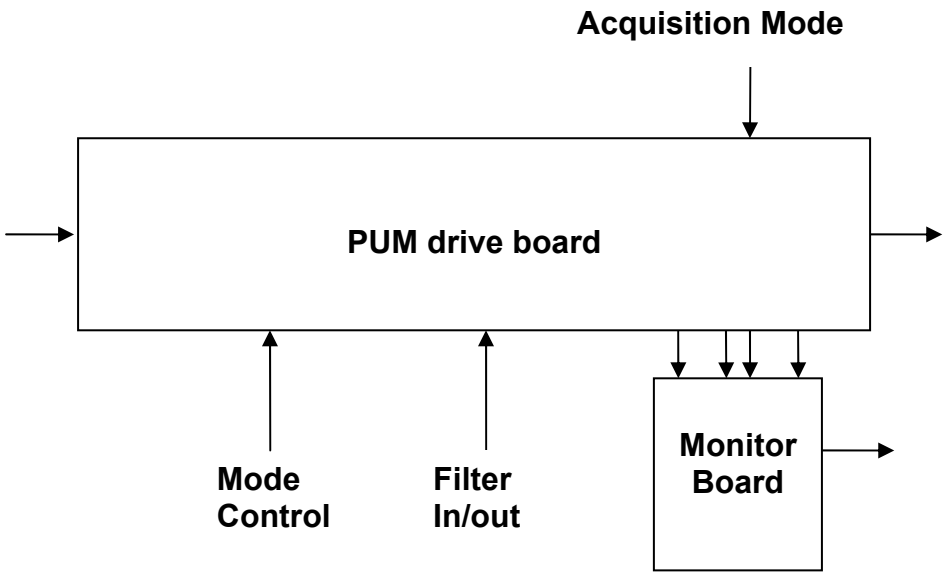
Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

Drive Card ID……PUM18P
Monitor Card ID ……..MON85

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

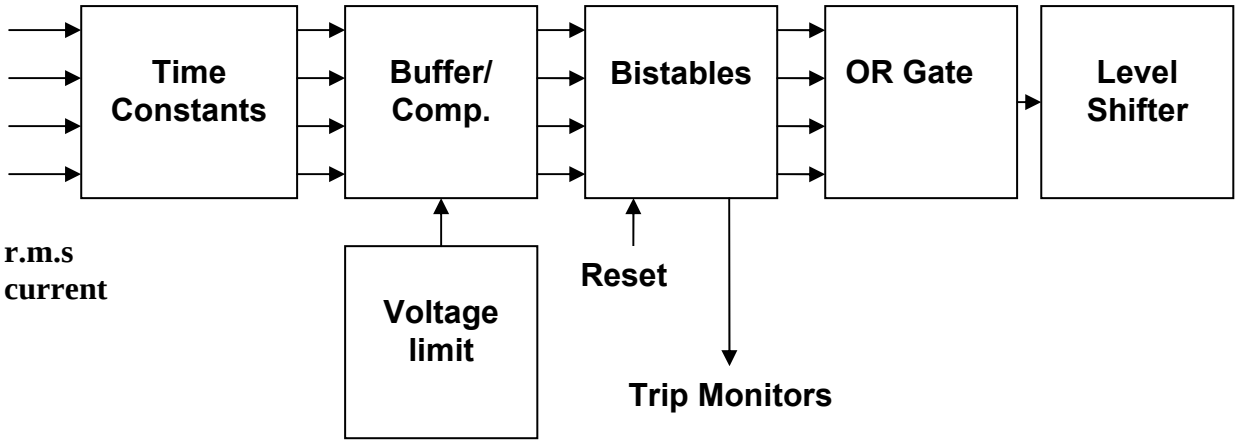
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

Ok

Reset link added between J7/2 and J7/18

Links:
Check that the links W4 is present on each channel.

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

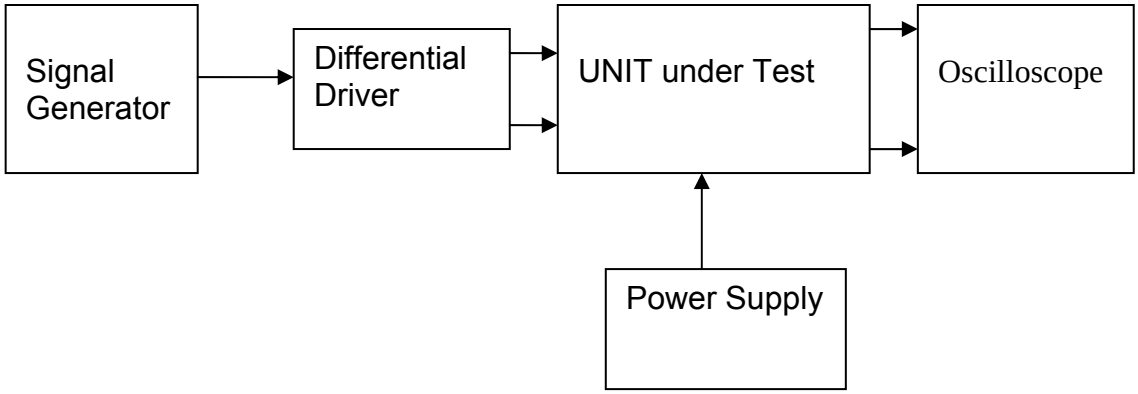
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	+11.98 v	√	1.2 mV
+15v TP4	+14.96 v	√	1.2 mV
-15v TP6	-14.96 v	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pick up present on incoming power lines

Record Power Supply Currents

Supply	Current
+16.5v	0.736 A
-16.5v	0.553 A

If the supplies are correct, proceed to the next test.

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.194	2	0.195v +/- 0.01v	√
2	0.195	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.195	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.198	1	0.195v +/- 0.01v	√
2	0.197	4	0.195v +/- 0.01v	√
3	0.198	7	0.195v +/- 0.01v	√
4	0.198	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.35 v
R.M.S. Current in the load	117.5 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.75 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.75 seconds

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.496	24.8 mA
Ch2	0.499	24.95 mA
Ch3	0.494	24.7 mA
Ch4	0.491	24.5 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654	32.70 mA	**16mA**	√
Ch2	0.656	32.80 mA	**16mA**	√
Ch3	0.653	32.65 mA	**16mA**	√
Ch4	0.652	31.25 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**16mA**	√
Ch2	0.750	37.5 mA	**16mA**	√
Ch3	0.750	37.5 mA	**16mA**	√
Ch4	0.750	37.5 mA	**16mA**	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.196	9.8 mA
Ch3	0.194	9.7 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.419	20.95 mA	**16mA**	√
Ch2	0.423	21.15 mA	**16mA**	√
Ch3	0.421	21.05 mA	**16mA**	√
Ch4	0.419	20.95 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.729	36.45 mA	**16mA**	√
Ch3	0.729	36.45 mA	**16mA**	√
Ch4	0.729	36.45 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**16mA**	√
Ch2	0.749	36.45 mA	**16mA**	√
Ch3	0.748	37.4 mA	**16mA**	√
Ch4	0.749	36.45 mA	**16mA**	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.16	5.88	294 mA
Ch3	4.14	5.85	293 mA
Ch4	4.15	5.86	293 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.56	7.86	393 mA	**400mA**	
Ch2	5.56	7.86	393 mA	**400mA**	
Ch3	5.55	7.85	392 mA	**400mA**	
Ch4	5.55	7.85	392 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.42	471 mA	**400mA**	√
Ch2	6.66	9.42	471 mA	**400mA**	√
Ch3	6.66	9.42	471 mA	**400mA**	√
Ch4	6.65	9.40	470 mA	**400mA**	√

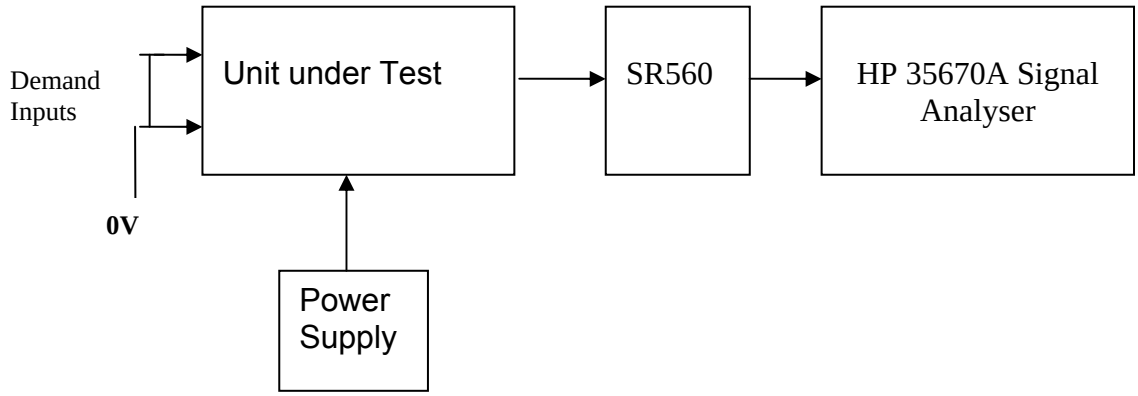
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	**400mA**	√
Ch2	6.69	9.46	473 mA	**400mA**	√
Ch3	6.69	9.46	473 mA	**400mA**	√
Ch4	6.68	9.45	472 mA	**400mA**	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-101.2	-161.2
Ch2	-155.1	-101.56	-161.5
Ch3	-155.1	-100.54	-161.5
Ch4	-155.1	-100.29	-161.2

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.73	2.9μV√Hz	√
2		1.71	2.9μV√Hz	√
3		1.70	2.9μV√Hz	√
4		1.79	2.9μV√Hz	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM18P
Test Engineer ……RMC
Date ……14/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM18P
Driver board ID	PUM18P
Driver board Drawing No/Issue No	D070483_
Driver board Serial Number	PUM18P
Monitor board ID	MON85
Monitor board Drawing No/Issue No	D070480_5_K
Monitor board Serial Number	MON85

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

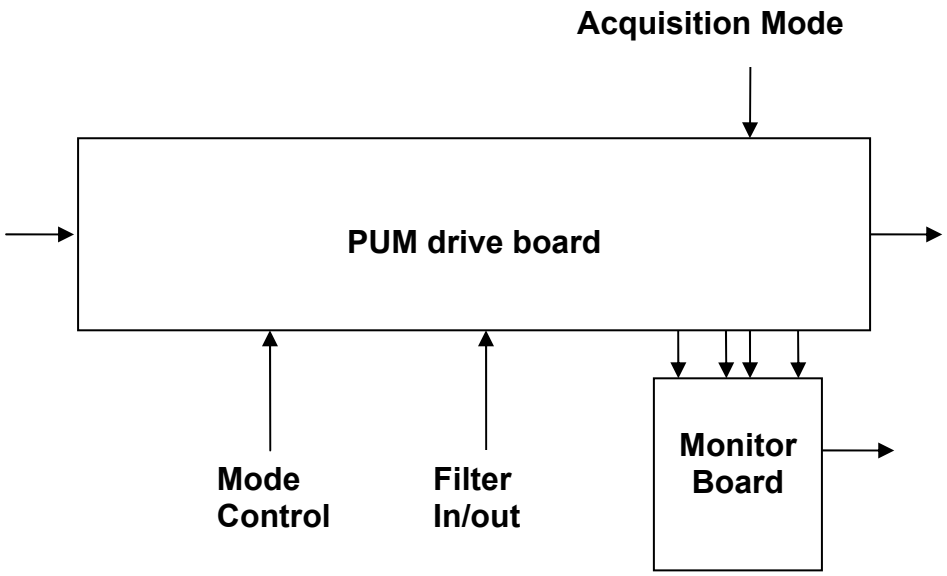
Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

Drive Card ID……PUM19P
Monitor Card ID ……..MON162

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

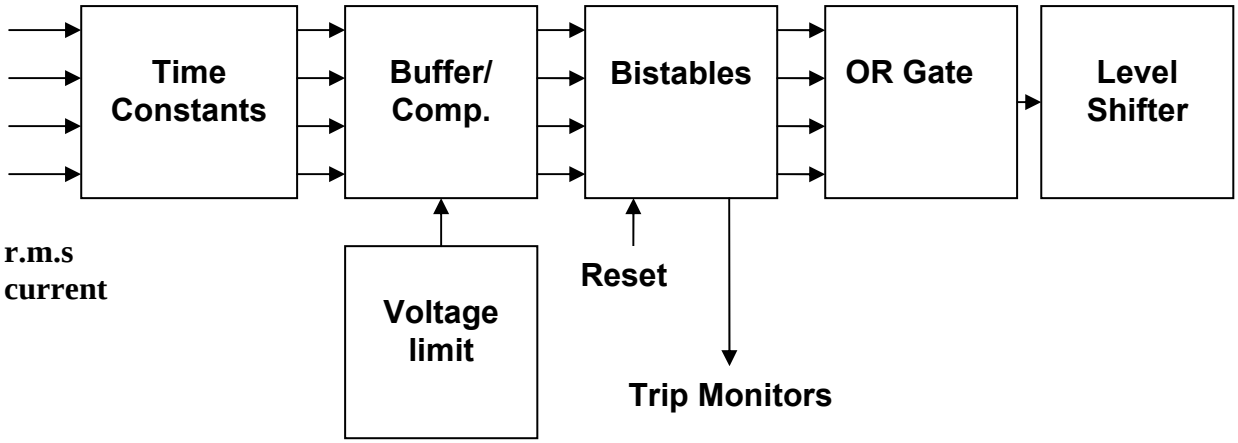
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link added between J7/2 and J7/18

IC7 on channel 2 was changed because it was faulty

Links:

Check that the links W4 is present on each channel.

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

4. Continuity Checks

Continuity to the PD in from SAT (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

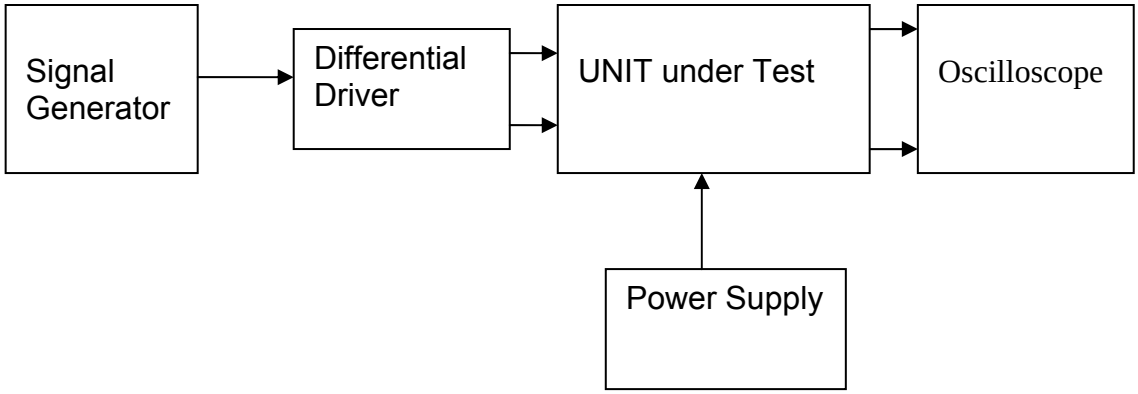
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.00	√	2 mV
+15v TP4	14.82	√	2 mV
-15v TP6	-15.10	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pick up

Record Power Supply Currents

Supply	Current
+16.5v	0.560
-16.5v	0.481

If the supplies are correct, proceed to the next test.

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33	3	0.33v	√
2	0.33	6	0.33v	√
3	0.33	9	0.33v	√
4	0.33	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195	2	0.195v +/- 0.01v	√
2	0.194	5	0.195v +/- 0.01v	√
3	0.195	8	0.195v +/- 0.01v	√
4	0.194	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.200	1	0.195v +/- 0.01v	√
2	0.200	4	0.195v +/- 0.01v	√
3	0.200	7	0.195v +/- 0.01v	√
4	0.199	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

See Monitor re-test report.

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.32
R.M.S. Current in the load	116 mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	3.6 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	1.3 seconds

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494	24.70 mA
Ch2	0.494	24.70 mA
Ch3	0.495	24.75 mA
Ch4	0.493	44.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.65 mA	**16mA**	√
Ch2	0.653	32.65 mA	**16mA**	√
Ch3	0.654	32.70 mA	**16mA**	√
Ch4	0.653	32.65 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.50 mA	**16mA**	√
Ch2	0.751	37.55 mA	**16mA**	√
Ch3	0.750	37.50 mA	**16mA**	√
Ch4	0.750	37.50 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.50 mA	**16mA**	√
Ch2	0.751	37.55 mA	**16mA**	√
Ch3	0.750	37.50 mA	**16mA**	√
Ch4	0.750	37.50 mA	**16mA**	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.194	9.70 mA
Ch3	0.196	9.80 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.419	20.95 mA	**16mA**	√
Ch2	0.420	21.0 mA	**16mA**	√
Ch3	0.424	21.2 mA	**16mA**	√
Ch4	0.422	21.1 mA	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**16mA**	√
Ch2	0.730	36.50 mA	**16mA**	√
Ch3	0.730	36.50 mA	**16mA**	√
Ch4	0.730	36.50 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.40 mA	**16mA**	√
Ch2	0.750	37.50 mA	**16mA**	√
Ch3	0.749	37.45 mA	**16mA**	√
Ch4	0.749	37.45 mA	**16mA**	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.14	5.85	292 mA
Ch3	4.15	5.86	293 mA
Ch4	4.13	5.84	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.56	7.86	393 mA	**400mA**	√
Ch2	5.55	7.85	392 mA	**400mA**	√
Ch3	5.55	7.85	392 mA	**400mA**	√
Ch4	5.53	7.82	391 mA	**400mA**	√

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**400mA**	√
Ch2	6.68	9.44	472 mA	**400mA**	√
Ch3	6.66	9.42	470 mA	**400mA**	√
Ch4	6.66	9.42	470 mA	**400mA**	√

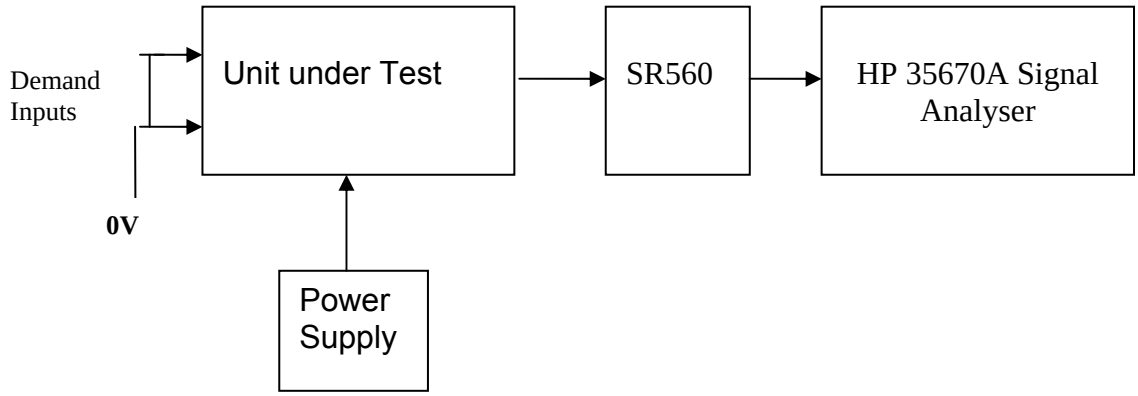
5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**400mA**	√
Ch2	6.71	9.46	473 mA	**400mA**	√
Ch3	6.69	9.46	473 mA	**400mA**	√
Ch4	6.69	9.46	473 mA	**400mA**	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-99.73	-159 dB
Ch2	-155.1	-100.61	-160 dB
Ch3	-155.1	-100.27	-160 dB
Ch4	-155.1	-101.01	-161 dB

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.14	2.9μV√Hz	√
2		1.81	2.9μV√Hz	√
3		1.82	2.9μV√Hz	√
4		1.87	2.9μV√Hz	√

Unit……PUM19P
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Unit……PUM19P
Test Engineer …….RMC
Date ……16/2/11

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	PUM19P
Driver board ID	PUM19P
Driver board Drawing No/Issue No	D070483_07_K
Driver board Serial Number	PUM19P
Monitor board ID	MON62
Monitor board Drawing No/Issue No	D070480_05_K
Monitor board Serial Number	MON62

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900292 Advanced LIGO UK December 2009

PUM Driver Unit Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

PUM DRIVER UNIT BOARD TEST REPORT

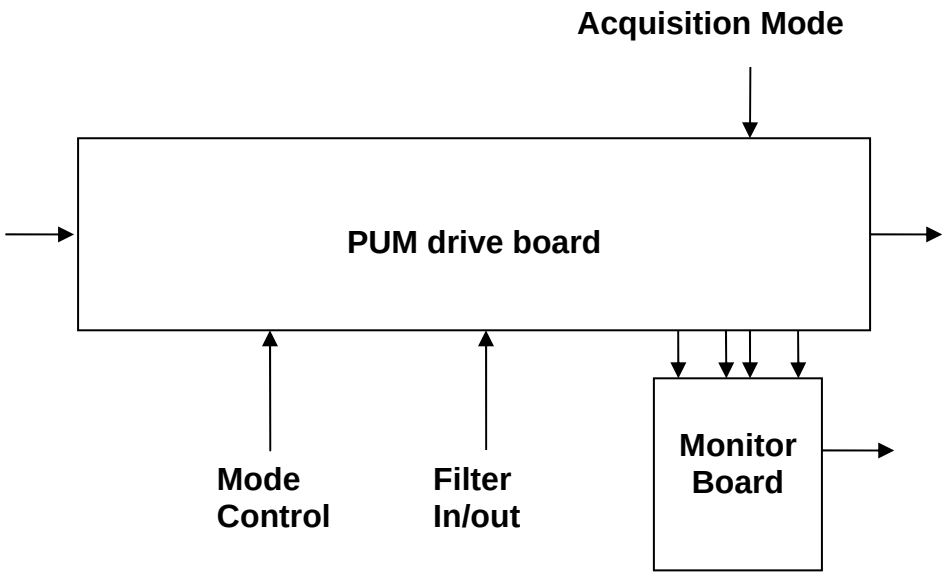
Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

Drive Card ID……PUM1P
Monitor Card ID …… MON60P

Contents

1. Description

Block diagram



Description
The PUM unit consists of four identical channels and the power regulators which provide regulated power to the four channels.

Each channel consists of a coil drive channel, and monitor circuitry. There is also a time delayed trip circuit, which protects the OSEMs from being over driven for long periods.

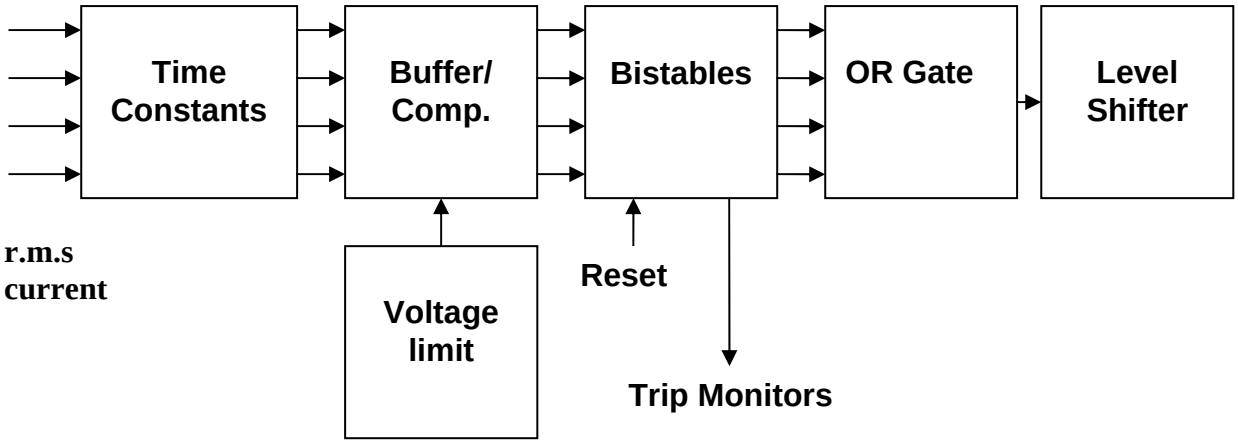
The driver ha 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a Test Mode which routes the inputs to the Test Connector.

The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

All bistables are reset at power on, and may be reset by a single command line.

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
DVM	Fluke	287	
Voltage calibrator	Time	1044	
PSU	Farnell	30-2	
PSU	Farnell	30-2	
Scope	Tektronix	2225	
DSA	Agilent	35670	

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the links W4 is present on each channel.

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

4. Continuity Checks

Continuity to the V, I and R.M.S Monitor (J1)

PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5		0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

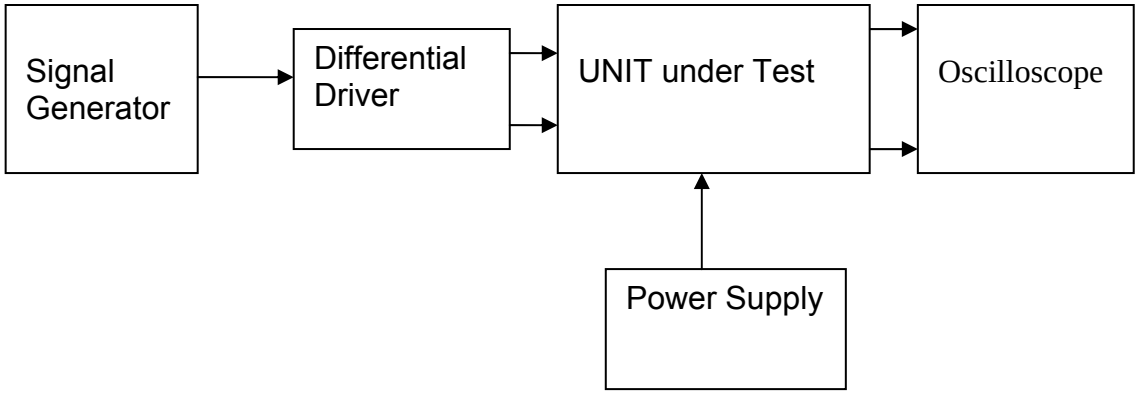
LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5		0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Pd from Sat

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
Drive Input J3 pins 1, 2, 3, 4 = positive input
Drive Input J3 pins 6, 7, 8, 9 = negative input
Drive Input J3 pin 5 = ground

Power
DC IN J1 pin 9, 10 = +16.5v
DC IN J1 pin 11,12 = -16.5
DC IN J1 pins 22, 23, 24, 25 = 0v

Outputs
Coil Out to Sat (J4)

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.008v	√	1mV
+15v TP4	14.902v	√	1.2mV
-15v TP6	-15.141	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.5A
-16.5v	0.48A

If the supplies are correct, proceed to the next test.

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS √

Channel	Indicator		OK?
	ON	OFF	
Ch1			
Ch2			
Ch3			
Ch4			

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply an input from the signal generator at 1 KHz, and adjust the amplitude until the output is 1vr r.m.s as measured between TP10 and TP12.
Measure the Voltage Monitor outputs with respect to 0v for each channel.

8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	OK?
1	0.33v	3	0.33v	√
2	0.33v	6	0.33v	√
3	0.33v	9	0.33v	√
4	0.33v	12	0.33v	√

8.2 Current Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.195v	2	0.195v +/- 0.01v	√
2	0.195v	5	0.195v +/- 0.01v	√
3	0.195v	8	0.195v +/- 0.01v	√
4	0.195v	11	0.195v +/- 0.01v	√

8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	OK?
1	0.200v	1	0.195v +/- 0.01v	√
2	0.201v	4	0.195v +/- 0.01v	√
3	0.197v	7	0.195v +/- 0.01v	√
4	0.199v	10	0.195v +/- 0.01v	√

8.4 Noise Monitors

Using the Dynamic Signal Analyser, measure the noise monitor outputs in dBV/√Hz. Correct for the pre-amplifier gain (if used.)

Ch.	Pin	Output	Limit	OK?
1	1	1.11	2.9µV	√
2	2	1.34	2.9µV	√
3	3	1.39	2.9µV	√
4	4	1.43	2.9µV	√

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……26/5/10

9. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.
The trip circuit must be disconnected by unplugging the ribbon cable P3 for these tests.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……PUM1P……Serial No ……
Test Engineer ……RMC
Date ……19/5/10

10. Trip Circuit Tests

Switch the filters out.
Both the 16 way ribbon cables between the Drive Board and the Voltage Monitor board need to be connected as usual, for this test.

Observe TP25, and the channel outputs. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Connect the signal generator to the unit with a frequency of 200Hz. Put the unit in Acquisition Mode. Adjust the amplitude of the sine wave until the output current is 100mA r.m.s, which gives 2v r.m.s across the 20 ohm load resistor, The signal generator will be set at around 3.6v . Run the unit for a few minutes. It should keep running without tripping, and TP25 should remain low.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

R.M.S. Volts across the load	2.35v
R.M.S. Current in the load	117mA

Check that all output coil drive voltages disappear after the circuit has tripped.

Ch1 o/p disappeared?	√
Ch2 o/p disappeared?	√
Ch3 o/p disappeared?	√
Ch4 o/p disappeared?	√

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Disconnect the signal generator. Adjust the signal generator to 5.4v, giving an output current of around 150mA. Monitor TP25 and TP13. Connect the signal generator and measure the time taken for the circuit to trip..

Time taken to trip?	4.4 seconds

Disconnect the signal generator, and wait for the capacitors to discharge.
Cycle the power supply. Adjust the signal generator to 10v. connect the signal generator, and measure the time taken for the trip to operate.

Time taken to trip?	2.2 seconds

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11 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

11.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.2309	11.5 mA
Ch2	0.2307	11.53 mA
Ch3	0.2331	11.65 mA
Ch4	0.2317	11.58 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.397	19.85	**16mA**	√
Ch2	0.397	19.85	**16mA**	√
Ch3	0.400	20.00	**16mA**	√
Ch4	0.398	19.90	**16mA**	√

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.715	35.75 mA	**16mA**	√
Ch2	0.715	35.75 mA	**16mA**	√
Ch3	0.716	35.80 mA	**16mA**	√
Ch4	0.713	35.65 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.746	37.3 mA	**16mA**	√
Ch2	0.746	37.3 mA	**16mA**	√
Ch3	0.746	37.3 mA	**16mA**	√
Ch4	0.744	37.2 mA	**16mA**	√

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11.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.088	4.4		
Ch2	0.088	4.4		
Ch3	0.090	4.5		
Ch4	0.089	4.45		

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.253	12.65 mA	**16mA**	
Ch2	0.253	12.65 mA	**16mA**	
Ch3	0.256	12.85 mA	**16mA**	
Ch4	0.257	12.8 mA	**16mA**	

1KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.694	34.7 mA	**16mA**	√
Ch2	0.694	34.7 mA	**16mA**	√
Ch3	0.696	34.8 mA	**16mA**	√
Ch4	0.693	34.65 mA	**16mA**	√

5KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.746	37.3 mA	**16mA**	√
Ch2	0.746	37.3 mA	**16mA**	√
Ch3	0.746	37.3 mA	**16mA**	√
Ch4	0.744	37.2 mA	**16mA**	√

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Date ……20/5/10

11.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the unit running with a 10v input for too long, especially if the heat sink is not fitted. R.M.S feedback ribbon cable P3 must be disconnected for this test, to prevent tripping, and replaced by the grounded test ribbon cable.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	4.108	5.809	290.4 mA		
Ch2	4.119	5.825	291.2 mA		
Ch3	4.091	5.785	289.2 mA		
Ch4	4.113	5.816	290.8 mA		

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.58	7.791	394.5 mA	**400mA**	
Ch2	5.59	7.905	395.2 mA	**400mA**	
Ch3	5.57	7.877	393.8 mA	**400mA**	
Ch4	5.57	7.877	393.8 mA	**400mA**	

1K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.63	9.376	468.8 mA	**400mA**	√
Ch2	6.64	9.390	469.5 mA	**400mA**	√
Ch3	6.64	9.390	469.5 mA	**400mA**	√
Ch4	6.61	9.348	467.3 mA	**400mA**	√

5K Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.432	471.6 mA	**400mA**	√
Ch2	6.66	9.418	470.9 mA	**400mA**	√
Ch3	6.68	9.447	472.3 mA	**400mA**	√
Ch4	6.66	9.418	470.9 mA	**400mA**	√

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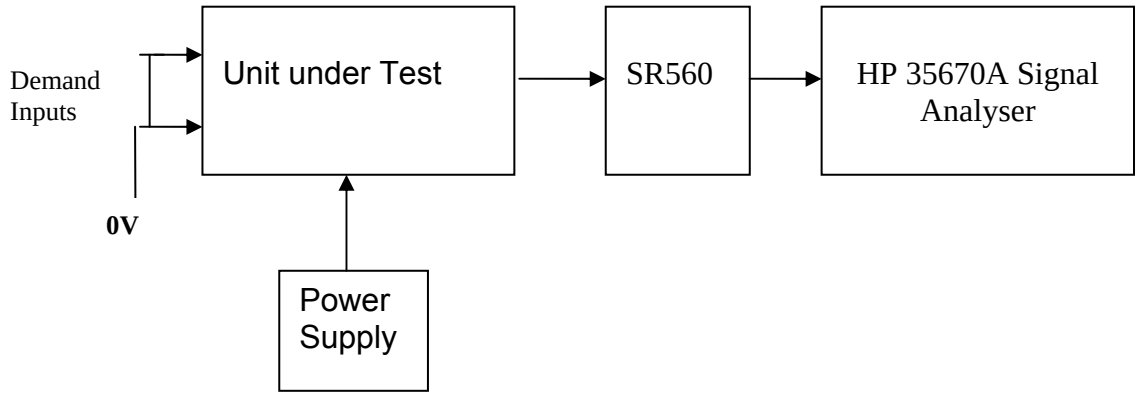
12 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter link W4 on each channel.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode and out of the Acquisition mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-100.6	-160.6
Ch2	-155.1	-100.3	-160.3
Ch3	-155.1	-100.5	-160.5
Ch4	-155.1	- 99.1	-159.1

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-12.00	√	-12.00	√	-12.00	√	-12.00	√
-7v	-8.40	√	-8.40	√	-8.40	√	-8.40	√
-5v	-5.97	√	-5.98	√	-5.99	√	-5.99	√
-1v	-1.19	√	-1.2	√	-1.2	√	-1.2	√
0v	0.00	√	-0.01	√	-0.01	√	0.01	√
1v	1.19	√	1.19	√	1.19	√	1.20	√
5v	6.00	√	6.00	√	6.00	√	6.00	√
7v	8.40	√	8.40	√	8.40	√	8.40	√
10v	12.00	√	12.00	√	12.00	√	12.00	√

Unit……Serial No ……
Test Engineer ……
Date ……

14. Final Assembly Tests

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that all links W4 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. √ Record below:

UoB box ID	PUM1P
Driver board ID	PUM1P
Driver board Drawing No/Issue No	D070483_5_K
Driver board Serial Number	PUM1P
Monitor board ID	MON60P
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON60P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √