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# PUM Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

**Institute for Gravitational Research**
**University of Glasgow**
Phone +44 (0) 141 330 5884
Fax +44 (0) 141 330 6833
E-mail k.strain@physics.gla.ac.uk
**Engineering Department**
**CCLRC Rutherford Appleton Laboratory**
Phone +44 (0) 1235 445 297
Fax +44 (0) 1235 445 843
E-mail J.Greenhalgh@rl.ac.uk

**School of Physics and Astronomy**
**University of Birmingham**
Phone +44 (0) 121 414 6447
Fax +44 (0) 121 414 3722
E-mail av@star.sr.bham.ac.uk
**Department of Physics**
**University of Strathclyde**
Phone +44 (0) 1411 548 3360
Fax +44 (0) 141 552 2891
E-mail N.Lockerbie@phys.strath.ac.uk

http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

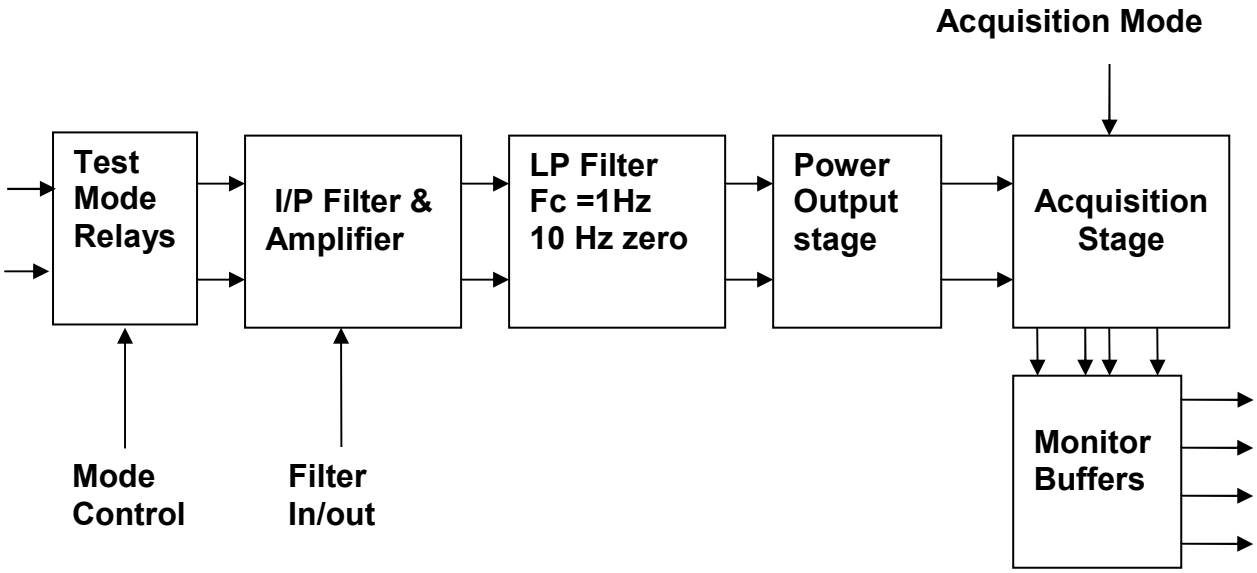
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……Serial No ……
Test Engineer ……
Date ……

## Contents

# 1. Description

**Block diagram**




**Description**
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

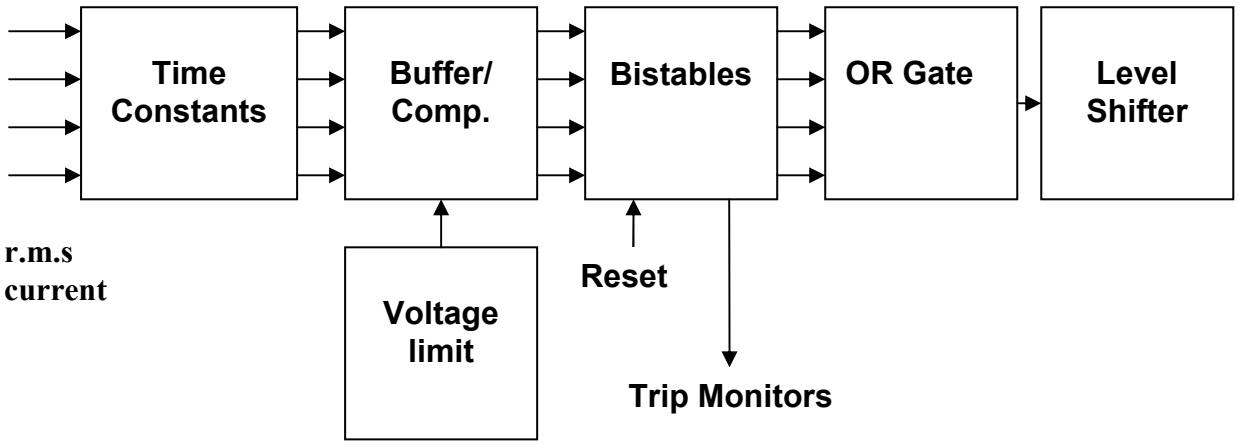
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

## Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.




### The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

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## 3. Inspection

### Workmanship

Inspect the general workmanship standard and comment:

## Links:

Check that the link W4 is present on each channel.

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## 4. Continuity Checks

**J2**

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|---|---|---|---|---|
| 1 | PD1P | Photodiode A+ | 1 | |
| 2 | PD2P | Photodiode B+ | 2 | |
| 3 | PD3P | Photodiode C+ | 3 | |
| 4 | PD4P | Photodiode D+ | 4 | |
| 5 | 0V | | | |
| 6 | PD1N | Photodiode A- | 14 | |
| 7 | PD2N | Photodiode B- | 15 | |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

**J5**

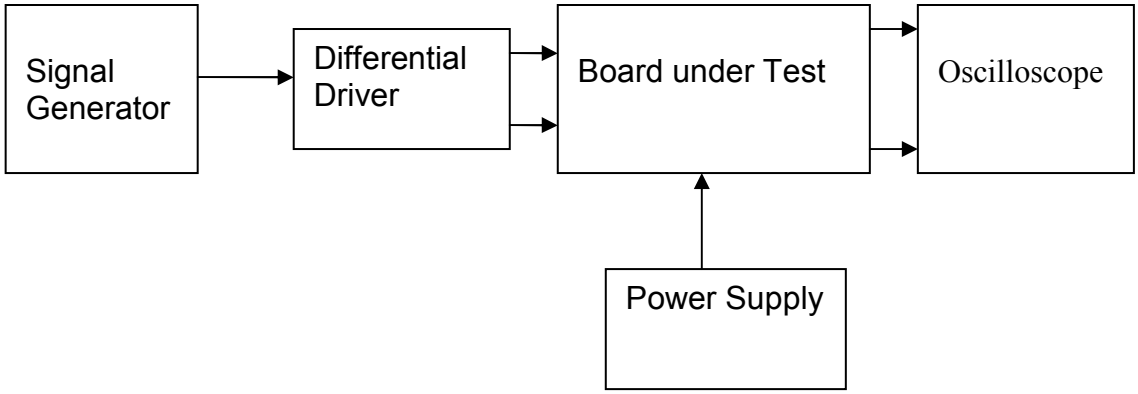
| PIN | SIGNAL | | To J1 PIN | OK? |
|---|---|---|---|---|
| 1 | Imon1P | | 5 | |
| 2 | Imon2P | | 6 | |
| 3 | Imon3P | | 7 | |
| 4 | Imon4P | | 8 | |
| 5 | 0V | | | |
| 6 | Imon1N | | 18 | |
| 7 | Imon2N | | 19 | |
| 8 | Imon3N | | 20 | |
| 9 | Imon4N | | 21 | |

**Power Supply to Satellite box**

**J1**

| PIN | SIGNAL | DESCRIPTION | OK? |
|---|---|---|---|
| 9 | V+ (TP1) | +17v Supply | |
| 10 | V+ (TP1) | +17v Supply | |
| 11 | V- (TP2) | -17v Supply | |
| 12 | V- (TP2) | -17v Supply | |
| 13 | 0V (TP3) | | |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

## 5. TEST SET UP




Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

| | |
|---|---|
| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

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## 6. Power

**Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.**

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

| Regulator | Output voltage | Nominal +/- 0.5v? | Output noise |
|---|---|---|---|
| +12v TP5 | | | |
| +15v TP4 | | | |
| -15v TP6 | | | |

| All Outputs smooth DC, no oscillation? | |
|---|---|

**Record Power Supply Currents**

| Supply | Current |
|---|---|
| +16.5v | |
| -16.5v | |

If the supplies are correct, proceed to the next test.

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## 7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

### Filter

| Channel | Indicator | | OK? |
|---|---|---|---|
| | ON | OFF | |
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

### TEST RELAYS

| Channel | Indicator | | OK? |
|---|---|---|---|
| | ON | OFF | |
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

### ACQUISITION RELAYS

| Channel | Indicator | | OK? |
|---|---|---|---|
| | ON | OFF | |
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

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## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.

### 8.1 Voltage Monitors

| Ch. | Output: TP10 to TP12 | Monitor Pins P1 | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|---|---|---|---|---|
| 1 | | Pin 1 to Pin 2 | | |
| 2 | | Pin 5 to Pin 6 | | |
| 3 | | Pin 9 to Pin 10 | | |
| 4 | | Pin 13 to Pin 14 | | |

### 8.2 Current monitors

| Ch. | Output between R29 and R130 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|---|---|---|---|---|
| 1 | | Pin 3 to Pin 4 | | |
| 2 | | Pin 7 to Pin 8 | | |
| 3 | | Pin 11 to Pin 12 | | |
| 4 | | Pin 15 to Pin 16 | | |

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**9. Filter Frequency Response Test:** Insert links W4 and W2 for each channel. Switch in the filter and test the response using the HP 35670A Dynamic Signal Analyser. Measure the transfer function between the source and the between TP10 and TP12.
This differential voltage may be measured using the SR560.

**0.1Hz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

**1Hz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

**10Hz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

**100Hz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

**1 KHz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

**5KHz**

| | Output | Specification | Pass/Fail |
|---|---|---|---|
| Ch1 | | | |
| Ch2 | | | |
| Ch3 | | | |
| Ch4 | | | |

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## 10. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

| | **Acquisition Mode: Distortion Free?** | **Non-Acquisition Mode: Distortion Free?** |
|---|---|---|
| **Ch1** | | |
| **Ch2** | | |
| **Ch3** | | |
| **Ch4** | | |

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## 11. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

### Prototype PP:

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential ride in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

| | |
|---|---|
| Stays low? | |

Very slowly increase the voltage, and observe the level at which it trips.

| | |
|---|---|
| Trip voltage? | |

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

| | |
|---|---|
| Time taken to trip? | |

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

| | |
|---|---|
| Time taken to trip? | |

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## 12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### 12.1 Noisy Mode

**With the acquisition mode switched out, and filters switched out,** apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

**100Hz**

| | Vo r.m.s | Io r.m.s (Vo/20) |
|---|---|---|
| Ch1 | | |
| Ch2 | | |
| Ch3 | | |
| Ch4 | | |

**200Hz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

**1KHz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

**5KHz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

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## 12.2 Low noise Mode

**With the acquisition mode switched out and filters switched in**, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

**100Hz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | | |
| Ch2 | | | | |
| Ch3 | | | | |
| Ch4 | | | | |

**200Hz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

**1KHz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

**5KHz**

| | Vo r.m.s | Io r.m.s (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|
| Ch1 | | | 16mA | |
| Ch2 | | | 16mA | |
| Ch3 | | | 16mA | |
| Ch4 | | | 16mA | |

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### 12.3 Acquisition Mode

**With the acquisition mode switched in, and filters switched out,** apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, aspecially if the heat sink is not fitted.

**100Hz**

| | Vo r.m.s | Vo pk. | Io pk. (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|---|
| Ch1 | | | | | |
| Ch2 | | | | | |
| Ch3 | | | | | |
| Ch4 | | | | | |

**200Hz**

| | Vo r.m.s | Vo pk. | Io pk. (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|---|
| Ch1 | | | | 400mA | |
| Ch2 | | | | 400mA | |
| Ch3 | | | | 400mA | |
| Ch4 | | | | 400mA | |

**1K Hz**

| | Vo r.m.s | Vo pk. | Io pk. (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|---|
| Ch1 | | | | 400mA | |
| Ch2 | | | | 400mA | |
| Ch3 | | | | 400mA | |
| Ch4 | | | | 400mA | |

**5K Hz**

| | Vo r.m.s | Vo pk. | Io pk. (Vo/20) | Specification | Pass/Fail |
|---|---|---|---|---|---|
| Ch1 | | | | 400mA | |
| Ch2 | | | | 400mA | |
| Ch3 | | | | 400mA | |
| Ch4 | | | | 400mA | |

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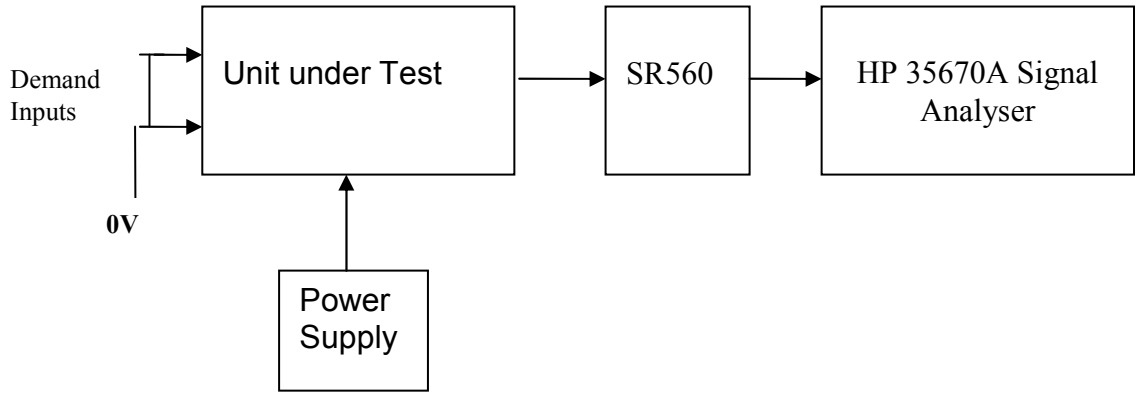
## 13 Noise Measurements

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
**Replace the filter links W4, W2 and W5 on each channel.**
**Connect the filter test box, and switch in all filters.**
**Switch it out of Test Mode and out of the Acquisition mode**
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs (TP10 and TP12). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.




### Measure the noise output at 10 Hz.

| | Spec in dB V/√Hz | Measured @ 10Hz | -60dB = |
|---|---|---|---|
| Ch1 | -155.1 | | |
| Ch2 | -155.1 | | |
| Ch3 | -155.1 | | |
| Ch4 | -155.1 | | |

### Notes:

Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

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## 14. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|---|---|---|---|---|---|---|---|---|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | | | | | | | | |
| -7v | | | | | | | | |
| -5v | | | | | | | | |
| -1v | | | | | | | | |
| 0v | | | | | | | | |
| 1v | | | | | | | | |
| 5v | | | | | | | | |
| 7v | | | | | | | | |
| 10v | | | | | | | | |