LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

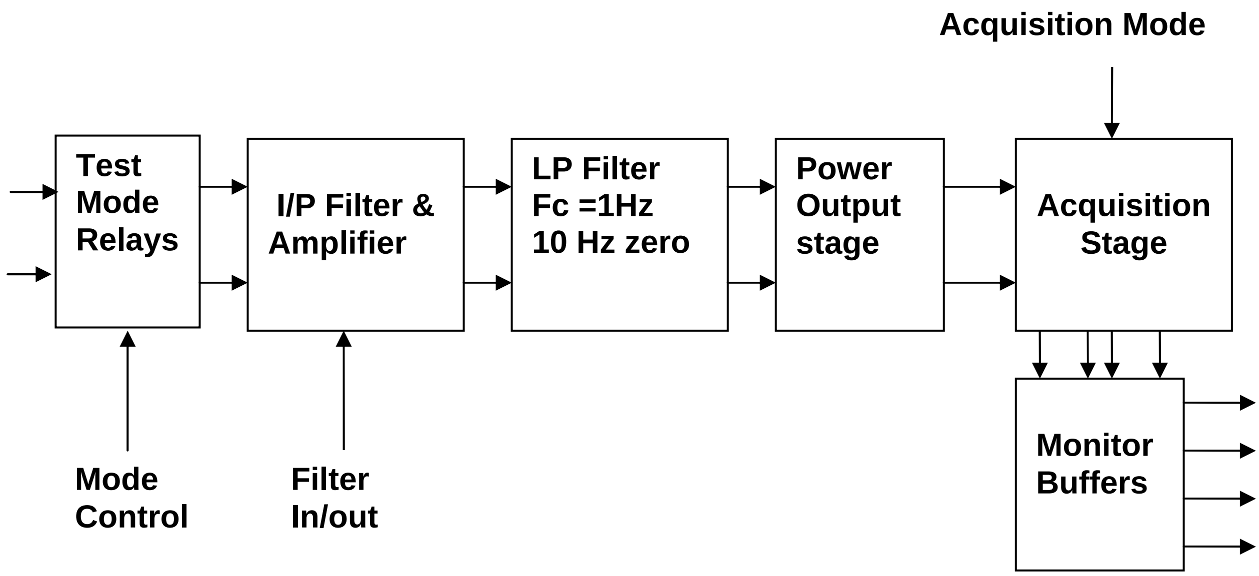
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM20P
Test Engineer ……….RMC
Date …………………..23/2/11

Contents

1. Description

Block diagram



Description

Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

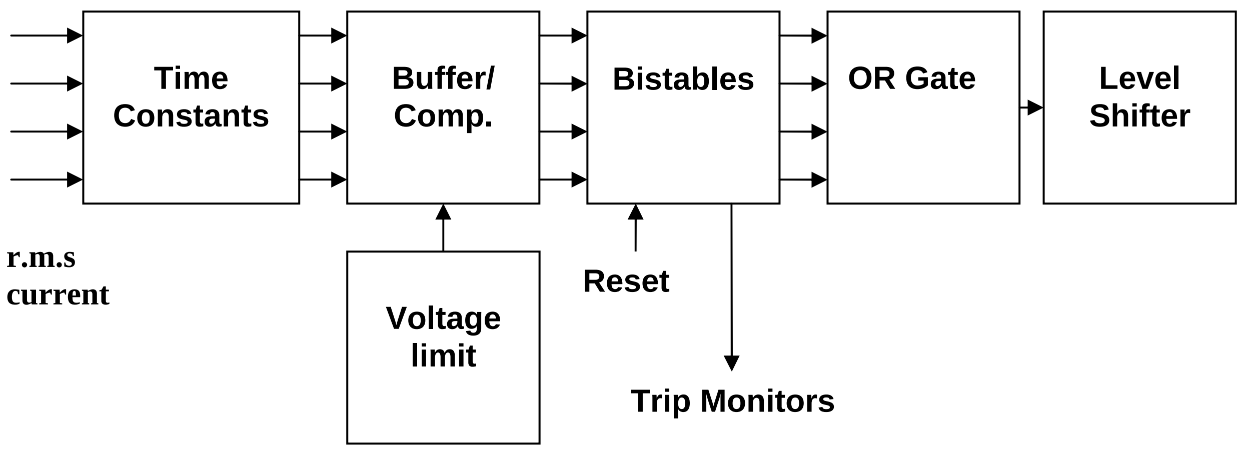
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link in place (J7/2 to 18)

Solder joint on C1, channel 4 reworked because of a dry joint.

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1, 3, 5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V			
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

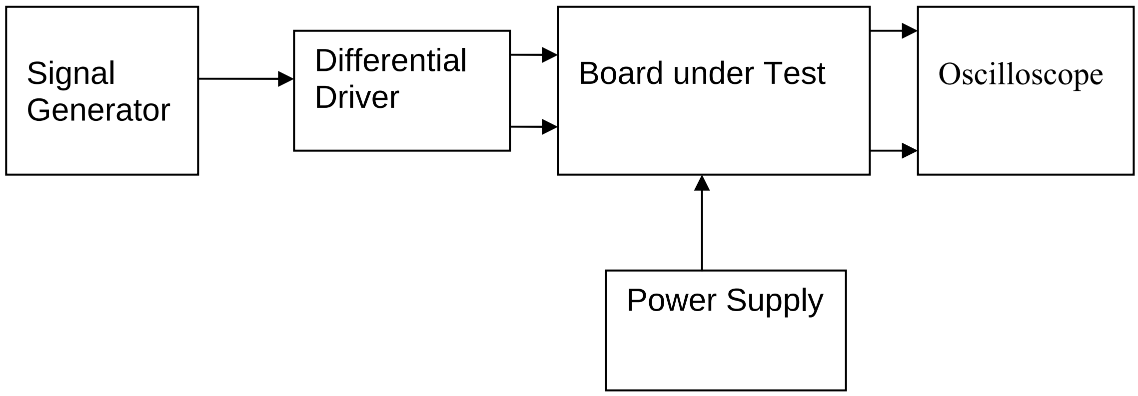
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V			
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	+12.017	√	2mV
+15v TP4	-15.040	√	1.5 mV
-15v TP6	+14.876	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pick up present

Record Power Supply Currents

Supply	**Current**
+16.5v	0.294 A
-16.5v	0.232 A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.201	Pin 1 to Pin 2	1.201	√
2	1.201	Pin 5 to Pin 6	1.200	√
3	1.200	Pin 9 to Pin 10	1.200	√
4	1.201	Pin 13 to Pin 14	1.200	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.962	Pin 3 to Pin 4	0.962	√
2	0.964	Pin 7 to Pin 8	0.964	√
3	0.964	Pin 11 to Pin 12	0.964	√
4	0.967	Pin 15 to Pin 16	0.967	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.23		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.13		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.20		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.27		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.54		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.50		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.13		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.13		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.13		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.13		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	o.472		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.476		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.469		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.465		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.16		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.18		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.18		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.18		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.18		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	5 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	40mV		33 to 45mV	-30dB to -27dB	√
Ch2	40mV		33 to 45mV	-30dB to -27dB	√
Ch3	39mV		33 to 45mV	-30dB to -27dB	√
Ch4	39 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.291		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.8 v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.2 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.3 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	**Io r.m.s (Vo/20)**
Ch1	0.498	24.9 mA
Ch2	0.495	24.7 mA
Ch3	0.489	24.4 mA
Ch4	0.494	24.7 mA

200Hz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.655	32.7 mA	**>16mA**	√
Ch2	0.654	32.7 mA	**>16mA**	√
Ch3	0.650	32.5 mA	**>16mA**	√
Ch4	0.654	32.7 mA	**>16mA**	√

1 KHz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.750	37.5 mA	**>16mA**	√
Ch2	0.750	37.5 mA	**>16mA**	√
Ch3	0.749	37.4 mA	**>16mA**	√
Ch4	0.751	37.5 mA	**>16mA**	√

5 KHz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.749	37.4 mA	**>16mA**	√
Ch2	0.750	37.5 mA	**>16mA**	√
Ch3	0.749	37.4 mA	**>16mA**	√
Ch4	0.751	37.5 mA	**>16mA**	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195	9.75 mA
Ch2	0.196	9.80 mA
Ch3	0.190	9.50 mA
Ch4	0.191	9.55 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.422	21.1 mA	>16mA	√
Ch2	0.423	21.1 mA	>16mA	√
Ch3	0.416	20.8 mA	>16mA	√
Ch4	0.415	20.7 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.4 mA	>16mA	√
Ch2	0.730	36.5 mA	>16mA	√
Ch3	0.728	36.4 mA	>16mA	√
Ch4	0.729	36.4 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	>16mA	√
Ch2	0.749	37.4 mA	>16mA	√
Ch3	0.748	37.4 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.18	5.91	295 mA
Ch2	4.18	5.91	295 mA
Ch3	4.16	5.88	294 mA
Ch4	4.15	5.87	293 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.58	7.89	394 mA	**>400mA**	
Ch2	5.59	7.90	395 mA	**>400mA**	
Ch3	5.57	7.87	393 mA	**>400mA**	
Ch4	5.56	7.86	393 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	**>400mA**	√
Ch2	6.70	9.47	473 mA	**>400mA**	√
Ch3	6.67	9.43	471 mA	**>400mA**	√
Ch4	6.68	9.33	466 mA	**>400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	**>400mA**	√
Ch2	6.72	9.50	475 mA	**>400mA**	√
Ch3	6.68	9.33	466 mA	**>400mA**	√
Ch4	6.71	9.49	474 mA	**>400mA**	√

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

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PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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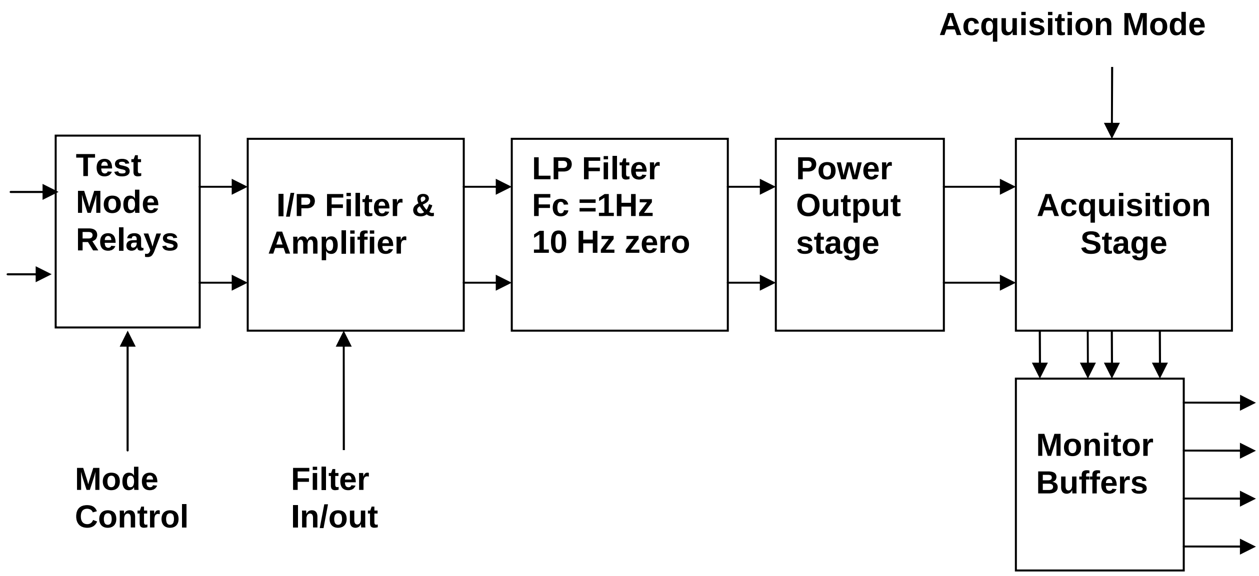
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit………PUM2P……………………Serial No ………………………………
Test Engineer ……RMC…
Date ………………4/1/2010

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

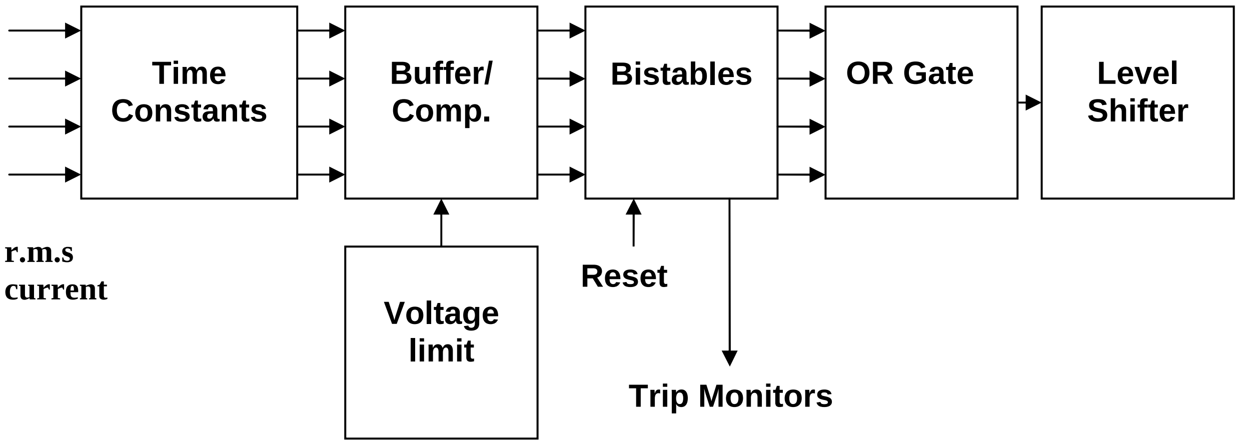
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Scope	Tektronix	2225	
PSU	Farnell	LT30-1	
PSU	Farnell	L30-2	
Calibrator	Time	1044	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the link W4 is present on each channel. √

Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header. √

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

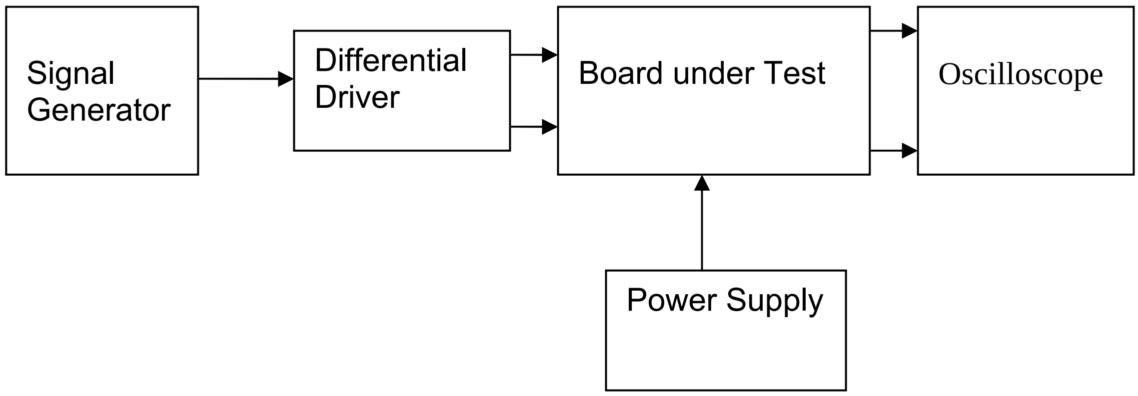
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.02v	√	1mV p/p
+15v TP4	-14.97v	√	1mV p/p
-15v TP6	-15.08v	√	5mV p/p

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	**Current**
+16.5v	0.49A
-16.5v	0.3A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.2V	Pin 1 to Pin 2	1.2V	√
2	1.2V	Pin 5 to Pin 6	1.2V	√
3	1.2V	Pin 9 to Pin 10	1.2V	√
4	1.2V	Pin 13 to Pin 14	1.2V	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.186V	Pin 3 to Pin 4	1.186V	√
2	1.186V	Pin 7 to Pin 8	1.186V	√
3	1.186V	Pin 11 to Pin 12	1.186V	√
4	1.186V	Pin 15 to Pin 16	1.186V	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.3dB	1.3dB	**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch2	7.53dB	1.53dB	**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch3	7.46dB	1.46dB	**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch4	7.35dB	1.35dB	**1.0 to 1.3v**	**0.4 to 2.4dB**	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.38	-5.62	**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch2	0.58	-5.42	**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch3	0.47	-5.53	**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch4	0.39	-5.63	**0.48 to 0.6v**	**-6.5 to -4.5dB**	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-11.46	-17.46	**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch2	-11.47	-17.47	**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch3	-11.43	-17.43	**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch4	-11.43	-17.43	**0.12 to 0.15v**	**-16.5 to -18.5dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-0.4	-6.4	**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch2	-0.48	-6.48	**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch3	-0.33	-6.33	**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch4	-0.32	-6.32	**0.42 to 0.52v**	**-5.5 to -7.5dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.06	1.06	**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch2	7.3	1.3	**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch3	7.31	1.31	**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch4	7.31	1.31	**1.0 to 1.28v**	**0.34 to 2.34dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.5	1.5	**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch2	7.45	1.45	**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch3	7.49	1.49	**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch4	7.49	1.49	**1.0 to 1.3v**	**0.5 to 2.5dB**	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-39.3	-45.3	0.3 to 0.4mV	-70dB to -65dB	
Ch2	-39.3	-45.3	0.3 to 0.4mV	-70dB to -65dB	
Ch3	38.3	-44.3	0.3 to 0.4mV	-70dB to -65dB	
Ch4	-39.4	-45.4	0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-37.6	-43.6	3.3 to 4.2mV	-50dB to -45dB	
Ch2	-37.6	-43.6	3.3 to 4.2mV	-50dB to -45dB	
Ch3	-37.6	-43.6	3.3 to 4.2mV	-50dB to -45dB	
Ch4	-37.5	-43.5	3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-22.4	-28.4	33 to 45mV	-30dB to -27dB	√
Ch2	-22.4	-28.4	33 to 45mV	-30dB to -27dB	√
Ch3	-22.4	-28.4	33 to 45mV	-30dB to -27dB	√
Ch4	-22.3	-28.3	33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-4.63	-10.63	0.275 to 0.32V	-12dB to -9dB	√
Ch2	-4.63	-10.63	0.275 to 0.32V	-12dB to -9dB	√
Ch3	-4.65	-10.65	0.275 to 0.32V	-12dB to -9dB	√
Ch4	-4.55	-10.55	0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-0.52	-6.52	0.46 to 0.49V	-7dB to -6dB	√
Ch2	-0.52	-6.52	0.46 to 0.49V	-7dB to -6dB	√
Ch3	-0.59	-6.59	0.46 to 0.49V	-7dB to -6dB	√
Ch4	-0.53	-6.53	0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	-0.48	-6.48	0.47 to 0.49V	-7dB to -6dB	√
Ch2	-0.49	-6.49	0.47 to 0.49V	-7dB to -6dB	√
Ch3	-0.55	-6.55	0.47 to 0.49V	-7dB to -6dB	√
Ch4	-0.49	-6.49	0.47 to 0.49V	-7dB to -6dB	√

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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.18v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.3 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.4 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.

Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.234	11.7 mA
Ch2	0.235	11.75 mA
Ch3	0.234	11.7 mA
Ch4	0.234	11.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.40	20mA	**16mA**	√
Ch2	0.40	20mA	**16mA**	√
Ch3	0.40	20mA	**16mA**	√
Ch4	0.40	20mA	**16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.722	36.1 mA	**16mA**	√
Ch2	0.723	36.1 mA	**16mA**	√
Ch3	0.723	36.1 mA	**16mA**	√
Ch4	0.725	36.25 mA	**16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.754	37.7 mA	**16mA**	√
Ch2	0.754	37.7 mA	**16mA**	√
Ch3	0.754	37.7 mA	**16mA**	√
Ch4	0.756	37.8 mA	**16mA**	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	**Io r.m.s (Vo/20)**
Ch1	0.089	4.45 mA
Ch2	0.088	4.4 mA
Ch3	0.090	4.5 mA
Ch4	0.090	4.5 mA

200Hz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.257	12.85	**16mA**	√
Ch2	0.257	12.57	**16mA**	√
Ch3	0.260	13.0	**16mA**	√
Ch4	0.261	13.0	**16mA**	√

1 KHz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.698	34.9 mA	**16mA**	√
Ch2	0.702	35.1 mA	**16mA**	√
Ch3	0.702	35.1 mA	**16mA**	√
Ch4	0.704	35.2 mA	**16mA**	√

5 KHz

	Vo r.m.s	**Io r.m.s (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	0.749	37.7 mA	**16mA**	√
Ch2	0.753	37.6 mA	**16mA**	√
Ch3	0.753	37.6 mA	**16mA**	√
Ch4	0.755	37.7 mA	**16mA**	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**
Ch1	4.13	5.8	292 mA
Ch2	4.15	5.8	293 mA
Ch3	4.14	5.8	292 mA
Ch4	4.19	5.9	296 mA

200Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	5.45	7.7	385 mA	**400mA**	
Ch2	5.47	7.7	386 mA	**400mA**	
Ch3	5.39	7.6	381 mA	**400mA**	
Ch4	5.53	7.8	391 mA	**400mA**	

1 KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	5.6	7.9	396 mA	**400mA**	
Ch2	5.57	7.8	393 mA	**400mA**	
Ch3	5.55	7.8	392 mA	**400mA**	
Ch4	5.63	7.9	398 mA	**400mA**	

5KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	5.66	8.00	400 mA	**400mA**	
Ch2	5.77	8.16	400 mA	**400mA**	
Ch3	5.73	8.10	405 mA	**400mA**	
Ch4	5.74	8.11	405 mA	**400mA**	

Unit………PUM2P……………………Serial No ………………………………
Test Engineer ……RMC…
Date ………………13/1/2010

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		**J3 pins 2,7**		**J3 pins 3,8**		**J3 pins 4,9**	
	Ch1 o/p	**Ch1 stable ?**	**Ch2 o/p**	**Ch2 stable ?**	**Ch3 o/p**	**Ch3 stable ?**	**Ch4 o/p**	**Ch4 stable ?**
-10v	-12.01	√	-12.00	√	-12.00	√	-12.008	√
-7v	-8.40	√	-8.40	√	-8.41	√	-8.406	√
-5v	-6.00	√	-6.10	√	-6.00	√	-6.004	√
-1v	-1.19	√	-1.19	√	-1.200	√	-1.196	√
0v	0.00	√	-0.00	√	0.003	√	0.000	√
1v	1.19	√	1.19	√	1.200	√	1.198	√
5v	6.00	√	5.99	√	6.00	√	6.004	√
7v	8.40	√	8.39	√	8.41	√	8.405	√
10v	12.00	√	12.00	√	12.00	√	12.007	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

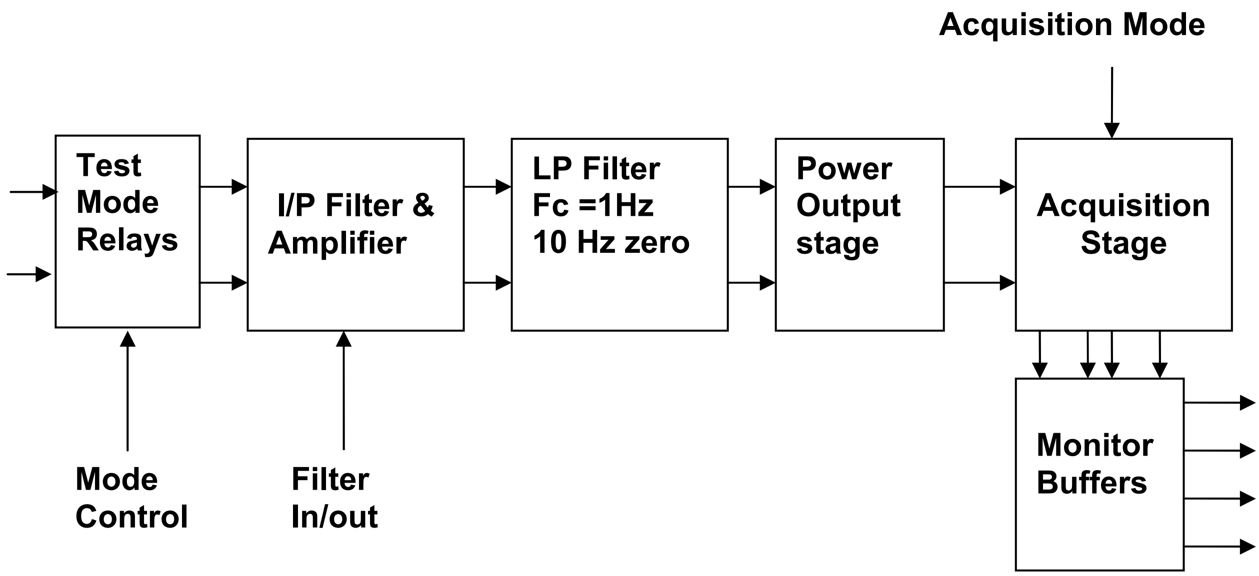
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………..PUM3P
Test Engineer ………RMC
Date …………………18/1/10

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

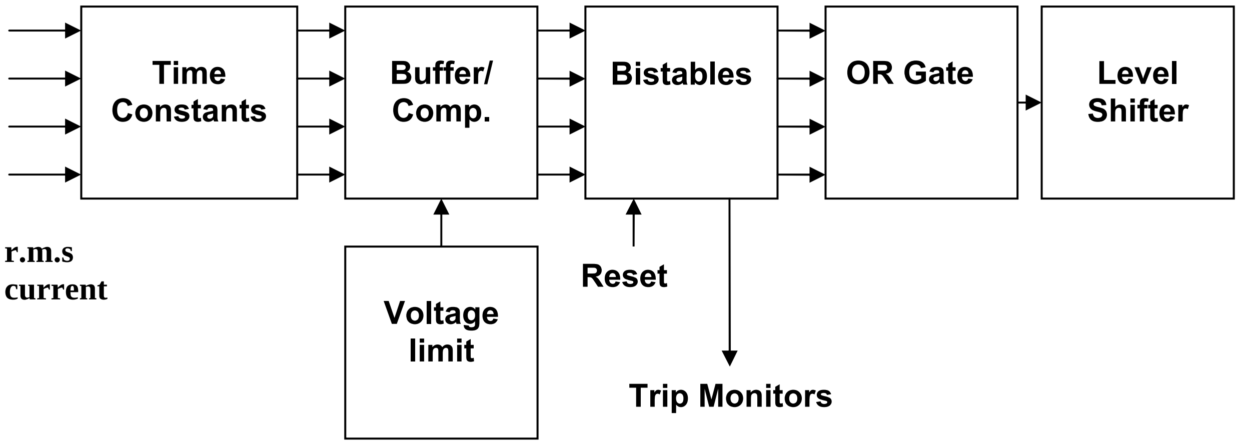
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Scope	Tektronix	2225	
PSU	Farnell	LT30-1	
PSU	Farnell	L30-2	
Calibrator	Time	1044	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Small mark on C2

Links:

Check that the link W4 is present on each channel. √
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.√

Unit……………………..PUM3P
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

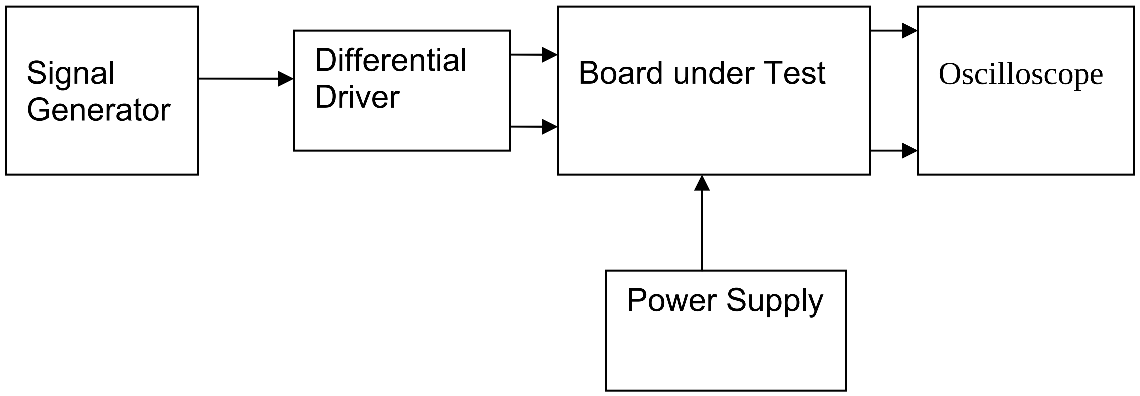
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.04	√	5 mV pk/pk
+15v TP4	14.95	√	5mV
-15v TP6	-14.95	√	25 mV

All Outputs smooth DC, no oscillation?	Occasional hf interference spike – probably pick up.

Record Power Supply Currents

Supply	Current
+16.5v	0.3A
-16.5v	0.25A

If the supplies are correct, proceed to the next test.

Unit…………………..PUM3P
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.2v	Pin 1 to Pin 2	1.2v	√
2	1.2v	Pin 5 to Pin 6	1.2v	√
3	1.2v	Pin 9 to Pin 10	1.2v	√
4	1.2v	Pin 13 to Pin 14	1.2v	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.188v	Pin 3 to Pin 4	1.188v	√
2	1.188v	Pin 7 to Pin 8	1.188v	√
3	1.188v	Pin 11 to Pin 12	1.188v	√
4	1.188v	Pin 15 to Pin 16	1.188v	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.53v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.53v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.53v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.53v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.47v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.47v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.47v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.47v		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.168v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.169v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.169v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.169v		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.193v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.194v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.194v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.193v		1.0 to 1.3v	0.5 to 2.5dB	√

Unit…………………..PUM3P
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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	6.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	6.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	6.0 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.7 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6.7 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.7 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.7 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	27 mV		33 to 45mV	-30dB to -27dB	
Ch2	27 mV		33 to 45mV	-30dB to -27dB	
Ch3	29 mV		33 to 45mV	-30dB to -27dB	
Ch4	30 mV		33 to 45mV	-30dB to -27dB	

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.289		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.466		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.471		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.468		0.47 to 0.49V	-7dB to -6dB	
Ch2	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………..PUM3P
Test Engineer ………RMC
Date …………………18/1/10

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit…………………..PUM3P
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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.195v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.5 seconds

Unit…………………..PUM3P
Test Engineer ………RMC
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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.236	11.8
Ch2	0.234	11.7
Ch3	0.234	11.7
Ch4	0.235	11.7

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.405	20.25	>16mA	√
Ch2	0.403	20.15	>16mA	√
Ch3	0.403	20.15	>16mA	√
Ch4	0.404	20.2	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724	36.2	>16mA	√
Ch2	0.724	36.2	>16mA	√
Ch3	0.724	36.2	>16mA	√
Ch4	0.725	36.2	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.755	37.75	>16mA	√
Ch2	0.755	37.75	>16mA	√
Ch3	0.755	37.75	>16mA	√
Ch4	0.756	37.8	>16mA	√

Unit…………………..PUM3P
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.09	4.5 mA
Ch2	0.09	4.5 mA
Ch3	0.09	4.5 mA
Ch4	0.089	4.45 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.259	12.95 mA	>16mA	
Ch2	0.259	12.95 mA	>16mA	
Ch3	0.259	12.95 mA	>16mA	
Ch4	0.258	12.90 mA	>16mA	

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.703	35.15 mA	>16mA	√
Ch2	0.703	35.15 mA	>16mA	√
Ch3	0.703	35.15 mA	>16mA	√
Ch4	0.704	35.20 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.754	37.7 mA	>16mA	√
Ch2	0.754	37.7 mA	>16mA	√
Ch3	0.754	37.7 mA	>16mA	√
Ch4	0.755	37.75 mA	>16mA	√

Unit…………………..PUM3P
Test Engineer ………RMC
Date …………………19/1/10

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.163	5.887	294 mA
Ch2	4.165	5.890	294 mA
Ch3	4.174	5.902	295 mA
Ch4	4.192	5.928	296 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.36	7.58	379 mA	**>400mA**	
Ch2	5.48	7.75	387 mA	**>400mA**	
Ch3	5.50	7.79	389 mA	**>400mA**	
Ch4	5.53	7.82	391 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.52	7.806	390 mA	**>400mA**	
Ch2	5.64	7.976	398 mA	**>400mA**	
Ch3	5.60	7.917	396 mA	**>400mA**	
Ch4	5.63	7.962	398 mA	**>400mA**	

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.61	7.934	396.6 mA	**>400mA**	
Ch2	5.59	7.805	395.3 mA	**>400mA**	
Ch3	5.60	7.919	395.9 mA	**>400mA**	
Ch4	5.58	7.891	394.5 mA	**>400mA**	

Unit…………………..PUM3P
Test Engineer ………RMC
Date …………………19/1/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	December 2009
	PUM Driver Board Test Report	
	R. M. Cutler, University of Birmingham	

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

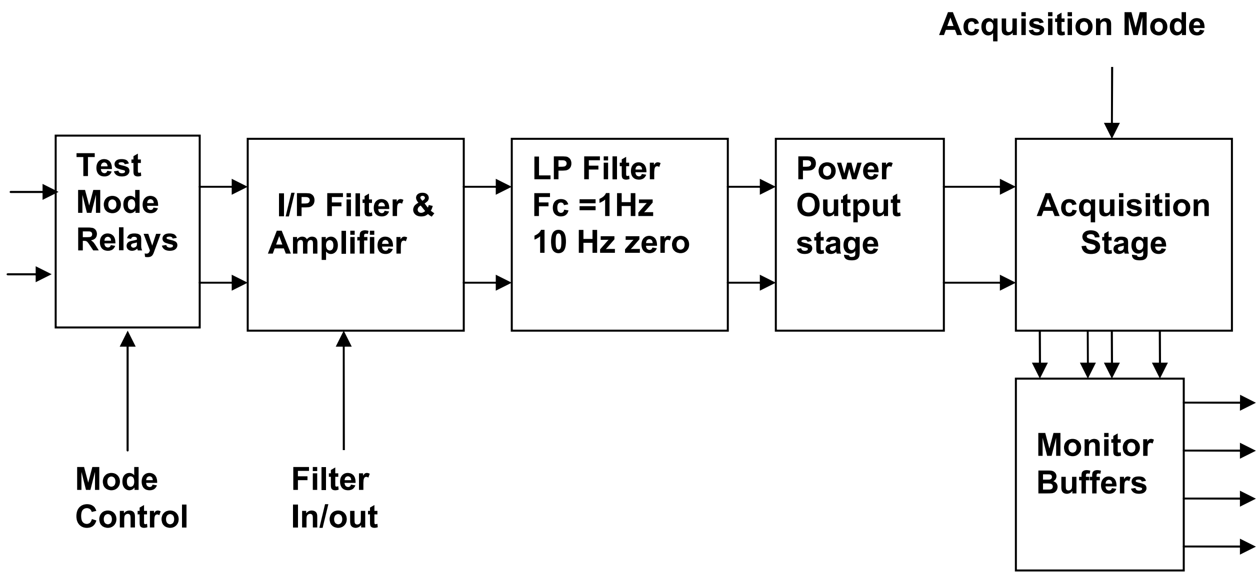
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/4/10

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

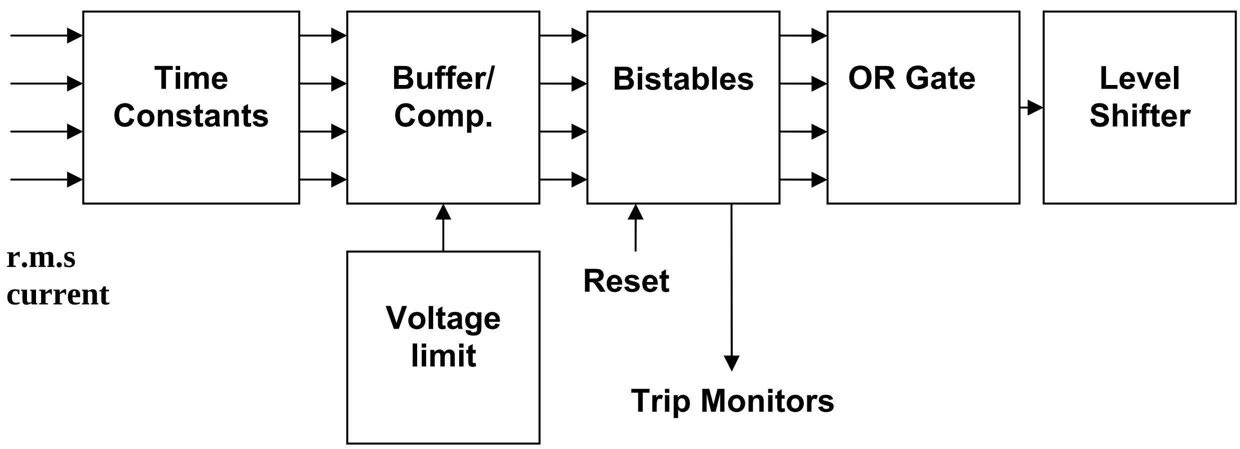
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit……………………..PUM4P
Test Engineer ………RMC
Date …………………6/4/10

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Scope	Tektronix	2225	
PSU	Farnell	LT30-1	
PSU	Farnell	L30-2	
Calibrator	Time	1044	

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the link W4 is present on each channel. √
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.√

Unit……………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

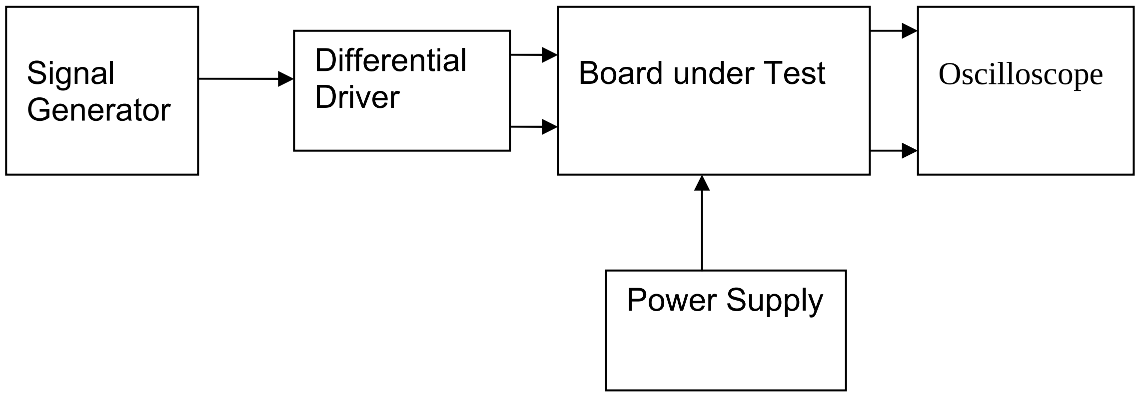
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.04	√	1 mV pk/pk
+15v TP4	14.95	√	1 mV
-15v TP6	-14.95	√	5 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.55A
-16.5v	0.29A

If the supplies are correct, proceed to the next test.

Unit……………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.2v	Pin 1 to Pin 2	1.2v	√
2	1.2v	Pin 5 to Pin 6	1.2v	√
3	1.2v	Pin 9 to Pin 10	1.2v	√
4	1.2v	Pin 13 to Pin 14	1.2v	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.985v	Pin 3 to Pin 4	0.985	√
2	0.985v	Pin 7 to Pin 8	0.984	√
3	0.985v	Pin 11 to Pin 12	0.985	√
4	0.987v	Pin 15 to Pin 16	0.985	√

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.1v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.13v		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.468v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.462v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.460v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.472v		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.13v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.12v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.12v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.12v		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.193v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.194v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.194v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.193v		1.0 to 1.3v	0.5 to 2.5dB	√

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	30 mV		33 to 45mV	-30dB to -27dB	
Ch2	28 mV		33 to 45mV	-30dB to -27dB	
Ch3	28 mV		33 to 45mV	-30dB to -27dB	
Ch4	28 mV		33 to 45mV	-30dB to -27dB	

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.291		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.466		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.471		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.477		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.477		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Power supply current limited operated, so changed to the 2Amp supply.

Unit.......................PUM4P
Test Engineer ....RMC
Date 13/5/10

12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.213v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.23	11.5 mA
Ch2	0.23	11.5 mA
Ch3	0.23	11.5 mA
Ch4	0.23	11.5 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.40	20 mA	>16mA	√
Ch2	0.40	20 mA	>16mA	√
Ch3	0.40	20 mA	>16mA	√
Ch4	0.40	20 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.72	36 mA	>16mA	√
Ch2	0.72	36 mA	>16mA	√
Ch3	0.72	36 mA	>16mA	√
Ch4	0.72	36 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.753	37.6 mA	>16mA	√
Ch2	0.753	37.6 mA	>16mA	√
Ch3	0.753	37.6 mA	>16mA	√
Ch4	0.753	37.6 mA	>16mA	√

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………6/5/10

12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.09	4.5 mA
Ch2	0.065	3.25 mA
Ch3	0.088	4.4 mA
Ch4	0.09	4.5 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.258	12.9 mA	>16mA	
Ch2	0.257	12.8 mA	>16mA	
Ch3	0.255	12.7 mA	>16mA	
Ch4	0.262	13.1 mA	>16mA	

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.7011	35 mA	>16mA	√
Ch2	0.7013	35 mA	>16mA	√
Ch3	0.7001	35 mA	>16mA	√
Ch4	0.7022	35 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.751	37.5 mA	>16mA	√
Ch2	0.751	37.5 mA	>16mA	√
Ch3	0.751	37.5 mA	>16mA	√
Ch4	0.751	37.5 mA	>16mA	√

Unit…………………..PUM4P
Test Engineer ………RMC
Date …………………12/5/10

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12	5.826	291 mA
Ch2	4.12	5.826	291 mA
Ch3	4.10	5.798	289 mA
Ch4	4.10	5.798	289 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.62	7.947	397 mA	>400mA	
Ch2	5.62	7.947	397 mA	>400mA	
Ch3	5.616	7.942	397 mA	>400mA	
Ch4	5.62	7.947	397 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.68	9.446	472.2 mA	>400mA	√
Ch2	6.68	9.446	472.2 mA	>400mA	√
Ch3	6.68	9.446	472.2 mA	>400mA	√
Ch4	6.70	9.475	473.7 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.843	9.677	483.8 mA	>400mA	√
Ch2	6.858	9.698	484.9 mA	>400mA	√
Ch3	6.83	9.659	482.9 mA	>400mA	√
Ch4	6.85	9.687	484.3 mA	>400mA	√

Unit……………………..PUM4P
Test Engineer ………RMC
Date …………………13/5/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

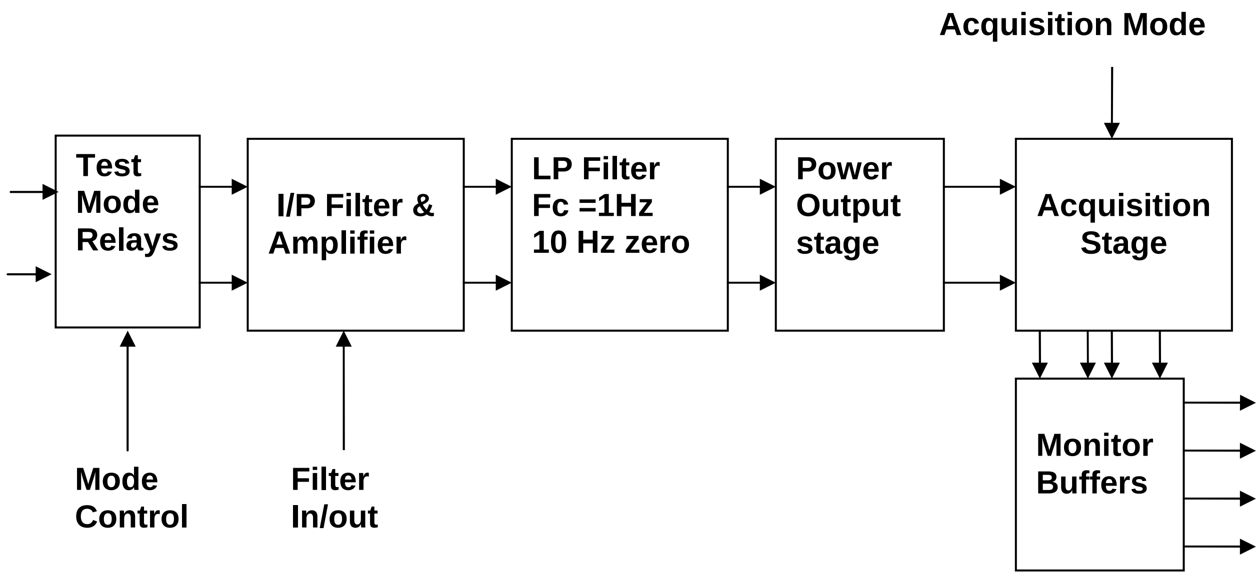
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM5P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………2/12/10

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

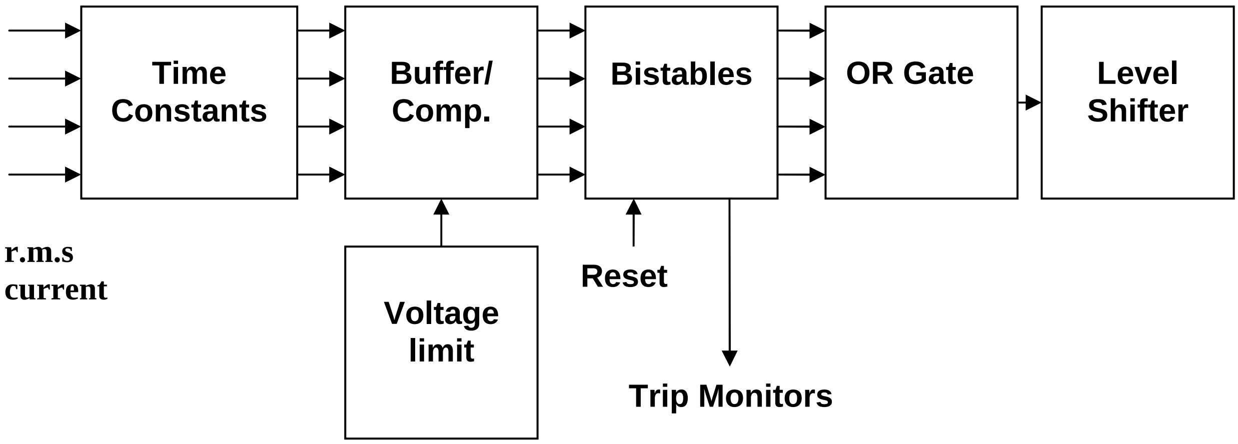
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit…………………PUM5……………Serial No ………………………………
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

Unit…………………PUM5P…………Serial No ………………………………
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

IC10 and IC11: AD797s replaced by AD8671

Ch 3 IC11 pin 7 track repaired.

RESET PULSE MOD

J7/2 Connected to J7/18 on 10/1/11

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………PUM5P…………Serial No ………………………………
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

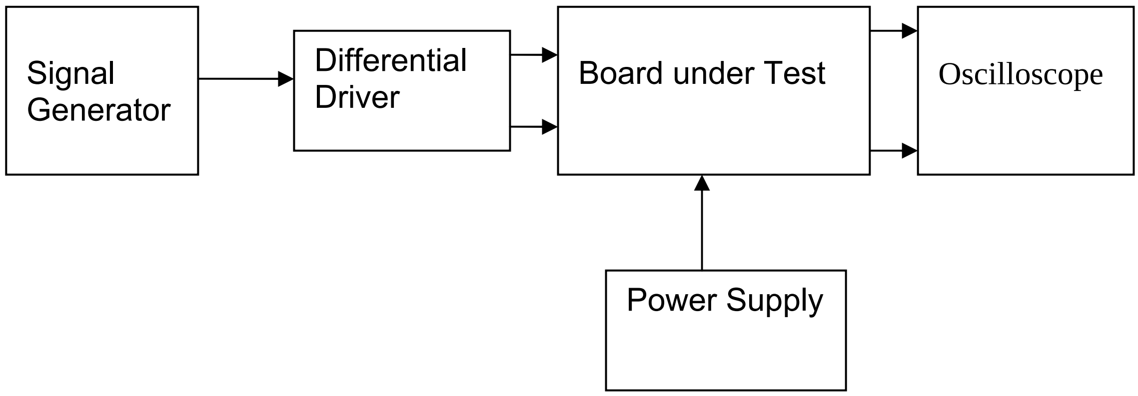
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM5P…………Serial No ………………………………
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.0v	√	1mV pk/pk
+15v TP4	14.9v	√	1.2 mV pk/pk
-15v TP6	-15.5v	√	5mV pk/pk

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.34 A
-16.5v	0.24 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM5P…………Serial No ………………………………
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1			√
Ch2			√
Ch3			√
Ch4			√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.0049	Pin 1 to Pin 2	1.0044	√
2	1.0048	Pin 5 to Pin 6	1.0043	√
3	1.0051	Pin 9 to Pin 10	1.0048	√
4	1.0048	Pin 13 to Pin 14	1.0047	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.8065	Pin 3 to Pin 4	0.8064	√
2	0.8072	Pin 7 to Pin 8	0.8071	√
3	0.8101	Pin 11 to Pin 12	0.8101	√
4	0.8073	Pin 15 to Pin 16	0.8075	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.3v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.3v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.3v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.3v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.55v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.135v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.135v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.14v		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.135v		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.48v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.49v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.49v		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.49v		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.18v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.2v		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.2v		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.2v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.21v		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.21v		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	6mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	6mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	6mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	40mV		33 to 45mV	-30dB to -27dB	√
Ch2	40mV		33 to 45mV	-30dB to -27dB	√
Ch3	40mV		33 to 45mV	-30dB to -27dB	√
Ch4	40mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.25v		0.275 to 0.32V	-12dB to -9dB	
Ch2	0.25v		0.275 to 0.32V	-12dB to -9dB	
Ch3	0.25v		0.275 to 0.32V	-12dB to -9dB	
Ch4	0.25v		0.275 to 0.32V	-12dB to -9dB	

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.49v		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0,49v		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.49v		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.49v		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.49v		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0,49v		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.49v		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.49v		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM5P…………Serial No ………………………………
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	OK

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.18v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.75 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.5 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.

Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.488	24.4mA
Ch2	0.492v	24.6mA
Ch3	0.499v	24.9mA
Ch4	0.49v	24.5mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.647v	32.3 mA	>16mA	√
Ch2	0.650v	32.5 mA	>16mA	√
Ch3	0.654v	32.7mA	>16mA	√
Ch4	0.648v	32.4mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745v	37.25mA	>16mA	√
Ch2	0.747v	37.35mA	>16mA	√
Ch3	0.746v	37.3mA	>16mA	√
Ch4	0.744v	37.2mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745v	37.25mA	>16mA	√
Ch2	0.747v	37.35mA	>16mA	√
Ch3	0.745v	37.25mA	>16mA	√
Ch4	0.744v	37.2mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.190v	9.5 mA
Ch2	0.193v	9.65 mA
Ch3	0.200v	10 mA
Ch4	0.192v	9.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.415v	20.75 mA	**>16mA**	√
Ch2	0.418v	20.9 mA	**>16mA**	√
Ch3	0.427v	21.35 mA	**>16mA**	√
Ch4	0.416v	20.8 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724v	36.2 mA	**>16mA**	√
Ch2	0.726v	36.3 mA	**>16mA**	√
Ch3	0.726v	36.3 mA	**>16mA**	√
Ch4	0.723v	36.15 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744v	37.2 mA	**>16mA**	√
Ch2	0.726v	36.3 mA	**>16mA**	√
Ch3	0.745v	37.25 mA	**>16mA**	√
Ch4	0.724v	36.2 mA	**>16mA**	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**
Ch1	4.15v	5.86	293 mA
Ch2	4.14v	5.85	292 mA
Ch3	4.10v	5.79	289 mA
Ch4	4.11v	5.81	290 mA

200Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	5.53v	7.82	391 mA	**>400mA**	
Ch2	5.51v	7.79	389 mA	**>400mA**	
Ch3	5.50v	7.78	389 mA	**>400mA**	
Ch4	5.49v	7.76	388 mA	**>400mA**	

1 KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	6.6v	9.33	466 mA	**>400mA**	√
Ch2	6.6v	9.33	466 mA	**>400mA**	√
Ch3	6.6v	9.33	466 mA	**>400mA**	√
Ch4	6.57v	9.29	464 mA	**>400mA**	√

5 KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	6.64v	9.39	469 mA	**>400mA**	√
Ch2	6.62v	9.36	468 mA	**>400mA**	√
Ch3	6.62v	9.36	468 mA	**>400mA**	√
Ch4	6.61v	9.34	467 mA	**>400mA**	√

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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP10 and TP12. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit………………PUM6 P………..Serial No ………………………………
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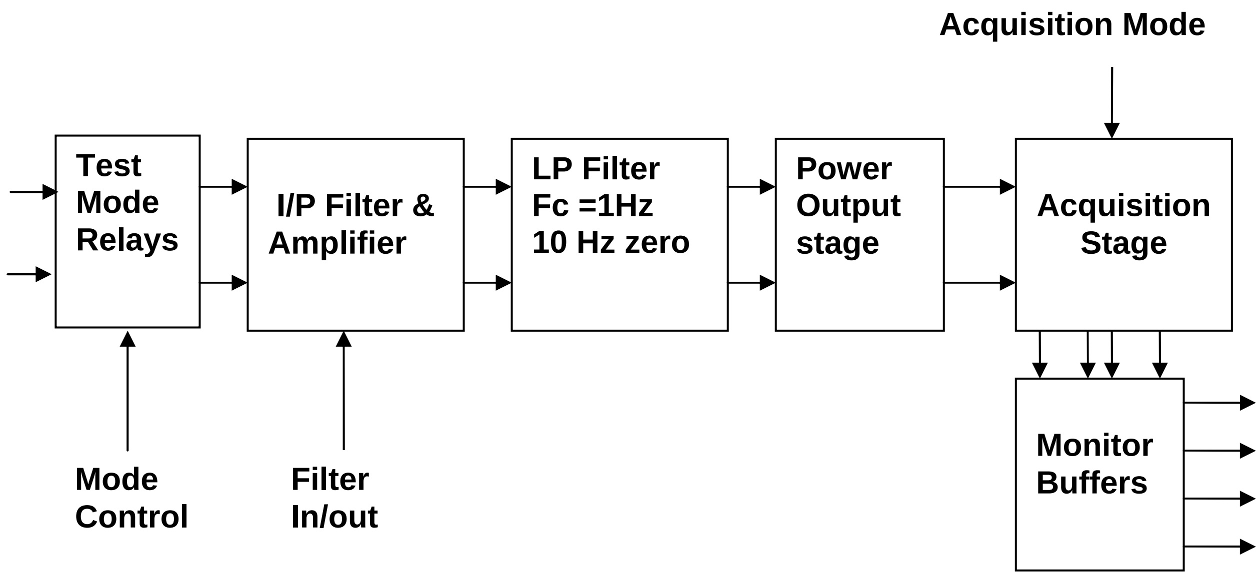
Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

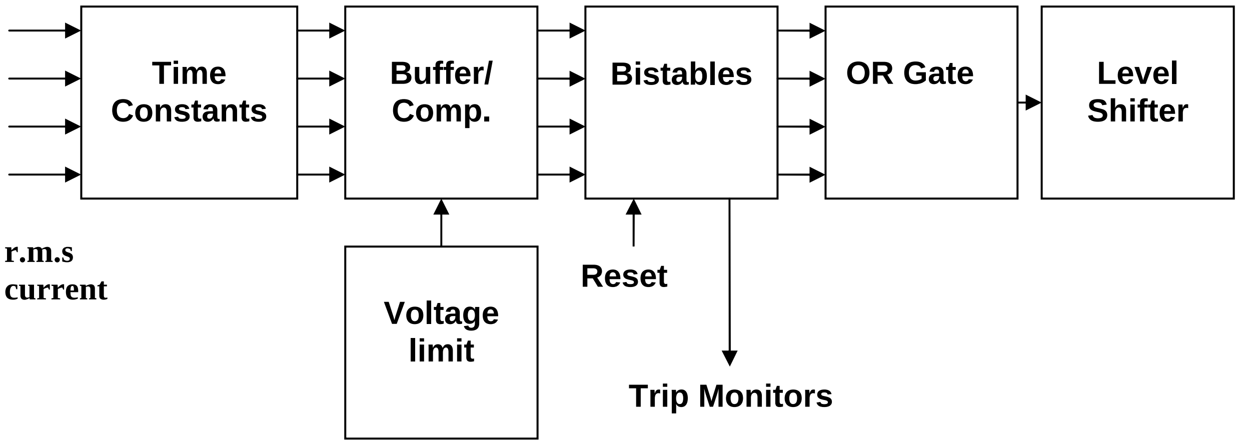
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

IC10 and IC11 Changed to AD8671 on all channels

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:
Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

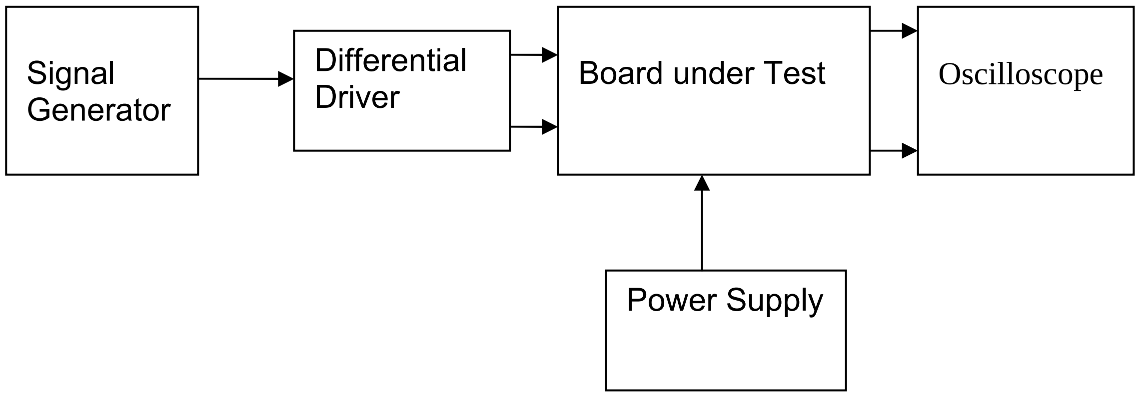
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.048v	√	1.2 mV pk/pk
+15v TP4	+14.9v	√	2mV pk/pk
-15v TP6	-15.15v	√	7mV pk/pk

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.505A
-16.5v	0.317A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.204v	Pin 1 to Pin 2	1.204v	√
2	1.204v	Pin 5 to Pin 6	1.204v	√
3	1.204v	Pin 9 to Pin 10	1.204v	√
4	1.204v	Pin 13 to Pin 14	1.204v	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.967v	Pin 3 to Pin 4	0.966v	√
2	0.967v	Pin 7 to Pin 8	0.967v	√
3	0.969v	Pin 11 to Pin 12	0.968v	√
4	0.963v	Pin 15 to Pin 16	0.963v	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.51v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.51v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.51v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.51v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.4753		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.4735		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.4742		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.4697		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.167		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.167		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.167		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.166		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.1938		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.1937		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.1938		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.1936		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	5mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	5mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	5mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	37mV		33 to 45mV	-30dB to -27dB	√
Ch2	36mV		33 to 45mV	-30dB to -27dB	√
Ch3	35mV		33 to 45mV	-30dB to -27dB	√
Ch4	37mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.296		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.4717		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.4729		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.4718		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.4722		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.4729		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.4742		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.4730		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.4736		0.47 to 0.49V	-7dB to -6dB	√

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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	Yes

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.1722v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.25 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.3 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.490	24.5 mA
Ch2	0.495	24.75 mA
Ch3	0.494	24.7 mA
Ch4	0.489	24.4 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.649	32.45 mA	>16mA	√
Ch2	0.653	32.65 mA	>16mA	√
Ch3	0.651	32.55 mA	>16mA	√
Ch4	0.648	32.4 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.747	37.35 mA	>16mA	√
Ch2	0.748	37.3 mA	>16mA	√
Ch3	0.746	37.3 mA	>16mA	√
Ch4	0.744	37.2 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.715	35.75 mA	>16mA	√
Ch2	0.747	37.35 mA	>16mA	√
Ch3	0.745	37.25 mA	>16mA	√
Ch4	0.743	37.15 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.195	9.75 mA
Ch3	0.194	9.70 mA
Ch4	0.192	9.60 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.419	20.95 mA	**>16mA**	√
Ch2	0.420	21.00 mA	**>16mA**	√
Ch3	0.419	20.95 mA	**>16mA**	√
Ch4	0.414	20.70 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.726	36.30 mA	**>16mA**	√
Ch2	0.726	36.30 mA	**>16mA**	√
Ch3	0.725	35.25 mA	**>16mA**	√
Ch4	0.723	36.15 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.746	37.30 mA	**>16mA**	√
Ch2	0.746	37.30 mA	**>16mA**	√
Ch3	0.745	37.25 mA	**>16mA**	√
Ch4	0.743	37.15 mA	**>16mA**	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.13	5.84	292 mA
Ch2	4.13	5.84	292 mA
Ch3	4.09	5.78	289 mA
Ch4	4.16	5.88	295 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.50	7.78	389 mA	**>400mA**	
Ch2	5.50	7.78	389 mA	**>400mA**	
Ch3	5.47	7.73	386 mA	**>400mA**	
Ch4	5.53	7.82	391 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.62	9.36	468 mA	**>400mA**	√
Ch2	6.62	9.36	468 mA	**>400mA**	√
Ch3	6.59	9.32	466 mA	**>400mA**	√
Ch4	6.60	9.33	466 mA	**>400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.64	9.39	469 mA	**>400mA**	√
Ch2	6.64	9.39	469 mA	**>400mA**	√
Ch3	6.62.	9.36	468 mA	**>400mA**	√
Ch4	6.62	9.36	468 mA	**>400mA**	√

Unit………………PUM6 P…………Serial No ………………………………
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

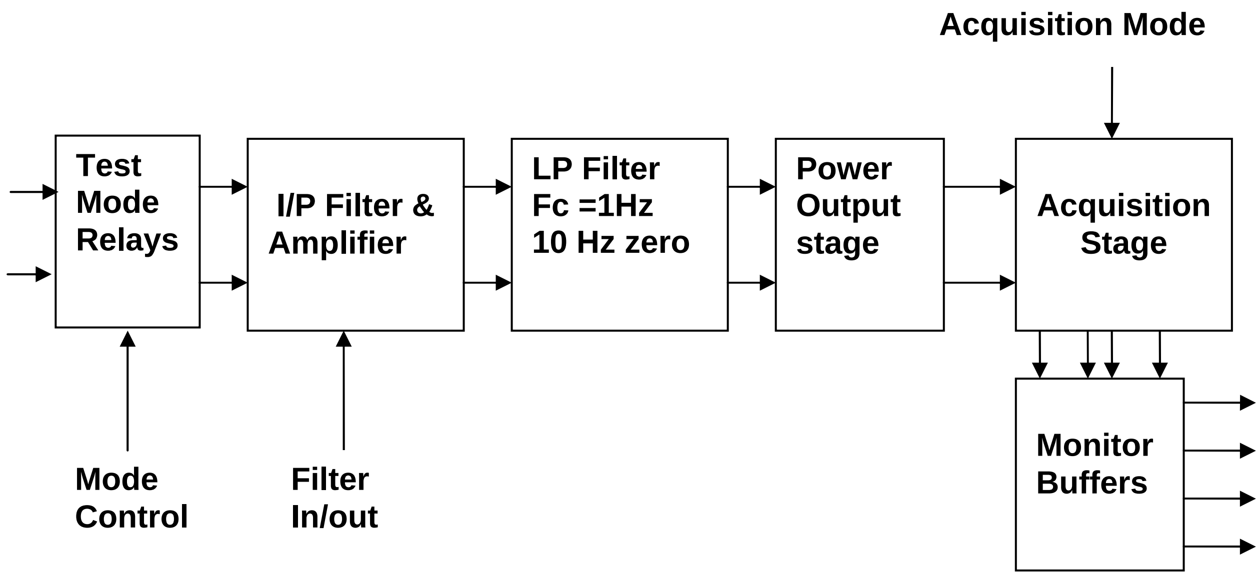
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM 7P
Test Engineer ……..RMC
Date ………………13/12/10

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

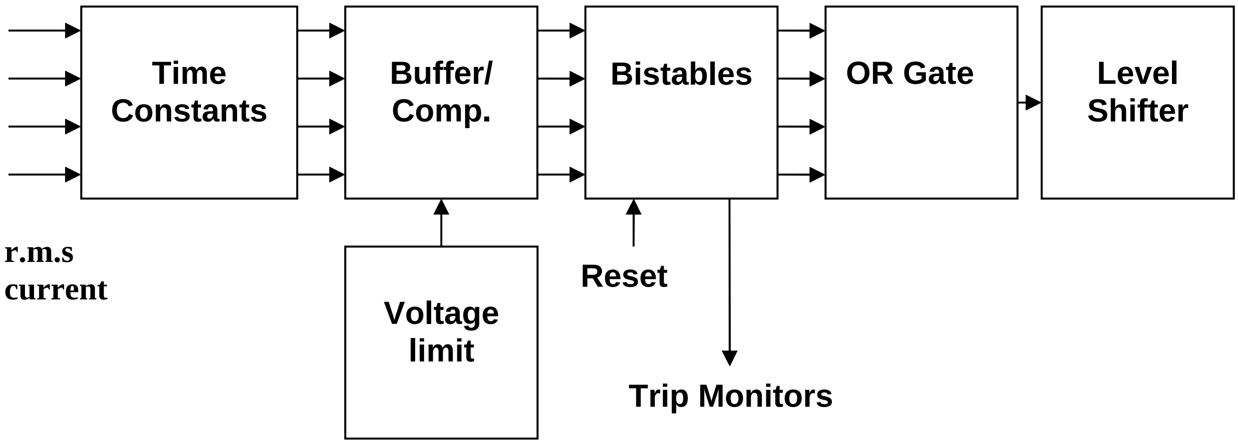
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

IC10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:
Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V			
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

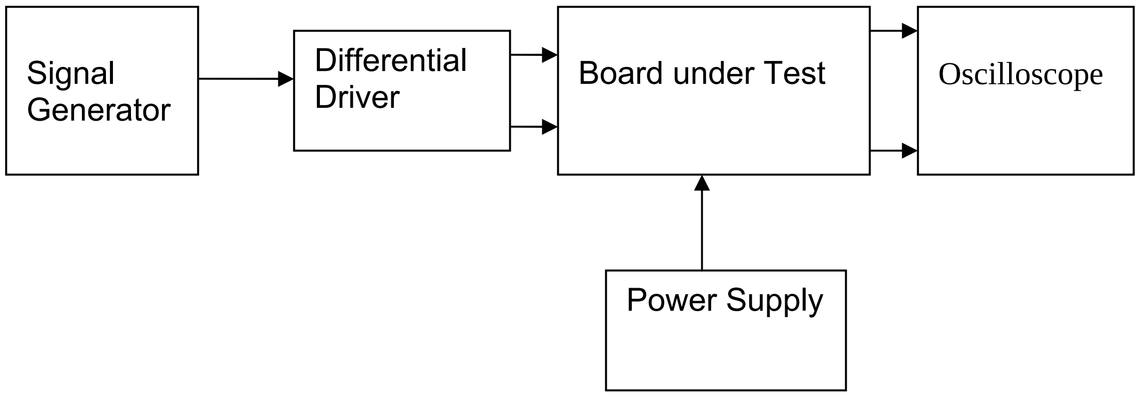
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.052v	√	1mV
+15v TP4	14.939v	√	1mV
-15v TP6	-15.012v	√	6mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	Current
+16.5v	0.3A
-16.5v	0.22A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.2069	Pin 1 to Pin 2	1.2065	√
2	1.2066	Pin 5 to Pin 6	1.2050	√
3	1.2066	Pin 9 to Pin 10	1.2063	√
4	1.2069	Pin 13 to Pin 14	1.2060	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.985	Pin 3 to Pin 4	0.982	√
2	0.967	Pin 7 to Pin 8	0.966	√
3	0.967	Pin 11 to Pin 12	0.967	√
4	0.965	Pin 15 to Pin 16	0.965	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.480		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.479		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.479		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.477		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.177		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.176		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.176		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.176		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.200		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.199		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.199		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.199		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.2 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	37 mV		33 to 45mV	-30dB to -27dB	√
Ch2	34 mV		33 to 45mV	-30dB to -27dB	√
Ch3	34 mV		33 to 45mV	-30dB to -27dB	√
Ch4	36 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.292		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.474		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.475		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.475		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.19v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.7 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.495	24.75 mA
Ch2	0.492	24.6 mA
Ch3	0.494	24.7 mA
Ch4	0.493	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.651	32.55 mA	>16mA	√
Ch2	0.650	32.5 mA	>16mA	√
Ch3	0.650	32.5 mA	>16mA	√
Ch4	0.650	32.5 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744	37.2 mA	>16mA	√
Ch2	0.745	37.2 mA	>16mA	√
Ch3	0.745	37.2 mA	>16mA	√
Ch4	0.744	37.2 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744	37.2 mA	>16mA	√
Ch2	0.745	37.2 mA	>16mA	√
Ch3	0.755	37.7 mA	>16mA	√
Ch4	0.744	37.2 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.195	9.75 mA
Ch3	0.195	9.75 mA
Ch4	0.194	9.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.42	21 mA	>16mA	√
Ch2	0.42	21 mA	>16mA	√
Ch3	0.42	21 mA	>16mA	√
Ch4	0.42	21 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.725	36.29 mA	>16mA	√
Ch2	0.726	36.3 mA	>16mA	√
Ch3	0.726	36.3 mA	>16mA	√
Ch4	0.724	36.2 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744	37.2 mA	>16mA	√
Ch2	0.745	37.25 mA	>16mA	√
Ch3	0.744	37.25 mA	>16mA	√
Ch4	0.743	37.15 mA	>16mA	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.10	5.8	289 mA
Ch2	4.10	5.8	289 mA
Ch3	4.01	5.67	283 mA
Ch4	4.08	5.77	288 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.48	7.74	387 mA	>400mA	
Ch2	5.48	7.74	387 mA	>400mA	
Ch3	5.48	7.74	387 mA	>400mA	
Ch4	5.45	7.70	385 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.44	9.1	455 mA	>400mA	√
Ch2	6.44	9.1	455 mA	>400mA	√
Ch3	6.43	9.09	454 mA	>400mA	√
Ch4	6.37	9.00	450 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.6	9.33	466 mA	>400mA	√
Ch2	6.6	9.33	466 mA	>400mA	√
Ch3	6.6	9.33	466 mA	>400mA	√
Ch4	6.56	9.27	463 mA	>400mA	√

Unit…………………PUM 7P
Test Engineer ……..RMC
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

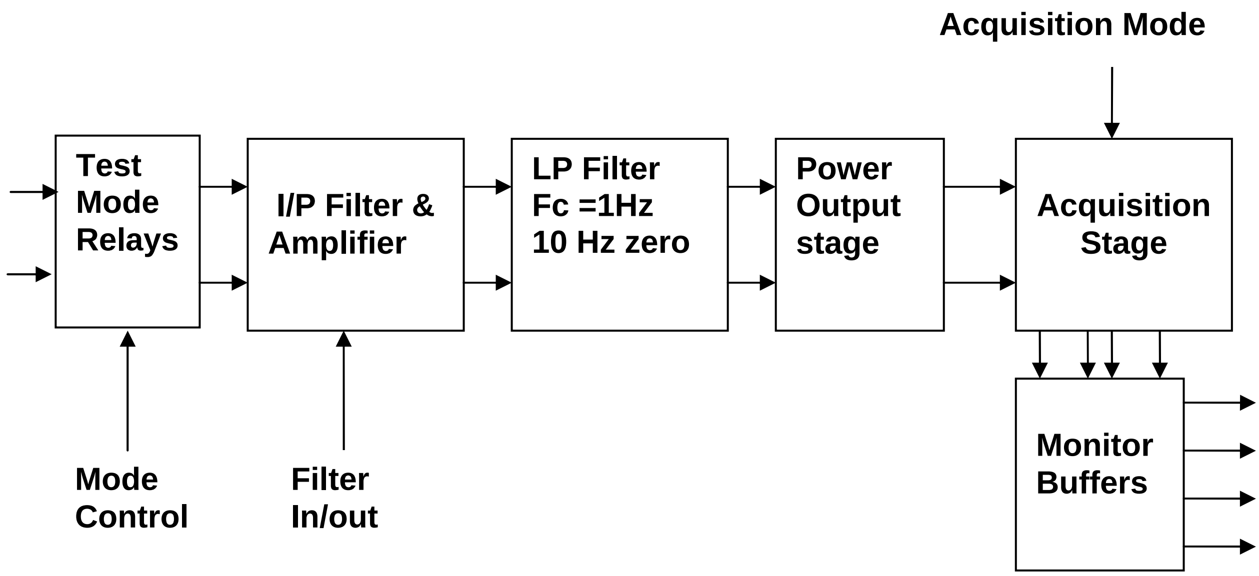
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM 8P
Test Engineer ………RMC
Date …………………14/12/10

Contents

1. Description

Block diagram



Description

Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

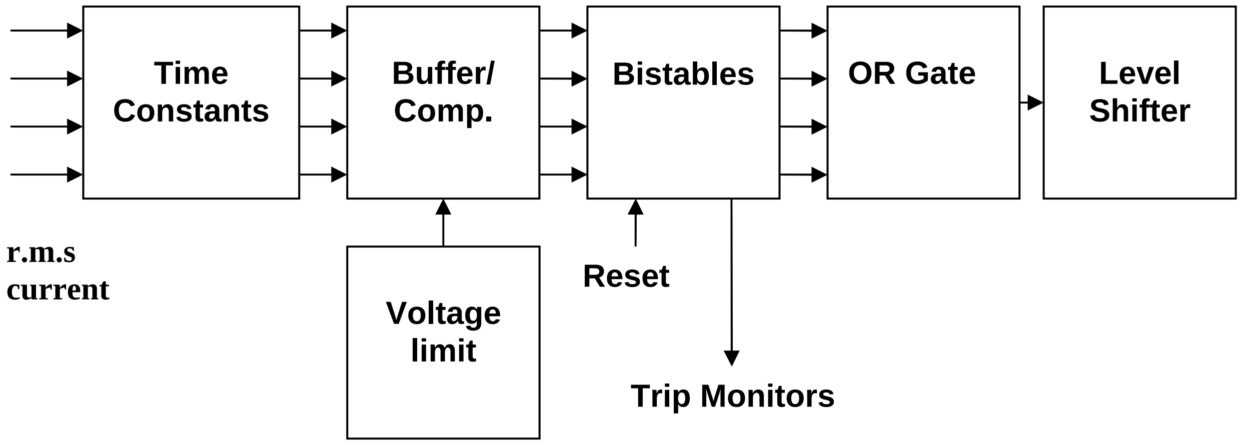
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

IC10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………..PUM 8P
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

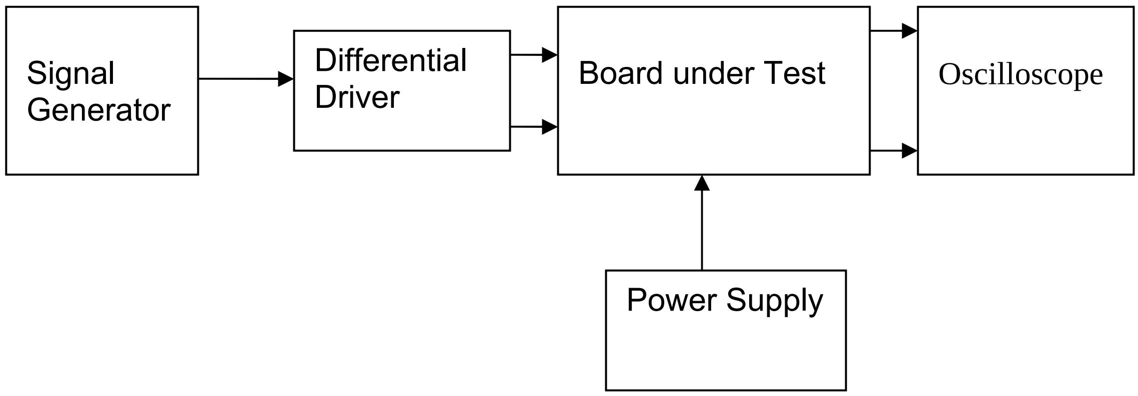
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.0v	√	1.2 mV
+15v TP4	14.9v	√	1.3mV
-15v TP6	-15.0v	√	6 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.303A
-16.5v	0.242A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.2096	Pin 1 to Pin 2	1.2098	√
2	1.2102	Pin 5 to Pin 6	1.2100	√
3	1.2095	Pin 9 to Pin 10	1.2098	√
4	1.2097	Pin 13 to Pin 14	1.2103	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.9609	Pin 3 to Pin 4	0.9606	√
2	0.9672	Pin 7 to Pin 8	0.9673	√
3	0.9649	Pin 11 to Pin 12	0.9647	√
4	0.9645	Pin 15 to Pin 16	0.9645	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.15		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.15		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.15		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.15		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.54		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.54		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.54		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.476		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.477		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.478		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.476		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.175		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.176		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.176		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.176		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.199		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.199		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.198		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.199		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	6 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	6 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	6 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	34 mV		33 to 45mV	-30dB to -27dB	√
Ch2	35 mV		33 to 45mV	-30dB to -27dB	√
Ch3	33 mV		33 to 45mV	-30dB to -27dB	√
Ch4	37 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.295		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.293		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

Unit……………………..PUM 8P
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	Yes

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.17v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.7 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.5 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.493	24.65 mA
Ch2	0.489	24.45 mA
Ch3	0.494	24.7 mA
Ch4	0.492	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.650	32.5 mA	>16mA	√
Ch2	0.649	32.45 mA	>16mA	√
Ch3	0.651	32.55 mA	>16mA	√
Ch4	0.649	32.45 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.746	37.3 mA	>16mA	√
Ch2	0.747	37.3 mA	>16mA	√
Ch3	0.745	37.2 mA	>16mA	√
Ch4	0.745	37.2 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.2 mA	>16mA	√
Ch2	0.746	37.3 mA	>16mA	√
Ch3	0.744	37.2 mA	>16mA	√
Ch4	0.744	37.2 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65
Ch2	0.192	9.60
Ch3	0.194	9.70
Ch4	0.193	9.65

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.418	20.90	>16mA	√
Ch2	0.417	20.85	>16mA	√
Ch3	0.420	21.00	>16mA	√
Ch4	0.417	20.85	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724	36.20	>16mA	√
Ch2	0.725	36.25	>16mA	√
Ch3	0.725	36.25	>16mA	√
Ch4	0.724	36.20	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744	37.20	>16mA	√
Ch2	0.745	37.25	>16mA	√
Ch3	0.743	37.15	>16mA	√
Ch4	0.743	37.15	>16mA	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.11	5.81	290 mA
Ch3	4.11	5.81	290 mA
Ch4	4.12	5.82	291 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.54	7.83	391 mA	>400mA	
Ch2	5.55	7.84	392 mA	>400mA	
Ch3	5.49	7.76	388 mA	>400mA	
Ch4	5.50	7.77	388 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.60	9.33	466 mA	>400mA	√
Ch2	6.58	9.30	465 mA	>400mA	√
Ch3	6.57	9.29	464 mA	>400mA	√
Ch4	6.57	9.28	464 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.62	9.36	468 mA	>400mA	√
Ch2	6.61	9.34	467 mA	>400mA	√
Ch3	6.62	9.36	468 mA	>400mA	√
Ch4	6.61	9.34	467 mA	>400mA	√

Unit……………………..PUM 8P
Test Engineer ………RMC
Date …………………14/12/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

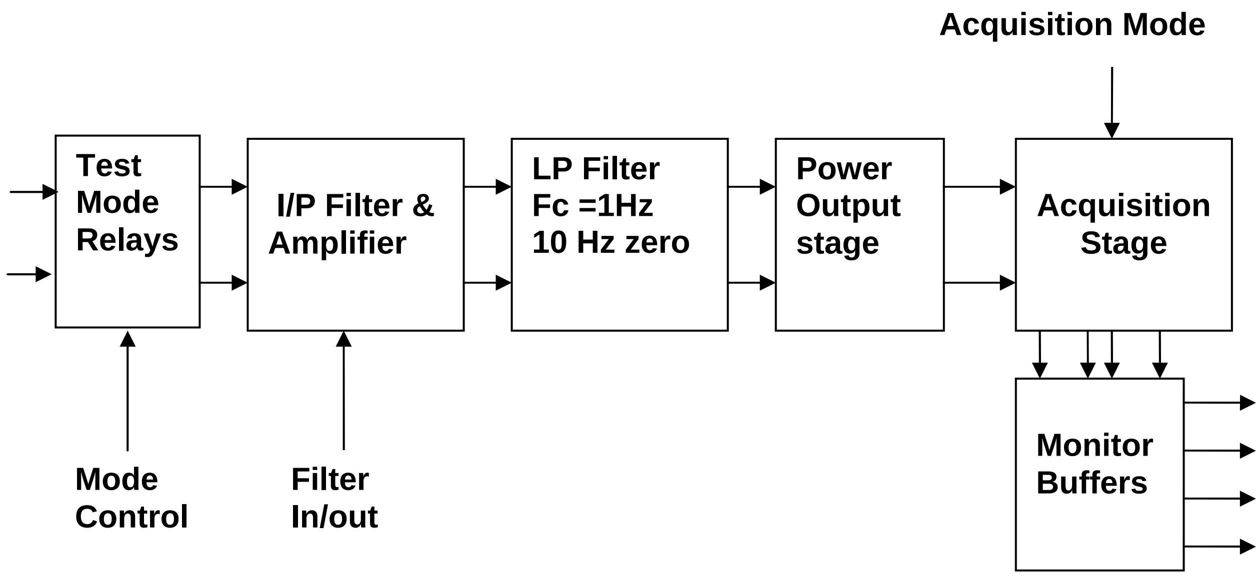
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM 9P
Test Engineer ……...RMC
Date ………………..20/12/10

Contents

1. Description

Block diagram



Description

Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

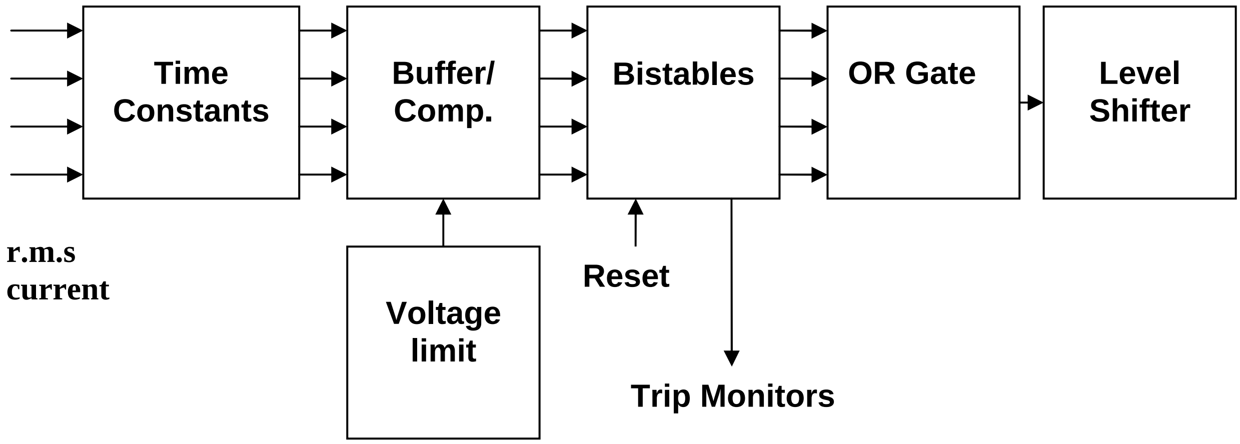
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

IC10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:
Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………PUM 9P
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

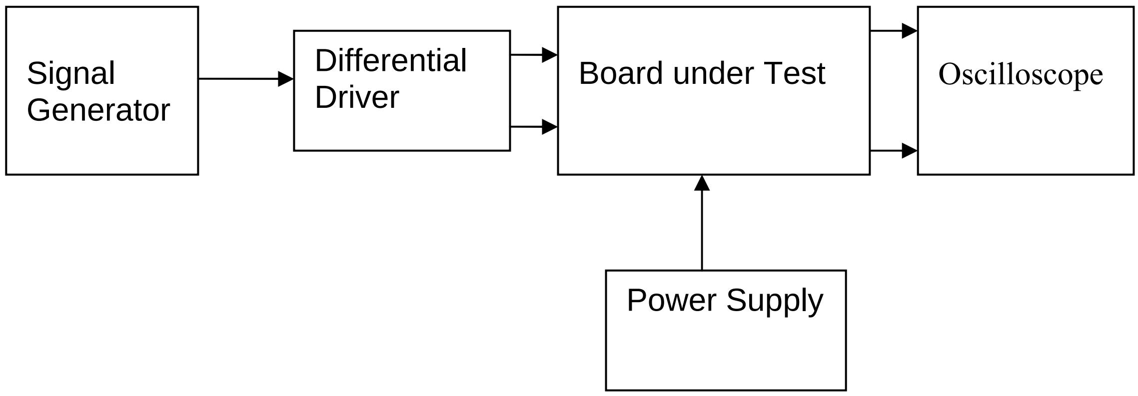
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.030v	√	1.2 mV
+15v TP4	14.968v	√	1.3 mV
-15v TP6	-15.107v	√	6 mV

All Outputs smooth DC, no oscillation?	**OK**

Record Power Supply Currents

Supply	**Current**
+16.5v	0.246 A
-16.5v	0.306 A

If the supplies are correct, proceed to the next test.

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Test Engineer ……...RMC
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM 9P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.199v	Pin 1 to Pin 2	1.198	√
2	1.200	Pin 5 to Pin 6	1.199	√
3	1.200	Pin 9 to Pin 10	1.198	√
4	1.200	Pin 13 to Pin 14	1.199	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.160	Pin 3 to Pin 4	1.161	√
2	1.160	Pin 7 to Pin 8	1.160	√
3	1.160	Pin 11 to Pin 12	1.160	√
4	1.161	Pin 15 to Pin 16	1.161	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.471		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.473		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.473		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.474		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.166		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.190		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.191		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.191		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.191		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	35 mV		33 to 45mV	-30dB to -27dB	√
Ch2	36 mV		33 to 45mV	-30dB to -27dB	√
Ch3	35 mV		33 to 45mV	-30dB to -27dB	√
Ch4	35 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.295		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.295		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.47		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.47		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.47		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.47		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.475		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM 9P
Test Engineer ……...RMC
Date ………………..20/12/10

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.18v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.7 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.484	24.2 mA
Ch2	0.493	24.6 mA
Ch3	0.495	24.7 mA
Ch4	0.489	24.4 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.644	32.2 mA	>16mA	√
Ch2	0.651	32.5 mA	>16mA	√
Ch3	0.651	32.5 mA	>16mA	√
Ch4	0.647	32.3 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.743	37.1 mA	>16mA	√
Ch2	0.746	37.3 mA	>16mA	√
Ch3	0.745	37.2 mA	>16mA	√
Ch4	0.743	37.1 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.743	37.15 mA	>16mA	√
Ch2	0.746	37.3 mA	>16mA	√
Ch3	0.744	37.2 mA	>16mA	√
Ch4	0.742	37.1 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.189	9.45
Ch2	0.194	9.7
Ch3	0.195	9.7
Ch4	0.192	9.6

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.413	20.65	**>16mA**	√
Ch2	0.412	20.6	**>16mA**	√
Ch3	0.412	20.6	**>16mA**	√
Ch4	0.417	20.85	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.722	36.1	**>16mA**	√
Ch2	0.725	36.25	**>16mA**	√
Ch3	0.724	36.2	**>16mA**	√
Ch4	0.722	36.1	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.741	36.0	**>16mA**	√
Ch2	0.745	37.25	**>16mA**	√
Ch3	0.743	37.15	**>16mA**	√
Ch4	0.741	36.0	**>16mA**	√

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12.3 Acquisition Mode
With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12	5.82	291 mA
Ch2	4.14	5.85	292 mA
Ch3	4.15	5.87	293 mA
Ch4	4.14	5.85	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.50	7.78	389 mA	>400mA	
Ch2	5.52	7.80	390 mA	>400mA	
Ch3	5.52	7.80	390 mA	>400mA	
Ch4	5.50	7.78	389 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.61	9.34	467 mA	>400mA	√
Ch2	6.61	9.34	467 mA	>400mA	√
Ch3	6.61	9.34	467 mA	>400mA	√
Ch4	6.58	9.30	465 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.63	9.37	468 mA	>400mA	√
Ch2	6.63	9.37	468 mA	>400mA	√
Ch3	6.62	9.36	468 mA	>400mA	√
Ch4	6.59	9.32	466 mA	>400mA	√

Unit…………………PUM 9P
Test Engineer ……...RMC
Date ………………..21/12/10

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

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PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

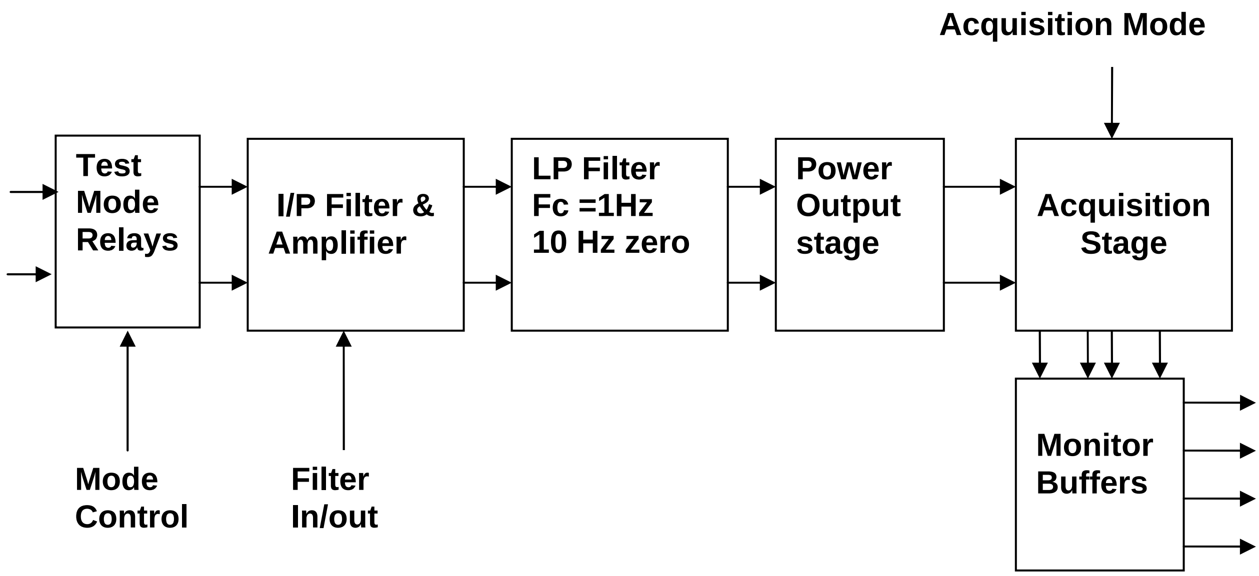
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM10P
Test Engineer ………RMC
Date ………………...22/12/10

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

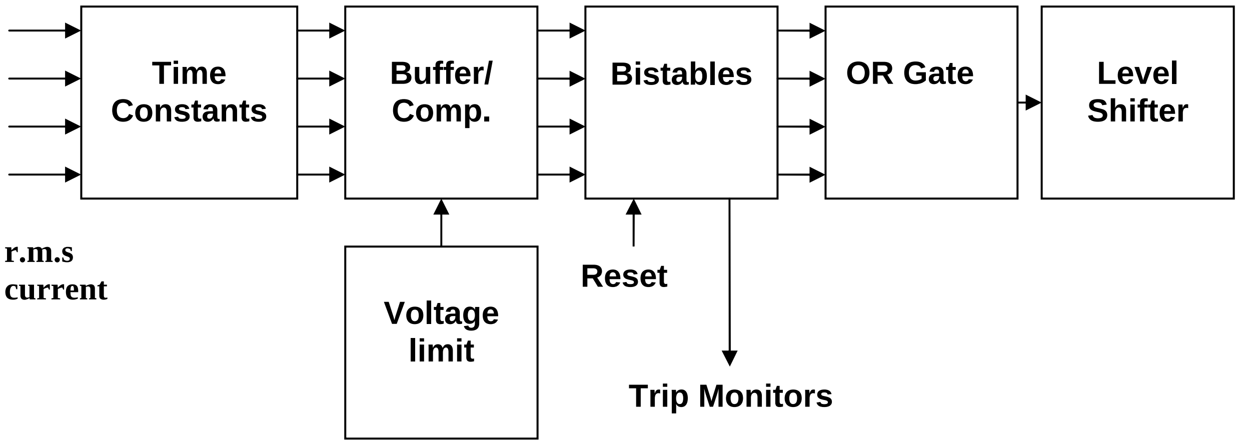
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

C10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………PUM10P
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

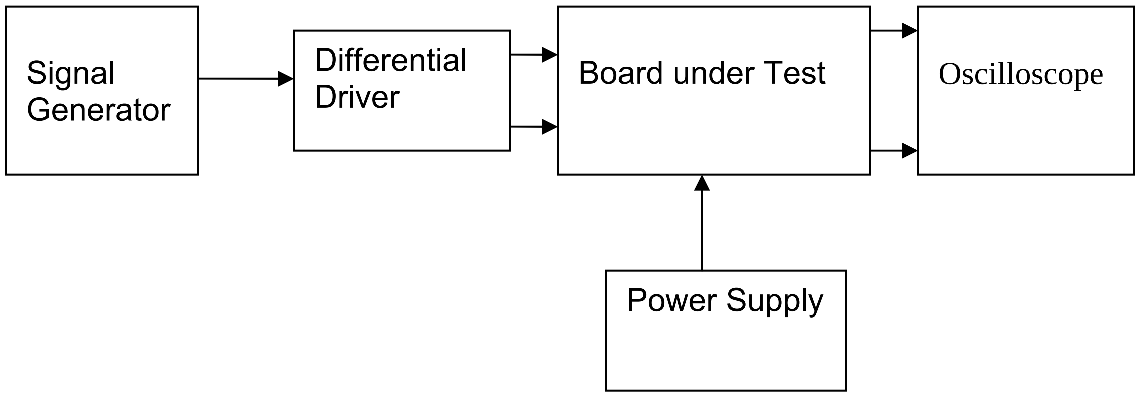
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.016v	√	1mV
+15v TP4	14.93v	√	1mV
-15v TP6	-14.89v	√	5mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.305 A
-16.5v	0.245 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM10P
Test Engineer ………RMC
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM10P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.20	Pin 1 to Pin 2	1.20	√
2	1.20	Pin 5 to Pin 6	1.20	√
3	1.20	Pin 9 to Pin 10	1.20	√
4	1.20	Pin 13 to Pin 14	1.20	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.16	Pin 3 to Pin 4	1.16	√
2	1.16	Pin 7 to Pin 8	1.16	√
3	1.16	Pin 11 to Pin 12	1.16	√
4	1.16	Pin 15 to Pin 16	1.16	√

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Test Engineer ………RMC
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.18v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.18v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.18v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.5v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.476		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.168		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.169		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.169		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.169		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.192		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.192		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.192		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.192		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	40		33 to 45mV	-30dB to -27dB	√
Ch2	40.2		33 to 45mV	-30dB to -27dB	√
Ch3	40.2		33 to 45mV	-30dB to -27dB	√
Ch4	40.2		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.295		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.295		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.295		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.474		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.475		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.475		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM10P
Test Engineer ………RMC
Date ………………....5/1/11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit…………………PUM10P
Test Engineer ………RMC
Date ………………....5/1/11

12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.192v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.3 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1 second

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.489	24.4 mA
Ch2	0.492	24.6 mA
Ch3	0.493	24.65 mA
Ch4	0.488	24.4 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.648	32.4 mA	>16mA	√
Ch2	0.651	32.5 mA	>16mA	√
Ch3	0.651	32.5 mA	>16mA	√
Ch4	0.647	32.3 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.25 mA	>16mA	√
Ch2	0.747	37.35 mA	>16mA	√
Ch3	0.747	37.35 mA	>16mA	√
Ch4	0.744	37.2 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.25 mA	>16mA	√
Ch2	0.746	37.3 mA	>16mA	√
Ch3	0.746	37.3 mA	>16mA	√
Ch4	0.743	37.1 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.192	9.6 mA
Ch2	0.194	9.7 mA
Ch3	0.194	9.7 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.417	20.85 mA	>16mA	√
Ch2	0.420	21.0 mA	>16mA	√
Ch3	0.420	21.0 mA	>16mA	√
Ch4	0.418	20.9 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724	37.7 mA	>16mA	√
Ch2	0.726	36.3 mA	>16mA	√
Ch3	0.725	36.25 mA	>16mA	√
Ch4	0.723	36.15 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.743	37.15 mA	>16mA	√
Ch2	0.745	37.25 mA	>16mA	√
Ch3	0.745	37.25 mA	>16mA	√
Ch4	0.742	37.1 mA	>16mA	√

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12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.13	5.84	292 mA
Ch2	4.15	5.86	293 mA
Ch3	4.16	5.88	294 mA
Ch4	4.14	5.85	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.52	7.80	390 mA	**>400mA**	
Ch2	5.53	7.82	391 mA	**>400mA**	
Ch3	5.54	7.83	391.5 mA	**>400mA**	
Ch4	5.52	7.80	390 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.61	9.34	467 mA	**>400mA**	√
Ch2	6.61	9.34	467 mA	**>400mA**	√
Ch3	6.63	9.37	468 mA	**>400mA**	√
Ch4	6.60	9.33	466 mA	**>400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.63	9.37	468 mA	**>400mA**	√
Ch2	6.64	9.39	469 mA	**>400mA**	√
Ch3	6.65	9.40	470 mA	**>400mA**	√
Ch4	6.63	9.33	466 mA	**>400mA**	√

Unit…………………PUM10P
Test Engineer ………RMC
Date ………………....5/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

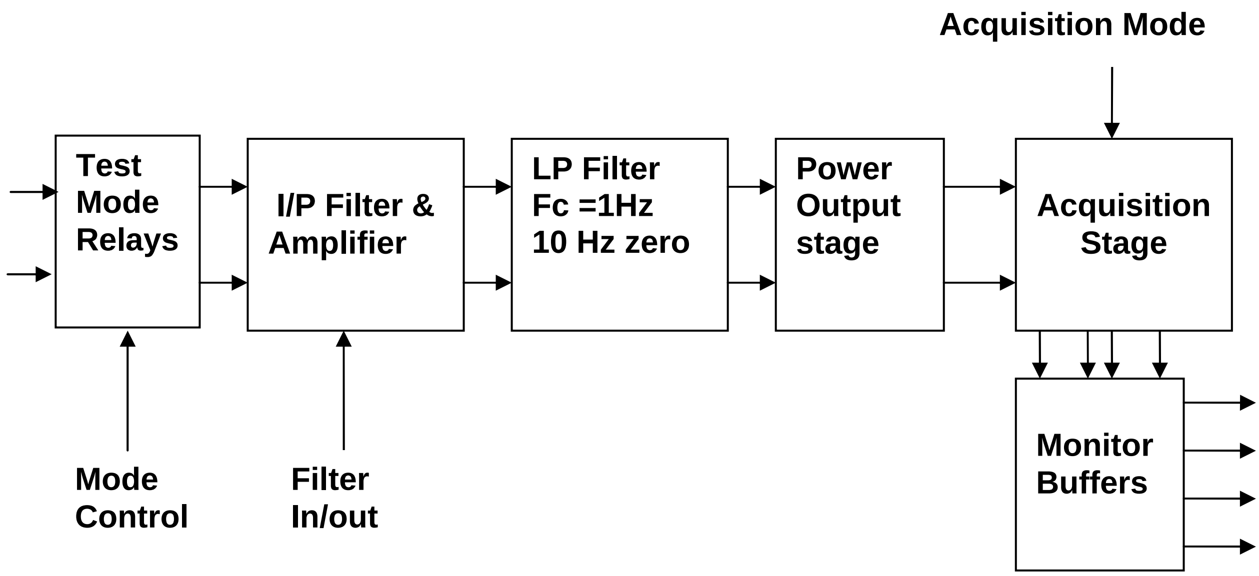
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM11P
Test Engineer ………RMC
Date ………………....5/1/11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

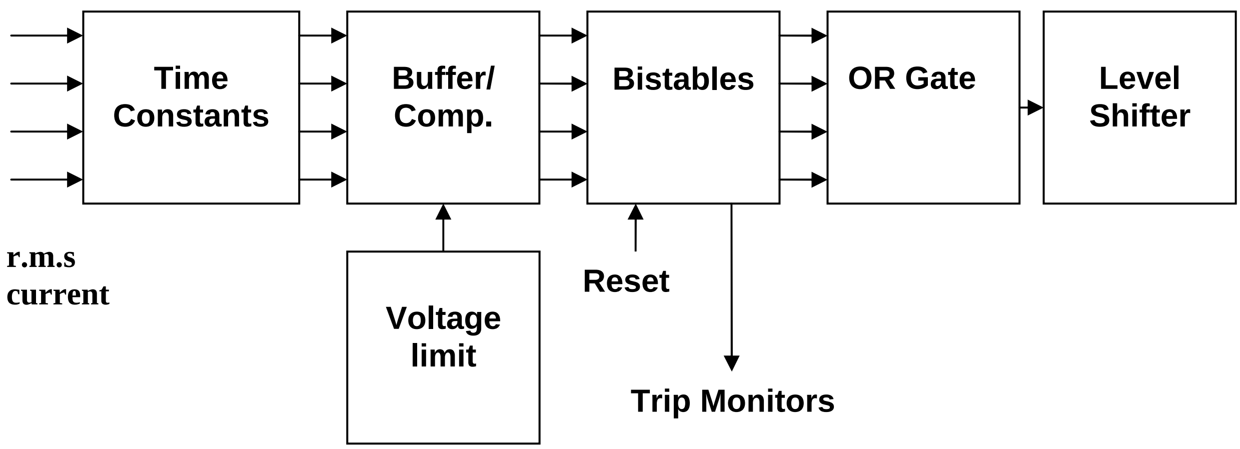
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit…………………PUM11P
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

Unit…………………PUM11P
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

C10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………PUM11P
Test Engineer ………RMC
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

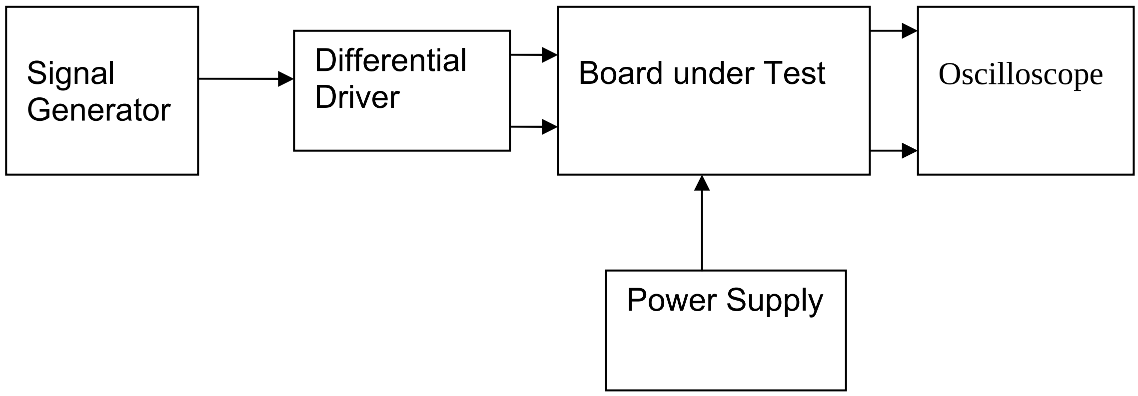
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM11P
Test Engineer ………RMC
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.037v	√	1mv pk/pk
+15v TP4	14.93v	√	1mv pk/pk
-15v TP6	-15.07v	√	1mv pk/pk

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.309A
-16.5v	0.247A

If the supplies are correct, proceed to the next test.

Unit…………………PUM11P
Test Engineer ………RMC
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM11P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.21v	Pin 1 to Pin 2	1.21v	√
2	1.21v	Pin 5 to Pin 6	1.21v	√
3	1.21v	Pin 9 to Pin 10	1.21v	√
4	1.21v	Pin 13 to Pin 14	1.21v	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.975v	Pin 3 to Pin 4	0.974v	√
2	0.972v	Pin 7 to Pin 8	0.972v	√
3	0.976v	Pin 11 to Pin 12	0.976v	√
4	0.972v	Pin 15 to Pin 16	0.972v	√

Unit…………………PUM11P
Test Engineer ………RMC
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.05v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.15v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.55v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.54v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.54v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.53v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.473		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.477		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.17		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.193		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.193		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.193		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.1929		1.0 to 1.3v	0.5 to 2.5dB	√

Unit…………………PUM11P
Test Engineer ………RMC
Date ………………....5/1/11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.4 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	7 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	40		33 to 45mV	-30dB to -27dB	√
Ch2	40		33 to 45mV	-30dB to -27dB	√
Ch3	39.6		33 to 45mV	-30dB to -27dB	√
Ch4	39.8		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.294		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.474		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.463		0.47 to 0.49V	-7dB to -6dB	

Unit…………………PUM11P
Test Engineer ………RMC
Date ………………....5/1/11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit…………………PUM11P
Test Engineer ………RMC
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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.16v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.3 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

Unit…………………PUM11P
Test Engineer ………RMC
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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494 v	24.7 mA
Ch2	0.492 v	24.6 mA
Ch3	0.493 v	24.65 mA
Ch4	0.488 v	24.4 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.651 v	32.55 mA	>16mA	
Ch2	0.650 v	32.5 mA	>16mA	
Ch3	0.652 v	32.6 mA	>16mA	
Ch4	0.657 v	32.8 mA	>16mA	

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745 v	37.25 mA	>16mA	√
Ch2	0.746 v	37.3 mA	>16mA	√
Ch3	0.746 v	37.3 mA	>16mA	√
Ch4	0.743 v	37.1 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744 v	37.2 mA	>16mA	√
Ch2	0.745 v	37.25 mA	>16mA	√
Ch3	0.746 v	37.3 mA	>16mA	√
Ch4	0.742 v	37.1 mA	>16mA	√

Unit…………………PUM11P
Test Engineer ………RMC
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193 v	9.65 mA
Ch2	0.193 v	9.65 mA
Ch3	0.194 v	9.70 mA
Ch4	0.189 v	9.45 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.418 v	20.9 mA	>16mA	√
Ch2	0.419 v	20.95 mA	>16mA	√
Ch3	0.420 v	21.00 mA	>16mA	√
Ch4	0.412 v	20.6 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724 v	36.2 mA	>16mA	√
Ch2	0.725 v	36.2 mA	>16mA	√
Ch3	0.725 v	36.2 mA	>16mA	√
Ch4	0.722 v	36.1 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744 v	37.2 mA	>16mA	√
Ch2	0.744 v	37.2 mA	>16mA	√
Ch3	0.745 v	37.2 mA	>16mA	√
Ch4	0.742 v	37.1 mA	>16mA	√

Unit…………………PUM11P
Test Engineer ………RMC
Date ………………....6/1/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12 v	5.82 v	291 mA
Ch2	4.14 v	5.85 v	290 mA
Ch3	4.11 v	5.81 v	290 mA
Ch4	4.14 v	5.85 v	290 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.50 v	7.78 v	389 mA	>400mA	
Ch2	5.52 v	7.80 v	390.3 mA	>400mA	
Ch3	5.50 v	7.78 v	389 mA	>400mA	
Ch4	5.52 v	7.80 v	390.3 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.62 v	9.36 v	468 mA	>400mA	√
Ch2	6.62 v	9.36 v	468 mA	>400mA	√
Ch3	6.61 v	9.34 v	467 mA	>400mA	√
Ch4	6.60 v	9.33 v	466 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.64 v	9.39 v	469 mA	>400mA	√
Ch2	6.64 v	9.39 v	469 mA	>400mA	√
Ch3	6.64 v	9.39 v	469 mA	>400mA	√
Ch4	6.62 v	9.36 v	468 mA	>400mA	√

Unit…………………PUM11P
Test Engineer ………RMC
Date ………………....6/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

Residual 2 mV at 100 kHz – possibly pick up.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

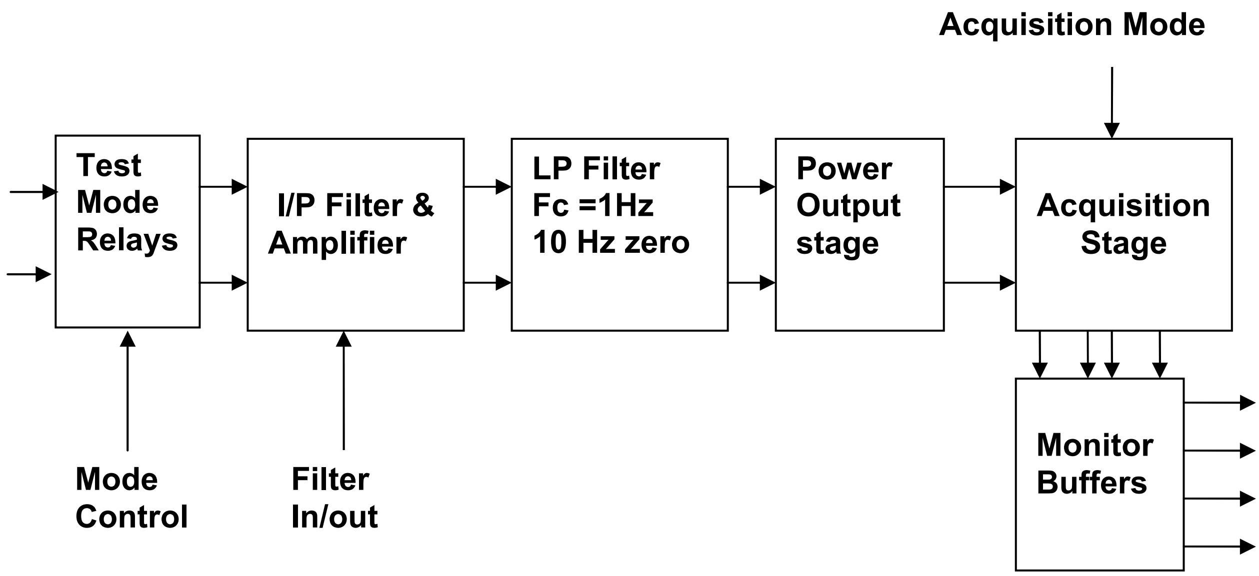
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

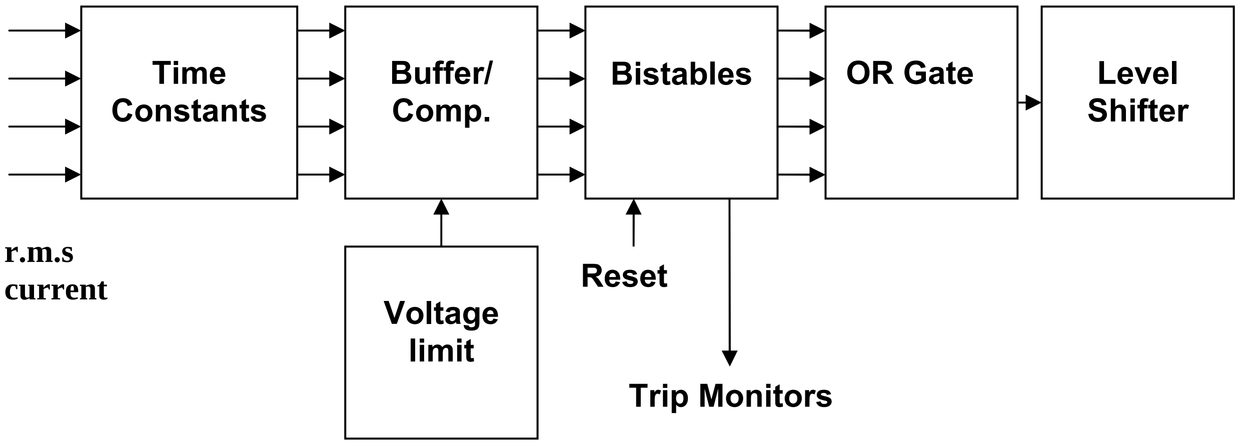
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit…………………PUM12P
Test Engineer ………RMC
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Power supply	TTI	EL302RD	
Power supply	Farnell	LT30-1	
Oscilloscope	Tektronix	2225	
Function Generator	Agient	33250A	

Unit…………………PUM12P
Test Engineer ………RMC
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3. Inspection

Workmanship
Inspect the general workmanship standard and comment:

OK

C10 and IC11 Changed to AD8671 on all channels.

RESET PULSE MOD
J7/2 Connected to J7/18 on 10/1/11

Links:
Check that the link W4 is present on each channel.

Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit…………………PUM12P
Test Engineer ………RMC
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

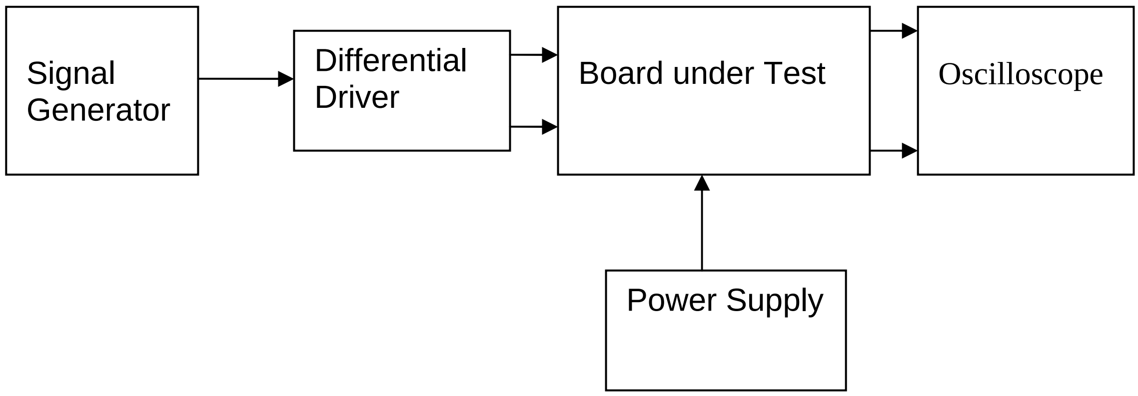
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM12P
Test Engineer ………RMC
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.04 v	√	1 mV
+15v TP4	14.9 v	√	1 mV
-15v TP6	-15.1 v	√	5 mV

All Outputs smooth DC, no oscillation?	√

Note – all noise measurements were made differentially wrt 0v as excessive common mode pick up was present, even when everything was switched off.

Record Power Supply Currents

Supply	**Current**
+16.5v	0.43 A
-16.5v	0.23 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM12P
Test Engineer ………RMC
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.20 v	Pin 1 to Pin 2	1.20 v	√
2	1.20 v	Pin 5 to Pin 6	1.20 v	√
3	1.20 v	Pin 9 to Pin 10	1.20 v	√
4	1.20 v	Pin 13 to Pin 14	1.20 v	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.968 v	Pin 3 to Pin 4	0.968 v	√
2	0.965 v	Pin 7 to Pin 8	0.965 v	√
3	0.968 v	Pin 11 to Pin 12	0.968 v	√
4	0.969 v	Pin 15 to Pin 16	0.969 v	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2 v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2 v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.17 v		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2 v		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5 v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5 v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5 v		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.5 v		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.129		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.470		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.477		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.479		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.166		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.166		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.167		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.167		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.189		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.190		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.189		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.190		1.0 to 1.3v	0.5 to 2.5dB	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	6 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.5 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	39 mV		33 to 45mV	-30dB to -27dB	√
Ch2	39 mV		33 to 45mV	-30dB to -27dB	√
Ch3	39 mV		33 to 45mV	-30dB to -27dB	√
Ch4	39 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.290		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.290		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.470		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.470		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………....6/1/11

12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.18v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.2 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………...6/1/11

12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.491	24.55 mA
Ch2	0.490	24.5 mA
Ch3	0.493	24.65 mA
Ch4	0.488	24.4 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.649	32.45 mA	>16mA	√
Ch2	0.649	32.45 mA	>16mA	√
Ch3	0.650	32.5 mA	>16mA	√
Ch4	0.646	32.3 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.745	37.25 mA	>16mA	√
Ch2	0.746	37.3 mA	>16mA	√
Ch3	0.745	37.25 mA	>16mA	√
Ch4	0.743	37.15 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.744	37.2 mA	>16mA	√
Ch2	0.745	37.25 mA	>16mA	√
Ch3	0.744	37.2 mA	>16mA	√
Ch4	0.743	37.15 mA	>16mA	√

Unit…………………PUM12P
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.191	9.55 mA
Ch3	0.195	9.75 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.418	20.9 mA	**>16mA**	√
Ch2	0.415	20.75 mA	**>16mA**	√
Ch3	0.421	21.5 mA	**>16mA**	√
Ch4	0.419	20.95 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724	36.2 mA	**>16mA**	√
Ch2	0.724	36.2 mA	**>16mA**	√
Ch3	0.724	36.2 mA	**>16mA**	√
Ch4	0.723	36.15 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.743	37.15 mA	**>16mA**	√
Ch2	0.744	37.2 mA	**>16mA**	√
Ch3	0.743	37.15 mA	**>16mA**	√
Ch4	0.742	37.1 mA	**>16mA**	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………....6/1/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.09	5.78	289 mA
Ch2	4.13	5.84	292 mA
Ch3	4.11	5.81	290 mA
Ch4	4.09	5.78	289 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.49	7.76	388 mA	>400mA	
Ch2	5.52	7.80	390.3 mA	>400mA	
Ch3	5.50	7.77	388 mA	>400mA	
Ch4	5.49	7.76	388 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.60	9.33	466 mA	>400mA	√
Ch2	6.58	9.30	465 mA	>400mA	√
Ch3	6.62	9.36	468 mA	>400mA	√
Ch4	6.60	9.33	466 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.63	9.37	468 mA	>400mA	√
Ch2	6.63	9.37	468 mA	>400mA	√
Ch3	6.64	9.39	469 mA	>400mA	√
Ch4	6.53	9.23	461 mA	>400mA	√

Unit…………………PUM12P
Test Engineer ………RMC
Date ………………....6/1/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**
	PUM Driver Board Test Report	
	R. M. Cutler, University of Birmingham	

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

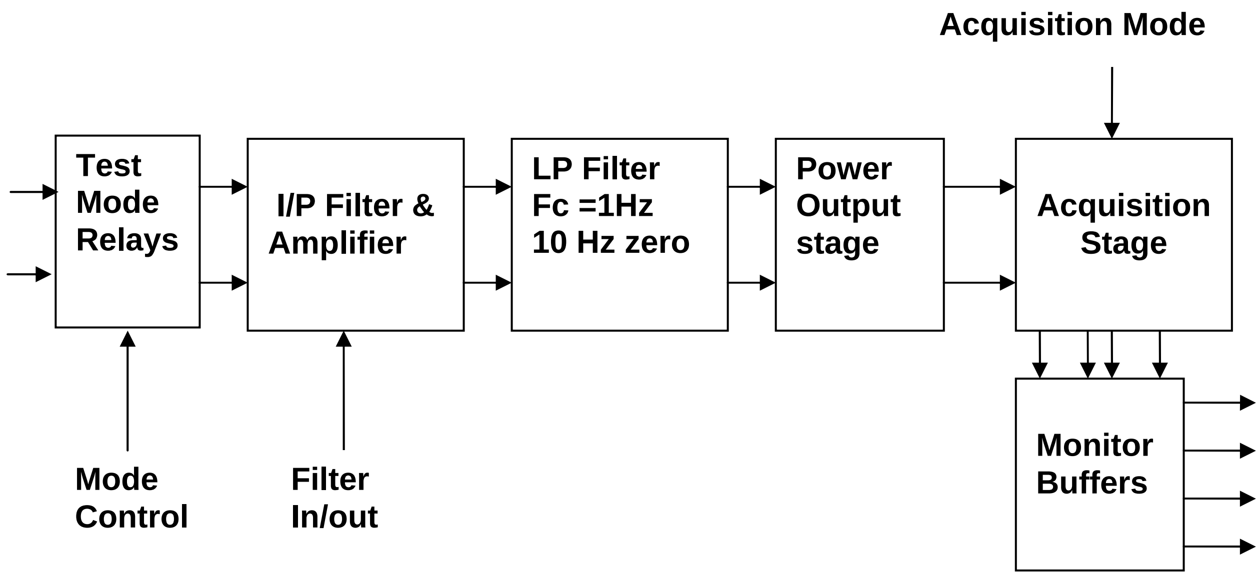
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………31/1/11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

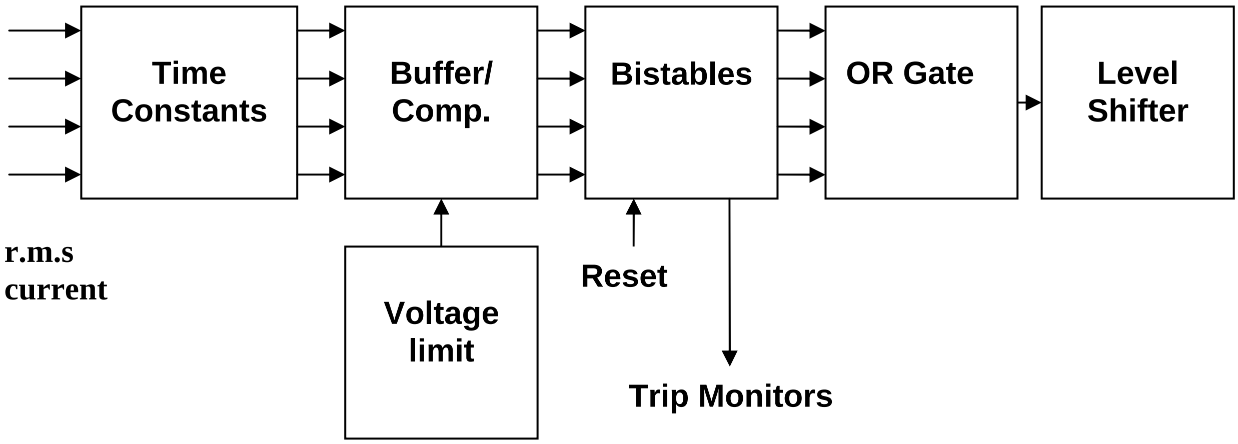
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………31/1/11

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit…………………PUM13P
Test Engineer …….....RMC
Date …………………31/1/11

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Reset pulse wire link added between pin 2 and pin 18 on J7

IC14, ch1 & IC14 ch2 changed

IC7 Ch1 changed

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

Unit.....................PUM13P
Test Engineer ....RMC
Date 31/1/11

4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

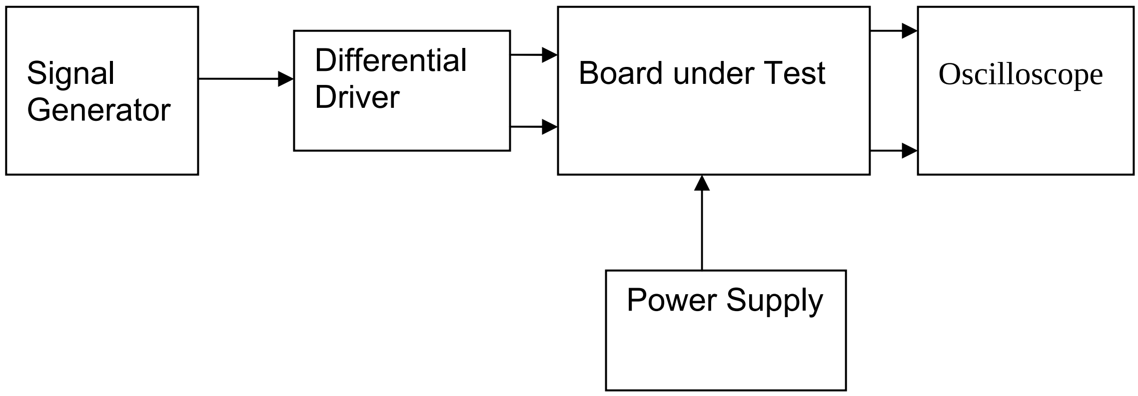
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………31/1/11

6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	+12.04 v	√	2 mV
+15v TP4	+14.79 v	√	2 mV
-15v TP6	-15.08 v	√	6 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.293 A
-16.5v	0.232 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………31/1/11

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………31/1/11

8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.201	Pin 1 to Pin 2	1.200	√
2	1.201	Pin 5 to Pin 6	1.201	√
3	1.201	Pin 9 to Pin 10	1.200	√
4	1.200	Pin 13 to Pin 14	1.200	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.965	Pin 3 to Pin 4	0.966	√
2	0.969	Pin 7 to Pin 8	0.969	√
3	0.965	Pin 11 to Pin 12	0.965	√
4	0.967	Pin 15 to Pin 16	0.967	√

Unit…………………PUM13P
Test Engineer ....RMC
Date …………………31/1/11

9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch2	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch3	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch4	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.51		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch2	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch3	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch4	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch2	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch3	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch4	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.47		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch2	0.47		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch3	0.47		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch4	0.47		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.16		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch2	1.16		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch3	1.16		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch4	1.16		**1.0 to 1.28v**	**0.34 to 2.34dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch2	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch3	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch4	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………1/2/11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	7.0 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	7.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	7.0 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	8.0 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	8.0 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	8.0 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.035		33 to 45mV	-30dB to -27dB	√
Ch2	0.035		33 to 45mV	-30dB to -27dB	√
Ch3	0.035		33 to 45mV	-30dB to -27dB	√
Ch4	0.036		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.291		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.471		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.471		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………17/2/11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Channel 1 was initially distorted. Ch 1 IC 7 was replaced, which solved this problem.

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………17/2/11

12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.172 v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	3.2 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………17/2/11

12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494	24.7 mA
Ch2	0.494	24.7 mA
Ch3	0.497	24.8 mA
Ch4	0.501	25.0 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.65 mA	>16mA	√
Ch2	0.654	32.70 mA	>16mA	√
Ch3	0.656	32.80 mA	>16mA	√
Ch4	0.658	32.90 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.752	37.6 mA	>16mA	√
Ch3	0.752	37.6 mA	>16mA	√
Ch4	0.752	37.6 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.752	37.6 mA	>16mA	√
Ch3	0.752	37.6 mA	>16mA	√
Ch4	0.751	37.5 mA	>16mA	√

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………17/2/11

12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.194	9.7 mA
Ch3	0.195	9.75 mA
Ch4	0.197	9,85 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.420	21.0 mA	**>16mA**	√
Ch2	0.421	21.0 mA	**>16mA**	√
Ch3	0.421	21.0 mA	**>16mA**	√
Ch4	0.424	21.2 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**>16mA**	√
Ch2	0.731	36.5 mA	**>16mA**	√
Ch3	0.730	36.5 mA	**>16mA**	√
Ch4	0.731	36.5 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	**>16mA**	√
Ch2	0.750	37.5 mA	**>16mA**	√
Ch3	0.750	37.5 mA	**>16mA**	√
Ch4	0.750	37.5 mA	**>16mA**	√

Unit…………………PUM13P
Test Engineer ……....RMC
Date …………………17/2/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.15	5.86	293 mA
Ch2	4.14	5.85	292 mA
Ch3	4.16	5.88	294 mA
Ch4	4.13	5.84	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.55	7.84	392 mA	>400mA	
Ch2	5.56	7.86	393 mA	>400mA	
Ch3	5.57	7.87	394 mA	>400mA	
Ch4	5.54	7.83	391 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	>400mA	√
Ch2	6.70	9.47	473 mA	>400mA	√
Ch3	6.68	9.44	472 mA	>400mA	√
Ch4	6.67	9.43	471 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	>400mA	√
Ch2	6.73	9.51	475 mA	>400mA	√
Ch3	6.71	9.49	474 mA	>400mA	√
Ch4	6.70	9.47	473 mA	>400mA	√

Unit…………………PUM13P
Test Engineer ……....RMC
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

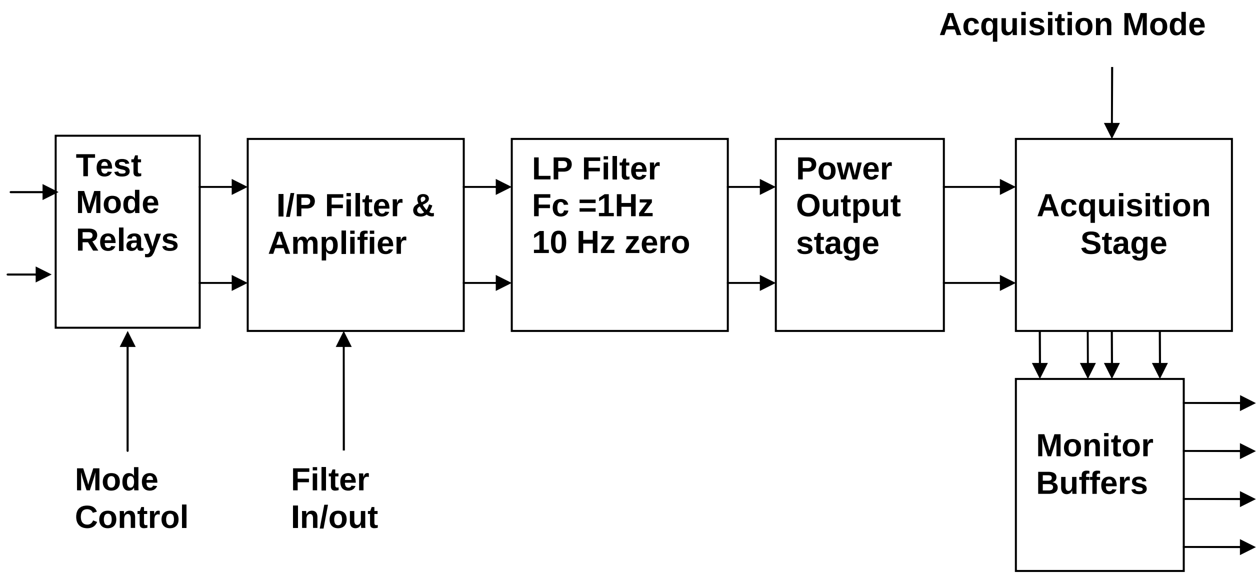
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM14P
Test Engineer ………RMC
Date …………………1/2/11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

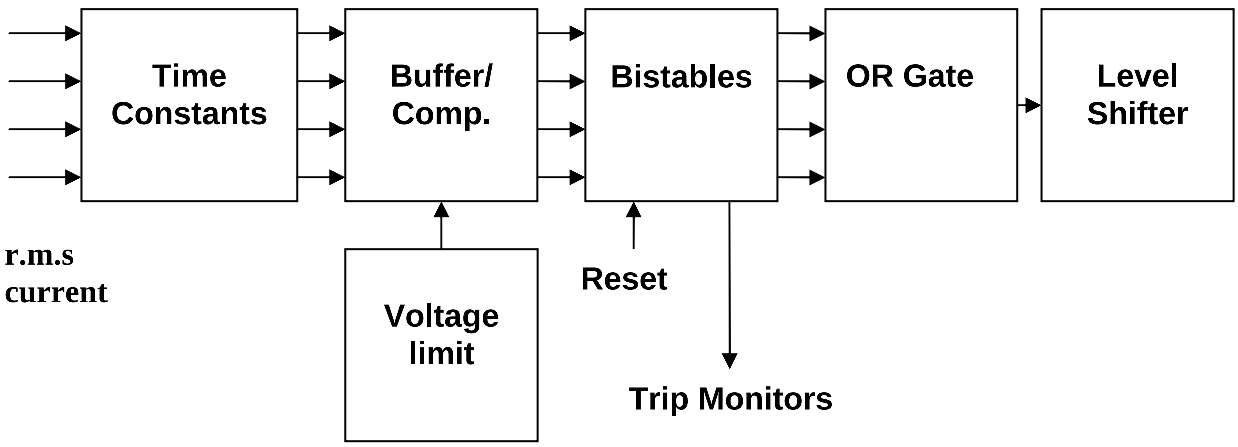
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

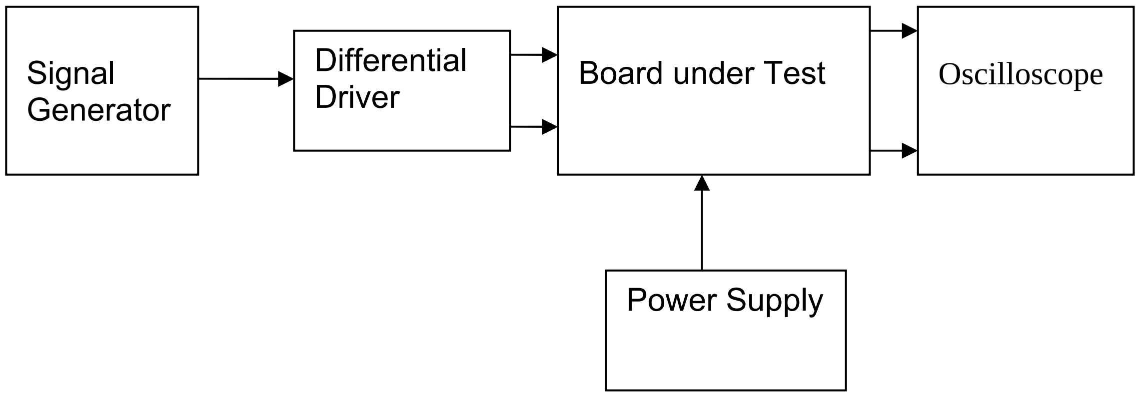
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM14P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	+12.048	√	2 mV
+15v TP4	+14.935	√	2 mV
-15v TP6	-15.017	√	6 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.309 A
-16.5v	0.248 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM14P
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM14P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.20	Pin 1 to Pin 2	1.20	√
2	1.20	Pin 5 to Pin 6	1.20	√
3	1.20	Pin 9 to Pin 10	1.20	√
4	1.20	Pin 13 to Pin 14	1.20	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.966	Pin 3 to Pin 4	0.965	√
2	0.966	Pin 7 to Pin 8	0.965	√
3	0.967	Pin 11 to Pin 12	0.966	√
4	0.963	Pin 15 to Pin 16	0.962	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.13		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch2	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch3	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch4	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.48		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch2	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch3	0.59		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch4	0.53		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch2	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch3	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch4	0.13		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.473		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch2	0.473		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch3	0.472		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch4	0.473		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.166		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch2	1.166		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch3	1.165		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch4	1.166		**1.0 to 1.28v**	**0.34 to 2.34dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch2	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch3	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch4	1.19		**1.0 to 1.3v**	**0.5 to 2.5dB**	√

Unit…………………PUM14P
Test Engineer ………RMC
Date …………………1/2/11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.6 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	5.3 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	5 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	5.3 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	37 mV		33 to 45mV	-30dB to -27dB	√
Ch2	37 mV		33 to 45mV	-30dB to -27dB	√
Ch3	36 mV		33 to 45mV	-30dB to -27dB	√
Ch4	35 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.283		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.295		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.473		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.473		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM14P
Test Engineer ………RMC
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.185v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

Unit…………………PUM14P
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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.495	24.75 mA
Ch2	0.499	24.95 mA
Ch3	0.502	25.10 mA
Ch4	0.496	24.80 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654	32.7 mA	>16mA	√
Ch2	0.657	32.8 mA	>16mA	√
Ch3	0.658	32.9 mA	>16mA	√
Ch4	0.655	32.75 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	>16mA	√
Ch2	0.75	37.5 mA	>16mA	√
Ch3	0.75	37.5 mA	>16mA	√
Ch4	0.75	37.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	>16mA	√
Ch2	0.75	37.5 mA	>16mA	√
Ch3	0.75	37.5 mA	>16mA	√
Ch4	0.75	37.5 mA	>16mA	√

Unit…………………PUM14P
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195	9.75 mA
Ch2	0.196	9.80 mA
Ch3	0.197	9.85 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.42	21 mA	>16mA	√
Ch2	0.42	21 mA	>16mA	√
Ch3	0.42	21 mA	>16mA	√
Ch4	0.42	21 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.73	36.5 mA	>16mA	√
Ch2	0.73	36.5 mA	>16mA	√
Ch3	0.73	36.5 mA	>16mA	√
Ch4	0.73	36.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	>16mA	√
Ch2	0.75	37.5 mA	>16mA	√
Ch3	0.75	37.5 mA	>16mA	√
Ch4	0.75	37.5 mA	>16mA	√

Unit…………………PUM14P
Test Engineer ………RMC
Date …………………1/2/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.17	5.89	294 mA
Ch2	4.18	5.91	295 mA
Ch3	4.16	5.88	294 mA
Ch4	4.20	5.94	297 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.58	7.89	394 mA	**>400mA**	
Ch2	5.58	7.89	394 mA	**>400mA**	
Ch3	5.57	7.87	393 mA	**>400mA**	
Ch4	5.60	7.92	396 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	**>400mA**	√
Ch2	6.70	9.47	473 mA	**>400mA**	√
Ch3	6.70	9.47	473 mA	**>400mA**	√
Ch4	6.69	9.46	473 mA	**>400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.71	9.49	474 mA	**>400mA**	√
Ch2	6.72	9.5	475 mA	**>400mA**	√
Ch3	6.72	9.5	475 mA	**>400mA**	√
Ch4	6.72	9.5	475 mA	**>400mA**	√

Unit…………………PUM14P
Test Engineer ………RMC
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

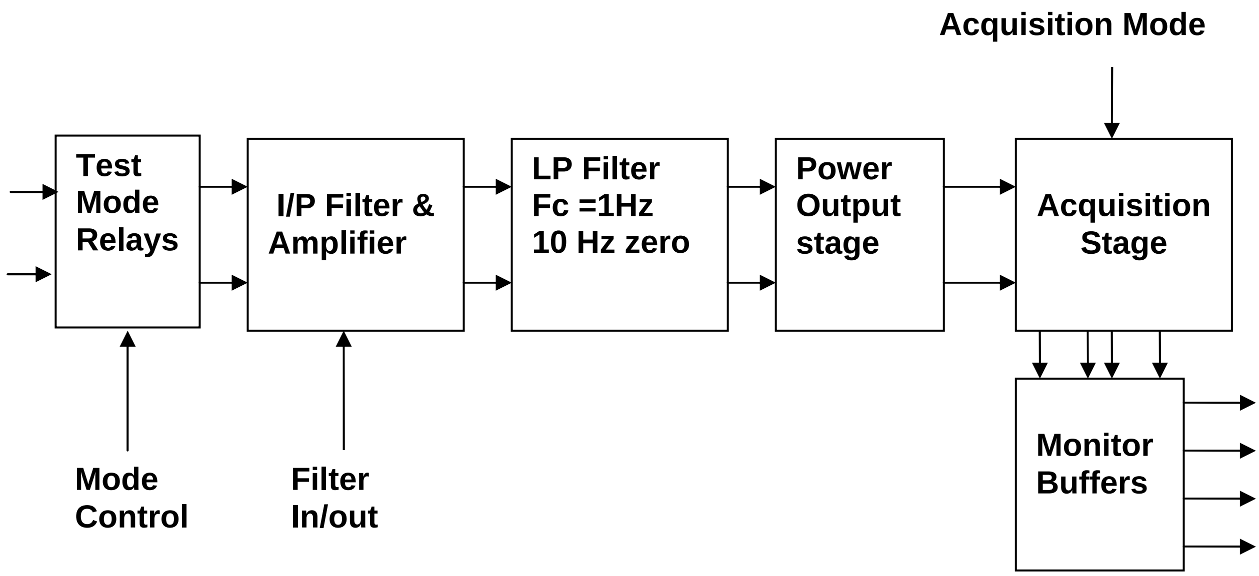
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit…………………PUM15P
Test Engineer ………RMC
Date ………………...1/2/11

Contents

1. Description

Block diagram



Description

Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

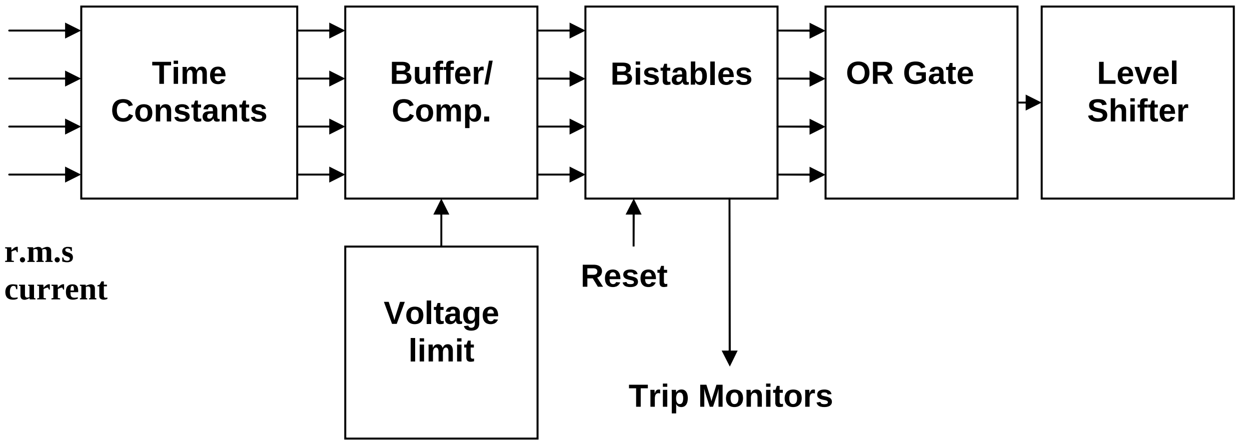
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK
Wire added to ink J7 pin 2 to the reset pulse

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

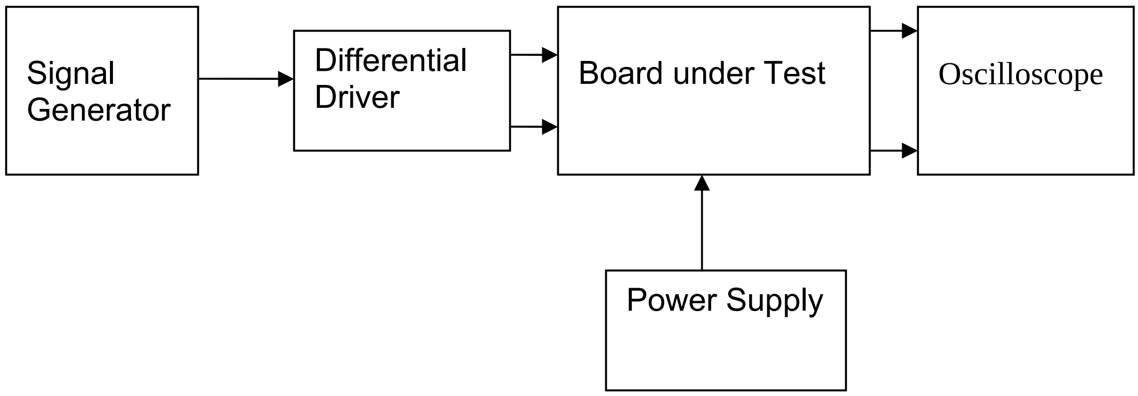
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit…………………PUM15P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	+12.002	√	2 mV
+15v TP4	+14.935	√	2 mV
-15v TP6	-15.016	√	6 mV

All Outputs smooth DC, no oscillation?	√

Some pick up present on all regulators: 15 MHz, 2 mV

Record Power Supply Currents

Supply	**Current**
+16.5v	0.301 A
-16.5v	0.240 A

If the supplies are correct, proceed to the next test.

Unit…………………PUM15P
Test Engineer ………RMC
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit…………………PUM15P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.201	Pin 1 to Pin 2	1.201	√
2	1.201	Pin 5 to Pin 6	1.201	√
3	1.201	Pin 9 to Pin 10	1.201	√
4	1.201	Pin 13 to Pin 14	1.201	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.969	Pin 3 to Pin 4	0.968	√
2	0.965	Pin 7 to Pin 8	0.966	√
3	0.968	Pin 11 to Pin 12	0.968	√
4	0.970	Pin 15 to Pin 16	0.970	√

Unit…………………PUM15P
Test Engineer ………RMC
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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.13		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch2	1.13		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch3	1.16		**1.0 to 1.3v**	**0.4 to 2.4dB**	√
Ch4	1.13√		**1.0 to 1.3v**	**0.4 to 2.4dB**	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch2	0.49		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch3	0.53		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√
Ch4	0.53		**0.48 to 0.6v**	**-6.5 to -4.5dB**	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.134		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch2	0.135		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch3	0.134		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√
Ch4	0.134		**0.12 to 0.15v**	**-16.5 to -18.5dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.479		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch2	0.481		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch3	0.477		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√
Ch4	0.479		**0.42 to 0.52v**	**-5.5 to -7.5dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.17		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch2	1.17		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch3	1.17		**1.0 to 1.28v**	**0.34 to 2.34dB**	√
Ch4	1.17		**1.0 to 1.28v**	**0.34 to 2.34dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch2	1.2		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch3	1.2		**1.0 to 1.3v**	**0.5 to 2.5dB**	√
Ch4	1.2		**1.0 to 1.3v**	**0.5 to 2.5dB**	√

Unit…………………PUM15P
Test Engineer ………RMC
Date ………………...2/2/11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.3 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.3 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6.3 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.3 mV		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.3 mV		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	37 mV		33 to 45mV	-30dB to -27dB	√
Ch2	36 mV		33 to 45mV	-30dB to -27dB	√
Ch3	37 mV		33 to 45mV	-30dB to -27dB	√
Ch4	35 mV		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.282		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.475		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.476		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.476		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.476		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.476		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.477		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.477		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.477		0.47 to 0.49V	-7dB to -6dB	√

Unit…………………PUM15P
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit…………………PUM15P
Test Engineer ………RMC
Date ………………...2/2/11

12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.118 v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.3 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.2 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.503	25.1 mA
Ch2	0.498	24.9 mA
Ch3	0.493	24.6 mA
Ch4	0.493	24.6 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.658	32.6 mA	>16mA	√
Ch2	0.656	32.8 mA	>16mA	√
Ch3	0.653	31.7 mA	>16mA	√
Ch4	0.653	31.7 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.750	37.5 mA	>16mA	√
Ch4	0.751	37.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.750	37.5 mA	>16mA	√
Ch4	0.751	37.5 mA	>16mA	√

Unit…………………PUM15P
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.198	9.45 mA
Ch2	0.197	9.85 mA
Ch3	0.194	9.70 mA
Ch4	0.194	9.70 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.425	21.25 mA	**>16mA**	√
Ch2	0.424	21.20 mA	**>16mA**	√
Ch3	0.420	21.00 mA	**>16mA**	√
Ch4	0.421	21.05 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	**>16mA**	√
Ch2	0.729	36.45 mA	**>16mA**	√
Ch3	0.730	36.50 mA	**>16mA**	√
Ch4	0.730	36.50 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749	37.45 mA	**>16mA**	√
Ch2	0.748	37.40 mA	**>16mA**	√
Ch3	0.749	37.45 mA	**>16mA**	√
Ch4	0.750	37.50 mA	**>16mA**	√

Unit…………………PUM15P
Test Engineer ………RMC
Date ………………...2/2/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**
Ch1	4.12	5.83	291 mA
Ch2	4.15	5.87	293 mA
Ch3	4.15	5.87	293 mA
Ch4	4.11	5.81	290 mA

200Hz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	5.53	7.82	391 mA	**>400mA**	
Ch2	5.55	7.85	392 mA	**>400mA**	
Ch3	5.56	7.86	393 mA	**>400mA**	
Ch4	5.53	7.82	391 mA	**>400mA**	

1 KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	6.67	9.43	471 mA	**>400mA**	√
Ch2	6.68	9.44	472 mA	**>400mA**	√
Ch3	6.68	9.44	472 mA	**>400mA**	√
Ch4	6.67	9.43	471 mA	**>400mA**	√

5 KHz

	Vo r.m.s	**Vo pk.**	**Io pk. (Vo/20)**	**Specification**	**Pass/Fail**
Ch1	6.70	9.47	473 mA	**>400mA**	√
Ch2	6.71	9.49	474 mA	**>400mA**	√
Ch3	6.71	9.49	474 mA	**>400mA**	√
Ch4	6.71	9.49	474 mA	**>400mA**	√

Unit…………………PUM15P
Test Engineer ………RMC
Date ………………...2/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

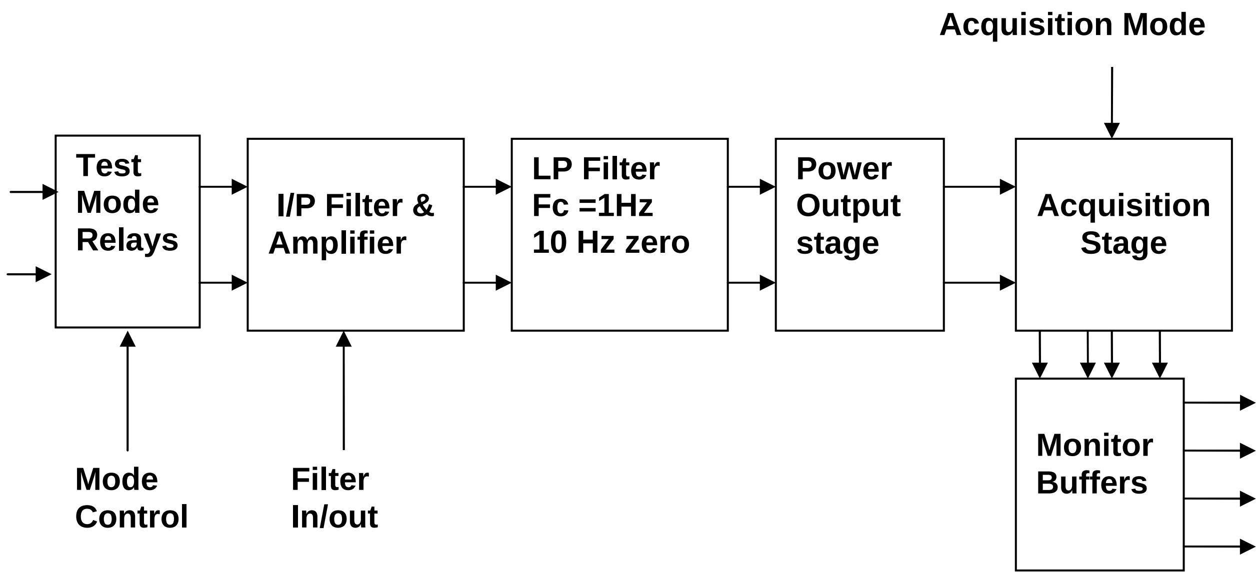
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM16P
Test Engineer ………...RMC
Date …………………..7/2/2011

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

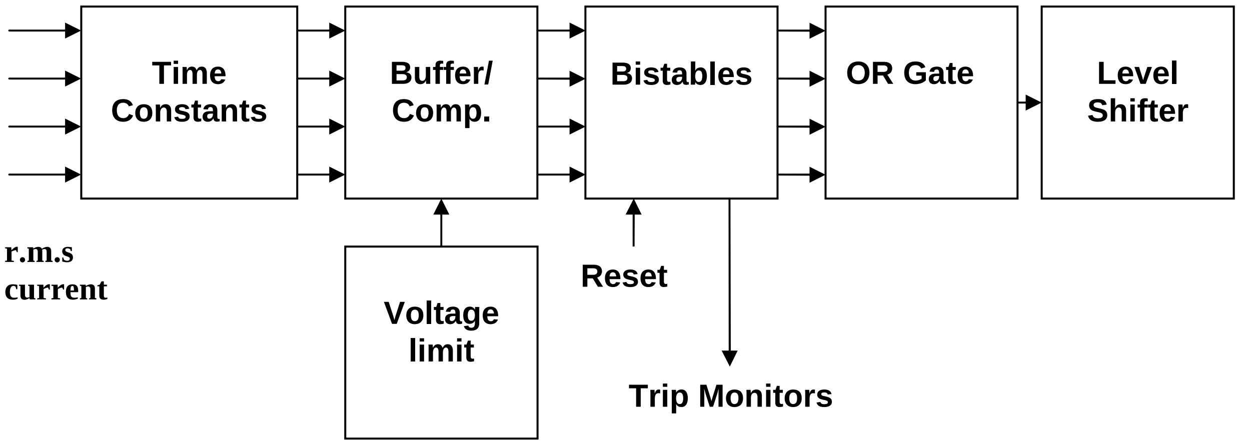
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link in place (J7/2 to 18)

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

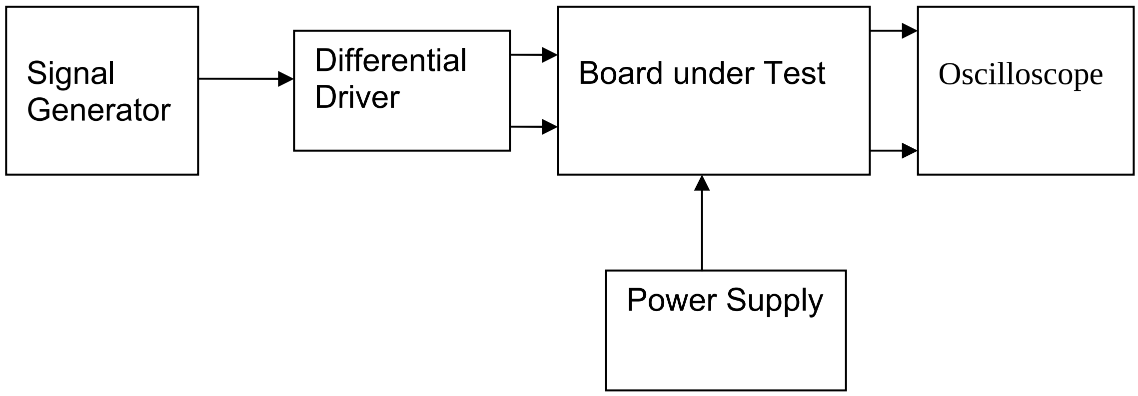
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………………PUM16P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	+12.08 v	√	2 mV
+15v TP4	+14.96 v	√	2.5 mV
-15v TP6	-15..01 v	√	7 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.312 A
-16.5v	0.251 A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.001	Pin 1 to Pin 2	1.001	√
2	1.001	Pin 5 to Pin 6	1.001	√
3	1.001	Pin 9 to Pin 10	1.001	√
4	1.001	Pin 13 to Pin 14	1.001	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.806	Pin 3 to Pin 4	0.806	√
2	0.808	Pin 7 to Pin 8	0.808	√
3	0.806	Pin 11 to Pin 12	0.805	√
4	0.804	Pin 15 to Pin 16	0.804	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.1		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.1		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.1		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.1		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.5		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.5		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.5		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.470		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.470		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.474		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.473		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.16		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.16		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.19		1.0 to 1.3v	0.5 to 2.5dB	√

Unit……………………PUM16P
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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch2	5 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch3	5 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch4	5 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.3 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch2	6.3 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch3	6.3 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch4	6.3 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	35 mV		**33 to 45mV**	**-30dB to -27dB**	√
Ch2	35 mV		**33 to 45mV**	**-30dB to -27dB**	√
Ch3	35 mV		**33 to 45mV**	**-30dB to -27dB**	√
Ch4	34 mV		**33 to 45mV**	**-30dB to -27dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.289		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch2	0.289		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch3	0.291		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch4	0.293		**0.275 to 0.32V**	**-12dB to -9dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch2	0.472		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch3	0.472		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch4	0.472		**0.46 to 0.49V**	**-7dB to -6dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch2	0.473		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch3	0.473		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch4	0.473		**0.47 to 0.49V**	**-7dB to -6dB**	√

Unit……………………PUM16P
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.185 v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.4 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.3 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.501	25 mA
Ch2	0.500	25 mA
Ch3	0.498	24.9 mA
Ch4	0.496	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.657	32.8 mA	**>16mA**	√
Ch2	0.657	32.8 mA	**>16mA**	√
Ch3	0.656	32.8 mA	**>16mA**	√
Ch4	0.656	32.8 mA	**>16mA**	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**>16mA**	√
Ch2	0.750	37.5 mA	**>16mA**	√
Ch3	0.751	37.5 mA	**>16mA**	√
Ch4	0.751	37.5 mA	**>16mA**	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	**>16mA**	√
Ch2	0.750	37.5 mA	**>16mA**	√
Ch3	0.750	37.5 mA	**>16mA**	√
Ch4	0.751	37.5 mA	**>16mA**	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.501	25.0 mA
Ch2	0.500	25.0 mA
Ch3	0.498	24.9 mA
Ch4	0.496	24.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.657	32.85 mA	>16mA	√
Ch2	0.657	32.85 mA	>16mA	√
Ch3	0.656	32.8 mA	>16mA	√
Ch4	0.655	32.75 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.751	37.5 mA	>16mA	√
Ch3	0.750	37.5 mA	>16mA	√
Ch4	0.752	37.6 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.750	37.5 mA	>16mA	√
Ch4	0.752	37.6 mA	>16mA	√

Unit……………………PUM16P
Test Engineer ………...RMC
Date …………………..7/2/2011

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.12	5.82	291 mA
Ch2	4.12	5.82	291 mA
Ch3	4.15	5.86	293 mA
Ch4	4.17	5.89	295 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.53	7.82	391 mA	>400mA	
Ch2	5.54	7.83	391 mA	>400mA	
Ch3	5.56	7.86	393 mA	>400mA	
Ch4	5.58	7.89	394 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.66	9.41	470 mA	>400mA	√
Ch2	6.68	9.44	472 mA	>400mA	√
Ch3	6.68	9.44	472 mA	>400mA	√
Ch4	6.69	9.46	473 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	>400mA	√
Ch2	6.72	9.50	475 mA	>400mA	√
Ch3	6.72	9.50	475 mA	>400mA	√
Ch4	6.73	9.51	476 mA	>400mA	√

Unit……………………PUM16P
Test Engineer ………...RMC
Date …………………..7/2/2011

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	**Ch2 stable ?**	**Ch3 stable ?**	**Ch4 stable ?**
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**

PUM Driver Board Test Report

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Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

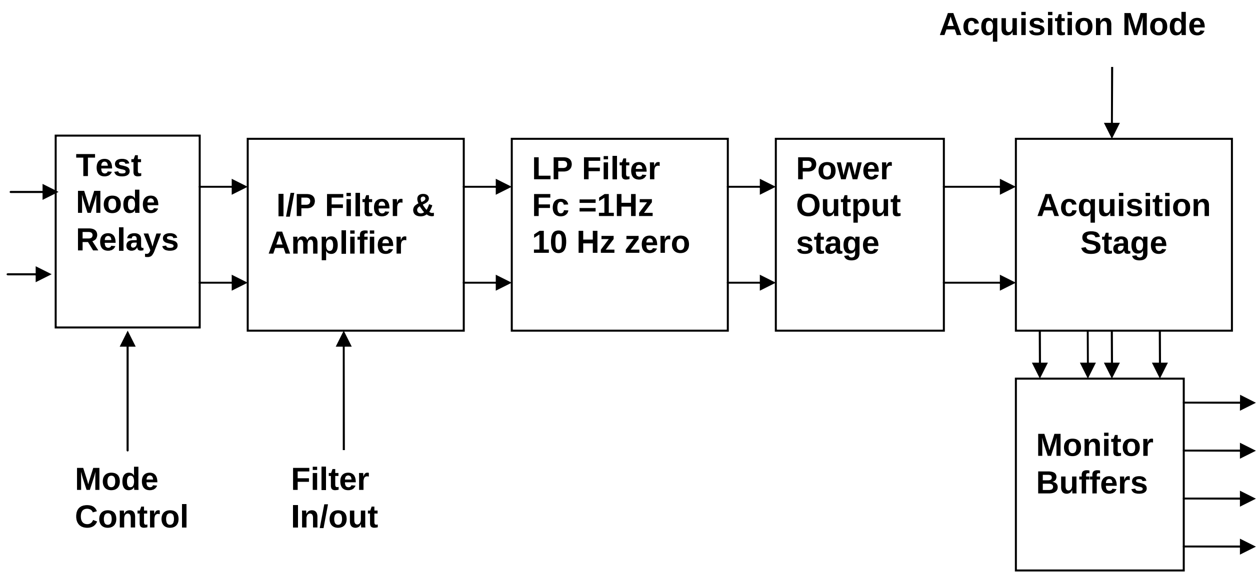
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM17P
Test Engineer ………RMC
Date …………………..9/2/11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

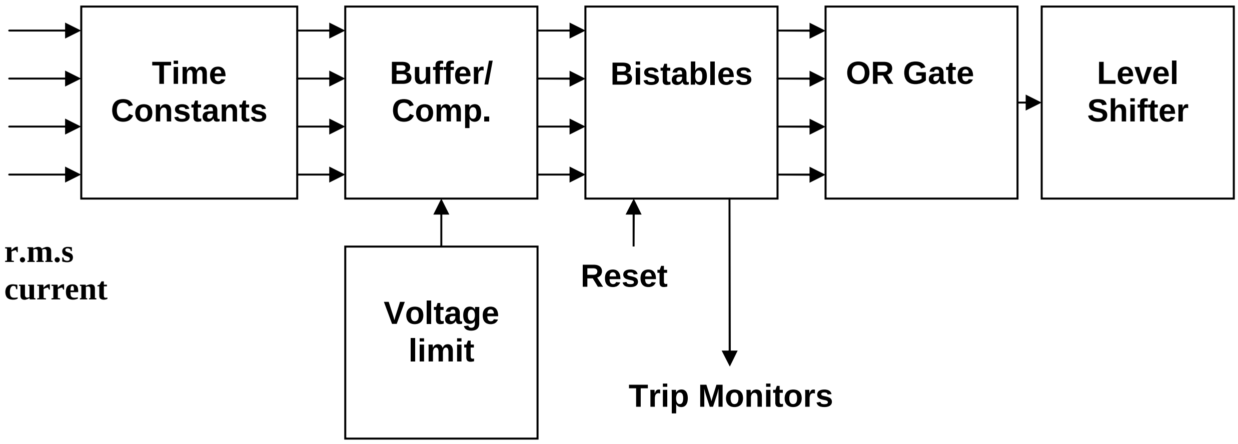
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit……………………PUM17P
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……………………PUM1√7P
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link in place (J7/2 to 18)

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

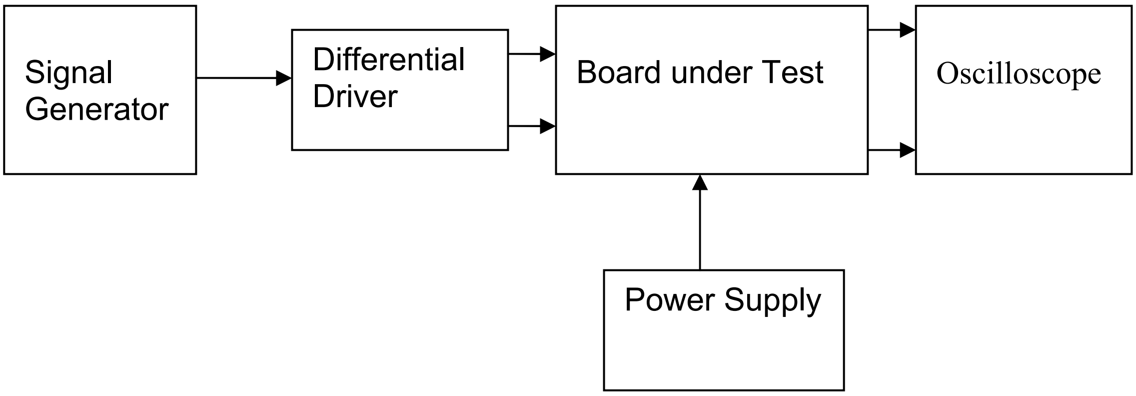
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………………PUM17P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.01 v	√	2 mV
+15v TP4	14.79 v	√	2 mV
-15v TP6	-15.08	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pick up

Record Power Supply Currents

Supply	Current
+16.5v	0.303 A
-16.5v	0.242 A

If the supplies are correct, proceed to the next test.

Unit……………………PUM17P
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.199	Pin 1 to Pin 2	1.198	√
2	0.199	Pin 5 to Pin 6	1.198	√
3	0.199	Pin 9 to Pin 10	1.198	√
4	0.199	Pin 13 to Pin 14	1.198	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.963	Pin 3 to Pin 4	0.963	√
2	0.965	Pin 7 to Pin 8	0.965	√
3	0.963	Pin 11 to Pin 12	0.963	√
4	0.965	Pin 15 to Pin 16	0.965	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.2		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.2		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.5		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.56		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.136		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.472		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.476		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.17		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.17		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.19		1.0 to 1.3v	0.5 to 2.5dB	√

Unit……………………PUM17P
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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.3 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch2	5.3 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch3	5.3 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	
Ch4	5.3 mV		**0.3 to 0.4mV**	**-70dB to -65dB**	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch2	6 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch3	6 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	
Ch4	6 mV		**3.3 to 4.2mV**	**-50dB to -45dB**	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	36.5		**33 to 45mV**	**-30dB to -27dB**	√
Ch2	34.4		**33 to 45mV**	**-30dB to -27dB**	√
Ch3	34.5		**33 to 45mV**	**-30dB to -27dB**	√
Ch4	35.8		**33 to 45mV**	**-30dB to -27dB**	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.293		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch2	0.292		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch3	0.293		**0.275 to 0.32V**	**-12dB to -9dB**	√
Ch4	0.292		**0.275 to 0.32V**	**-12dB to -9dB**	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.473		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch2	0.474		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch3	0.473		**0.46 to 0.49V**	**-7dB to -6dB**	√
Ch4	0.474		**0.46 to 0.49V**	**-7dB to -6dB**	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch2	0.474		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch3	0.474		**0.47 to 0.49V**	**-7dB to -6dB**	√
Ch4	0.474		**0.47 to 0.49V**	**-7dB to -6dB**	√

Unit……………………PUM17P
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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.17

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1 second

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.494	24.7 mA
Ch2	0.492	24.6 mA
Ch3	0.490	24.5 mA
Ch4	0.494	24.7 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654	32.7 mA	>16mA	√
Ch2	0.652	32.6 mA	>16mA	√
Ch3	0.651	32.5 mA	>16mA	√
Ch4	0.655	32.7 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	>16mA	√
Ch2	0.75	37.5 mA	>16mA	√
Ch3	0.75	37.5 mA	>16mA	√
Ch4	0.75	37.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.75	37.5 mA	>16mA	√
Ch2	0.75	37.5 mA	>16mA	√
Ch3	0.749	37.4 mA	>16mA	√
Ch4	0.75	37.5 mA	>16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.194	9.7 mA
Ch2	0.192	9.6 mA
Ch3	0.192	9.6 mA
Ch4	0.196	9.8 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.421	21.0 mA	>16mA	√
Ch2	0.418	20.9 mA	>16mA	√
Ch3	0.419	20.9 mA	>16mA	√
Ch4	0.423	21.1 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.730	36.5 mA	>16mA	√
Ch2	0.729	36.4 mA	>16mA	√
Ch3	0.729	36.4 mA	>16mA	√
Ch4	0.729	36.4 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.749	36.4 mA	>16mA	√
Ch2	0.749	36.4 mA	>16mA	√
Ch3	0.748	37.4 mA	>16mA	√
Ch4	0.749	36.4 mA	>16mA	√

Unit……………………PUM17P
Test Engineer ………RMC
Date …………………..9/2/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.14	5.85	292 mA
Ch3	4.16	5.88	294 mA
Ch4	4.14	5.85	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.57	7.88	394 mA	**>400mA**	
Ch2	5.56	7.86	393 mA	**>400mA**	
Ch3	5.57	7.88	394 mA	**>400mA**	
Ch4	5.55	7.85	392 mA	**>400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.68	9.44	472 mA	**>400mA**	√
Ch2	6.68	9.44	472 mA	**>400mA**	√
Ch3	6.68	9.44	472 mA	**>400mA**	√
Ch4	6.67	9.44	472 mA	**>400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.71	9.49	474 mA	**>400mA**	√
Ch2	6.71	9.49	474 mA	**>400mA**	√
Ch3	6.71	9.49	474 mA	**>400mA**	√
Ch4	6.70	9.47	473 mA	**>400mA**	√

Unit……………………PUM17P
Test Engineer ………RMC
Date …………………..9/2/11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291	Advanced LIGO UK	**December 2009**
PUM Driver Board Test Report		
R. M. Cutler, University of Birmingham		

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

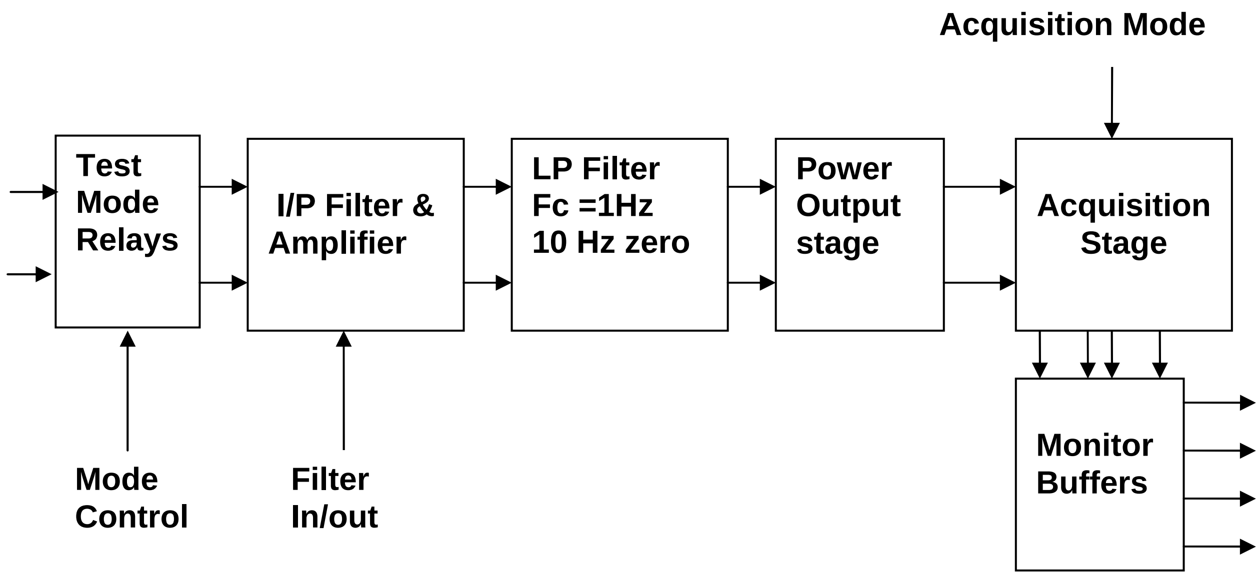
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM18P
Test Engineer ………RMC
Date …………………..10.2.11

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

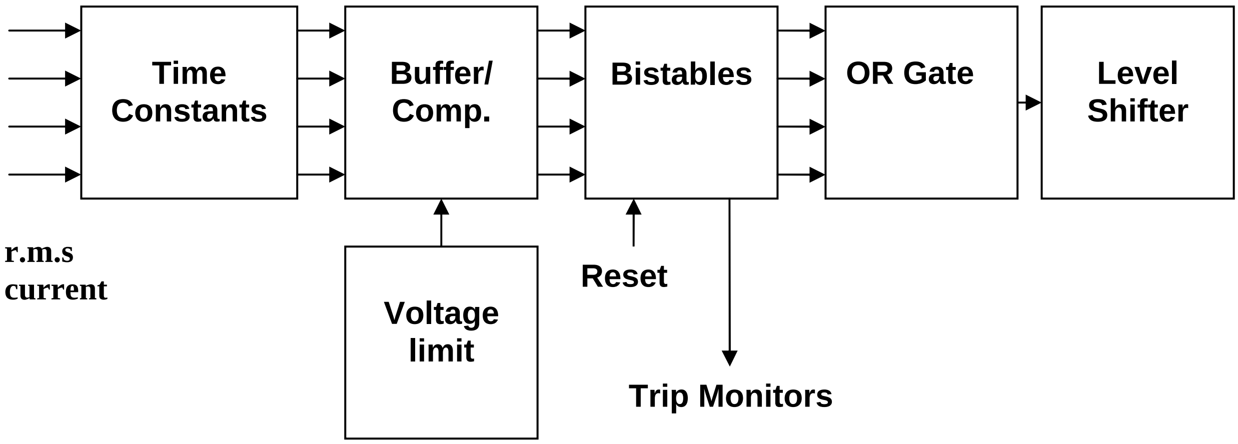
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

Unit……………………PUM18P
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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

Unit……………………PUM18P
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link in place (J7/2 to 18)

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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Test Engineer ………RMC
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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

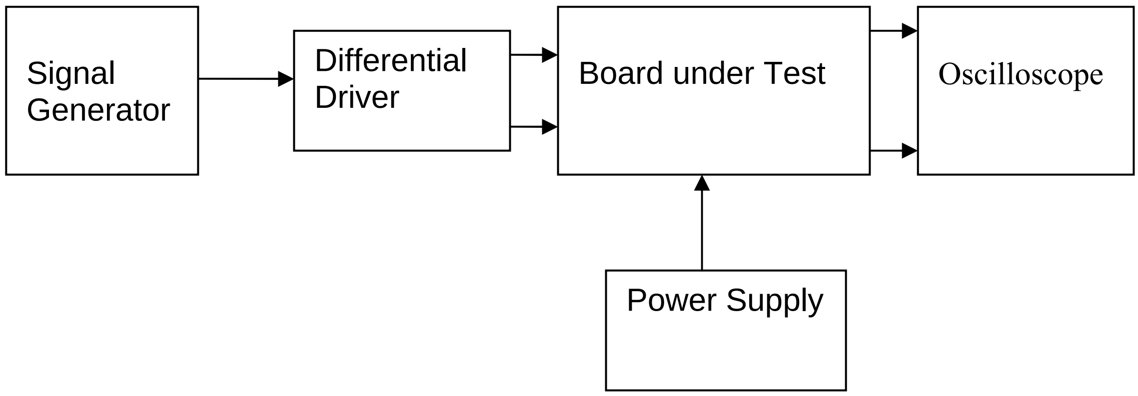
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………………PUM18P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	11.99	√	1.2 mV
+15v TP4	14.96	√	1.3 mV
-15v TP6	-14.96	√	7 mV

All Outputs smooth DC, no oscillation?	√

Record Power Supply Currents

Supply	**Current**
+16.5v	0.304
-16.5v	0.244

If the supplies are correct, proceed to the next test.

Unit……………………PUM18P
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

Unit……………………PUM18P
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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the "Not Tripped" lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.20	Pin 1 to Pin 2	1.20	√
2	1.20	Pin 5 to Pin 6	1.20	√
3	1.20	Pin 9 to Pin 10	1.20	√
4	1.20	Pin 13 to Pin 14	1.20	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.965	Pin 3 to Pin 4	0.964	√
2	0.964	Pin 7 to Pin 8	0.964	√
3	0.966	Pin 11 to Pin 12	0.966	√
4	0.965	Pin 15 to Pin 16	0.965	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.16		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.16		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.16		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.20		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.54		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.55		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.133		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.473		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.474		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.165		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.19		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.19		1.0 to 1.3v	0.5 to 2.5dB	√

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Test Engineer ………RMC
Date …………………..10.2.11

10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5 mV		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5 mV		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	7.0		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6.7		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.4		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.4		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	35.7		33 to 45mV	-30dB to -27dB	√
Ch2	35.0		33 to 45mV	-30dB to -27dB	√
Ch3	33.9		33 to 45mV	-30dB to -27dB	√
Ch4	35.1		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.292		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.294		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.470		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.471		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.475		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.475		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.471		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.472		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.475		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.475		0.47 to 0.49V	-7dB to -6dB	√

Unit……………………PUM18P
Test Engineer ………RMC
Date …………………..10.2.11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

Unit……………………PUM18P
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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.18 v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.2 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.25 seconds

Unit……………………PUM18P
Test Engineer ………RMC
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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.495	24.75 mA
Ch2	0.498	24.90 mA
Ch3	0.493	23.65 mA
Ch4	0.491	24.55 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.654	32.7 mA	>16mA	√
Ch2	0.656	32.8 mA	>16mA	√
Ch3	0.653	32.6 mA	>16mA	√
Ch4	0.651	32.5 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.749	37.4 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.749	37.3 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

Unit……………………..PUM18P
Test Engineer ………RMC
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.195	9.75 mA
Ch2	0.196	9.80 mA
Ch3	0.194	9.70 mA
Ch4	0.193	9.65 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.423	21.15 mA	>16mA	√
Ch2	0.423	21.15 mA	>16mA	√
Ch3	0.421	21.05 mA	>16mA	√
Ch4	0.419	20.95 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.45 mA	>16mA	√
Ch2	0.729	36.45 mA	>16mA	√
Ch3	0.729	36.45 mA	>16mA	√
Ch4	0.729	36.45 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	>16mA	√
Ch2	0.749	37.4 mA	>16mA	√
Ch3	0.748	37.4 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

Unit……………………PUM18P
Test Engineer ………RMC
Date …………………..10.2.11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.161	5.88	294 mA
Ch2	4.157	5.87	293 mA
Ch3	4.147	5.86	293 mA
Ch4	4.154	5.87	293 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.56	7.86	393 mA	>400mA	
Ch2	5.56	7.86	393 mA	>400mA	
Ch3	5.55	7.85	392 mA	>400mA	
Ch4	5.55	7.85	392 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	>400mA	√
Ch2	6.67	9.43	471 mA	>400mA	√
Ch3	6.67	9.43	471 mA	>400mA	√
Ch4	6.66	9.41	471 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.69	9.46	473 mA	>400mA	√
Ch2	6.69	9.46	473 mA	>400mA	√
Ch3	6.69	9.46	473 mA	>400mA	√
Ch4	6.68	9.44	472 mA	>400mA	√

Unit……………………PUM18P
Test Engineer ………RMC
Date …………………..10.2.11

13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291 Advanced LIGO UK **December 2009**

PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

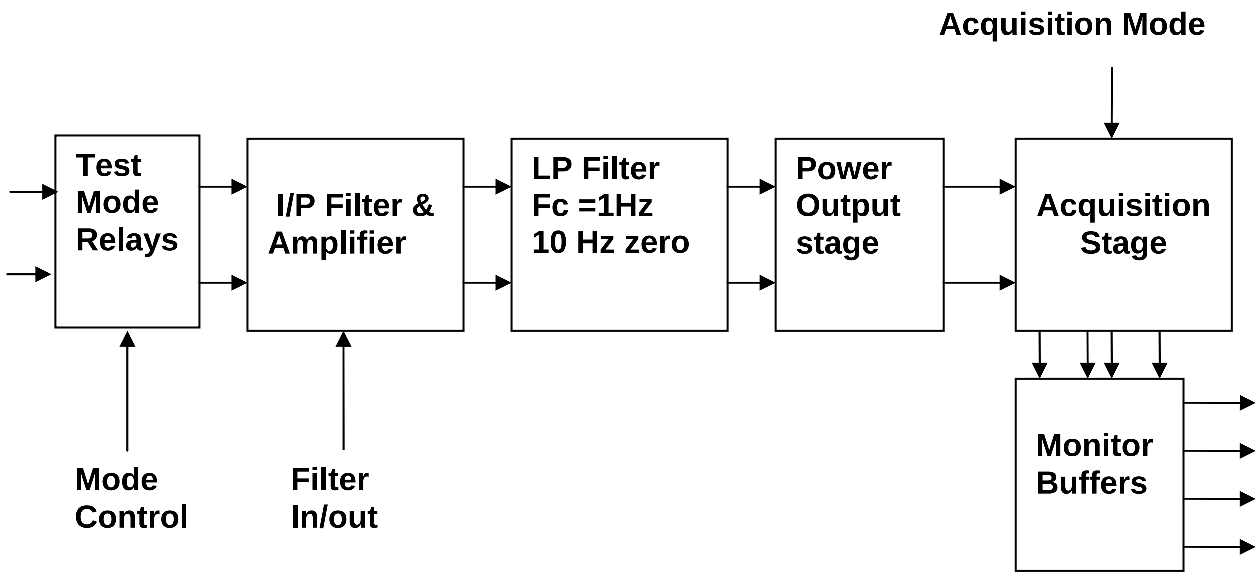
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit……………………PUM19P
Test Engineer ………RMC
Date …………………..14/2/11

Contents

1. Description

Block diagram



Description

Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

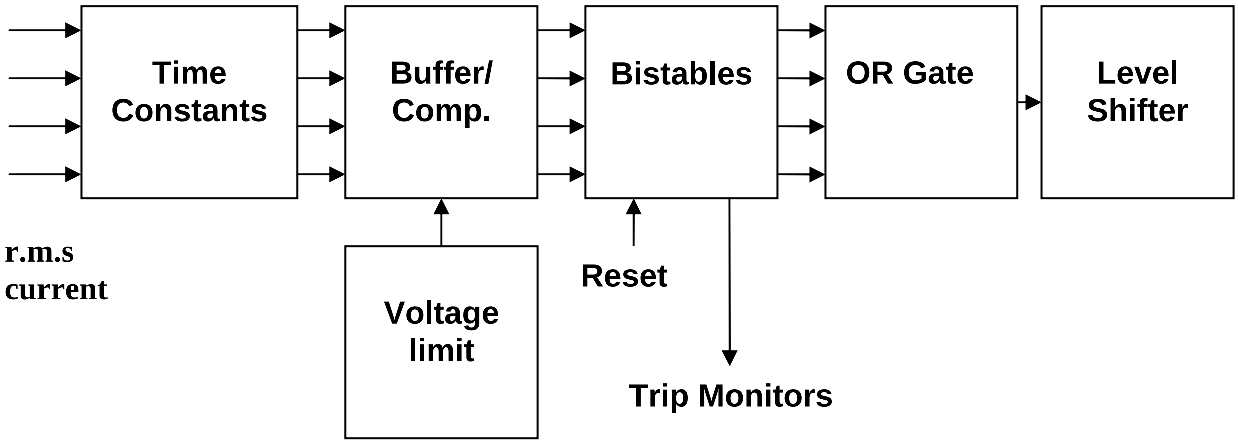
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

DVM	Fluke	287
Voltage calibrator	Time	1044
PSU	Farnell	30-2
PSU	Farnell	30-2
Scope	Tektronix	2225
DSA	Agilent	35670
Precision Amp	Stanford	SR560

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Ok

Reset link in place (J7/2 to 18)

Ch2 IC7 faulty: replaced.

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

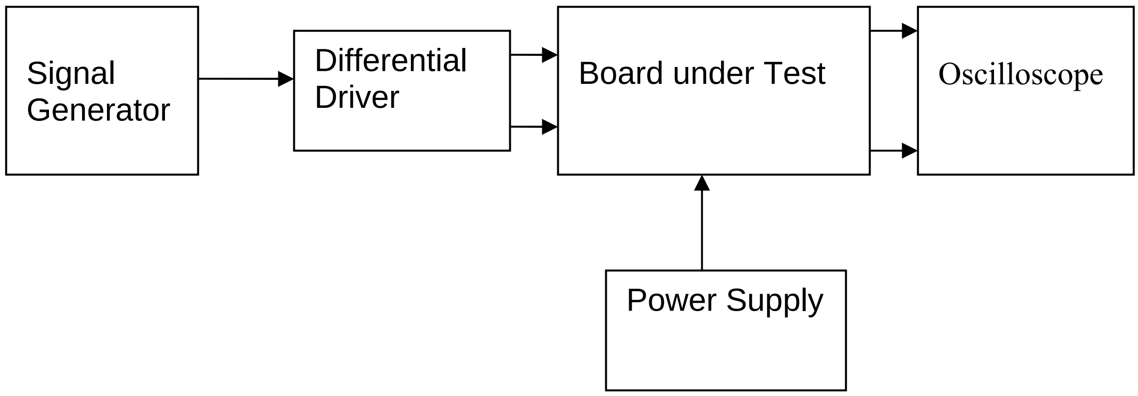
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
5	0V	√		
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……………………PUM19P
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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	Output voltage	Nominal +/- 0.5v?	Output noise
+12v TP5	12.011	√	1.5 mV
+15v TP4	14.832	√	2 mV
-15v TP6	-15.107	√	7 mV

All Outputs smooth DC, no oscillation?	√

Some pickup present

Record Power Supply Currents

Supply	Current
+16.5v	0.315
-16.5v	0.254

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

ACQUISITION RELAYS

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the “Not Tripped” indicators are on.

NOT TRIPPED indicators

Channel	**Indicator**
	ON?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.200	Pin 1 to Pin 2	1.200	√
2	1.200	Pin 5 to Pin 6	1.200	√
3	1.200	Pin 9 to Pin 10	1.200	√
4	1.200	Pin 13 to Pin 14	1.200	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	0.96	Pin 3 to Pin 4	0.96	√
2	0.96	Pin 7 to Pin 8	0.96	√
3	0.96	Pin 11 to Pin 12	0.96	√
4	0.96	Pin 15 to Pin 16	0.96	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.17		1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.17		1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.17		1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.17		1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.52		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.52		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.51		0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.53		0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.132		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.130		0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.131		0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.470		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.472		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.478		0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.475		0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.165		1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.166		1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.166		1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	1.189		1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.189		1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.189		1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.188		1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	5.4		0.3 to 0.4mV	-70dB to -65dB	
Ch2	5.5		0.3 to 0.4mV	-70dB to -65dB	
Ch3	5.5		0.3 to 0.4mV	-70dB to -65dB	
Ch4	5.4		0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	6.64		3.3 to 4.2mV	-50dB to -45dB	
Ch2	6.57		3.3 to 4.2mV	-50dB to -45dB	
Ch3	6.61		3.3 to 4.2mV	-50dB to -45dB	
Ch4	6.47		3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	39.6		33 to 45mV	-30dB to -27dB	√
Ch2	39.4		33 to 45mV	-30dB to -27dB	√
Ch3	39.7		33 to 45mV	-30dB to -27dB	√
Ch4	39.2		33 to 45mV	-30dB to -27dB	√

100Hz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.294		0.275 to 0.32V	-12dB to -9dB	√
Ch2	0.291		0.275 to 0.32V	-12dB to -9dB	√
Ch3	0.293		0.275 to 0.32V	-12dB to -9dB	√
Ch4	0.290		0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.472		0.46 to 0.49V	-7dB to -6dB	√
Ch2	0.473		0.46 to 0.49V	-7dB to -6dB	√
Ch3	0.470		0.46 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	-6dB	Simulation		Pass/Fail
Ch1	0.474		0.47 to 0.49V	-7dB to -6dB	√
Ch2	0.475		0.47 to 0.49V	-7dB to -6dB	√
Ch3	0.471		0.47 to 0.49V	-7dB to -6dB	√
Ch4	0.472		0.47 to 0.49V	-7dB to -6dB	√

Unit……………………PUM19P
Test Engineer ………RMC
Date …………………..14/2/11

11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, press the reset button on the test box or turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.19v

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	1.5 seconds

Unit……………………PUM19P
Test Engineer ………RMC
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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.495	24.75 mA
Ch2	0.493	24.65 mA
Ch3	0.495	24.75 mA
Ch4	0.494	24.70 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.653	32.65 mA	>16mA	√
Ch2	0.653	32.65 mA	>16mA	√
Ch3	0.654	32.70 mA	>16m A	√
Ch4	0.654	32.70 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.751	37.5 mA	>16mA	√
Ch3	0.751	37.5 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.750	37.5 mA	>16mA	√
Ch2	0.751	37.5 mA	>16mA	√
Ch3	0.751	37.5 mA	>16mA	√
Ch4	0.750	37.5 mA	>16mA	√

Unit……………………PUM19P
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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.193	9.65 mA
Ch2	0.193	9.65 mA
Ch3	0.196	9.80 mA
Ch4	0.195	9.75 mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.418	20.9 mA	>16mA	√
Ch2	0.420	21.0 mA	>16mA	√
Ch3	0.424	21.2 mA	>16mA	√
Ch4	0.422	21.1 mA	>16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.729	36.4 mA	>16mA	√
Ch2	0.730	36.5 mA	>16mA	√
Ch3	0.730	36.5 mA	>16mA	√
Ch4	0.730	36.5 mA	>16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.748	37.4 mA	>16mA	√
Ch2	0.750	37.5 mA	>16mA	√
Ch3	0.749	37.4 mA	>16mA	√
Ch4	0.749	37.4 mA	>16mA	√

Unit……………………PUM19P
Test Engineer ………RMC
Date …………………..14/2/11

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)
Ch1	4.16	5.88	294 mA
Ch2	4.15	5.57	293 mA
Ch3	4.16	5.88	294 mA
Ch4	4.13	5.84	292 mA

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.56	7.86	393 mA	>400mA	
Ch2	5.56	7.86	393 mA	>400mA	
Ch3	5.56	7.86	393 mA	>400mA	
Ch4	5.54	7.83	391 mA	>400mA	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.67	9.43	471 mA	>400mA	√
Ch2	6.68	9.44	472 mA	>400mA	√
Ch3	6.67	9.43	471 mA	>400mA	√
Ch4	6.68	9.44	472 mA	>400mA	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.70	9.47	473 mA	>400mA	√
Ch2	6.72	9.50	475 mA	>400mA	√
Ch3	6.70	9.47	473 mA	>400mA	√
Ch4	6.71	9.49	474 mA	>400mA	√

Unit……………………PUM19P
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13. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Check stability while slowly increasing the output voltage. (Link W2 in)

	Ch1 stable ?	Ch2 stable ?	Ch3 stable ?	Ch4 stable ?
-10v	√	√	√	√
-7v	√	√	√	√
-5v	√	√	√	√
-1v	√	√	√	√
0v	√	√	√	√
1v	√	√	√	√
5v	√	√	√	√
7v	√	√	√	√
10v	√	√	√	√

LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900291-V2	Advanced LIGO UK	**June 2010**

PUM Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

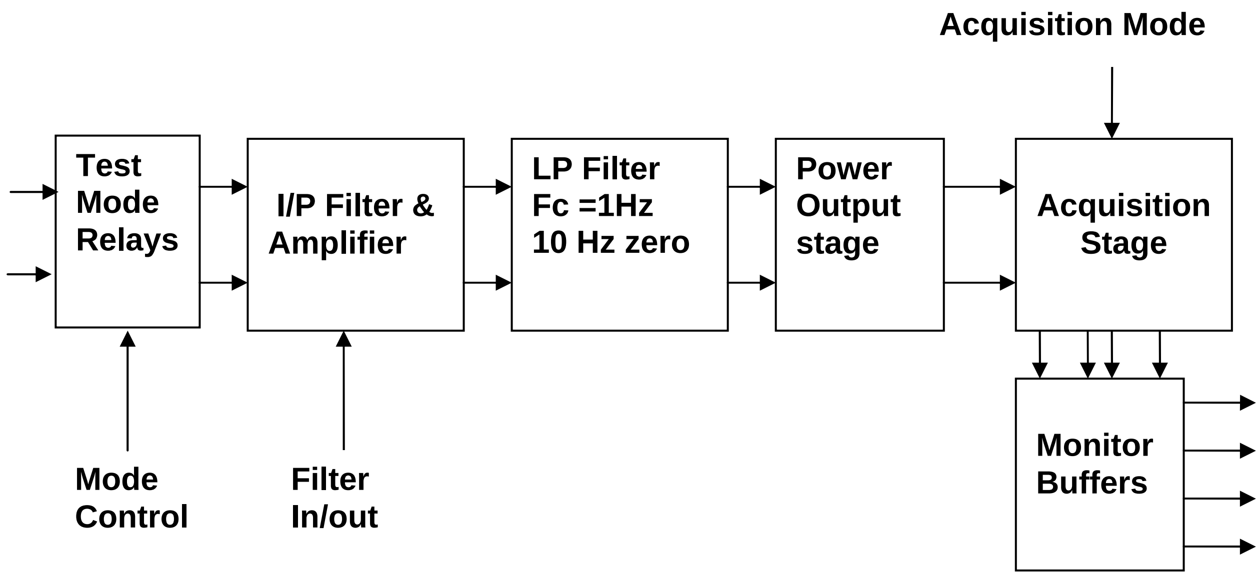
http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

Unit………………PUM1P   Serial No ………………………………
Test Engineer …RMC
Date ……………20/12/09

Contents

1. Description

Block diagram



Description
Each PUM Driver board consists of four identical channels and the power regulators which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block has a gain of 1.2.

The third block contains a low pass filter with a corner frequency of 0.5 Hz, followed by a complimentary zero at 5 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 0.5 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 5 Hz, after which the characteristic levels off. This filter may be switched in and out by command as required under relay control.

The third block also contains a high pass section which increases the gain at high frequencies to give the required dynamic range at high frequencies.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is wired to have unity gain, the operational amplifier providing the internal gain in the loop. The loop is closed around the buffer/operational amplifier pair. The current limit is set of the driver is set to 0. 5A

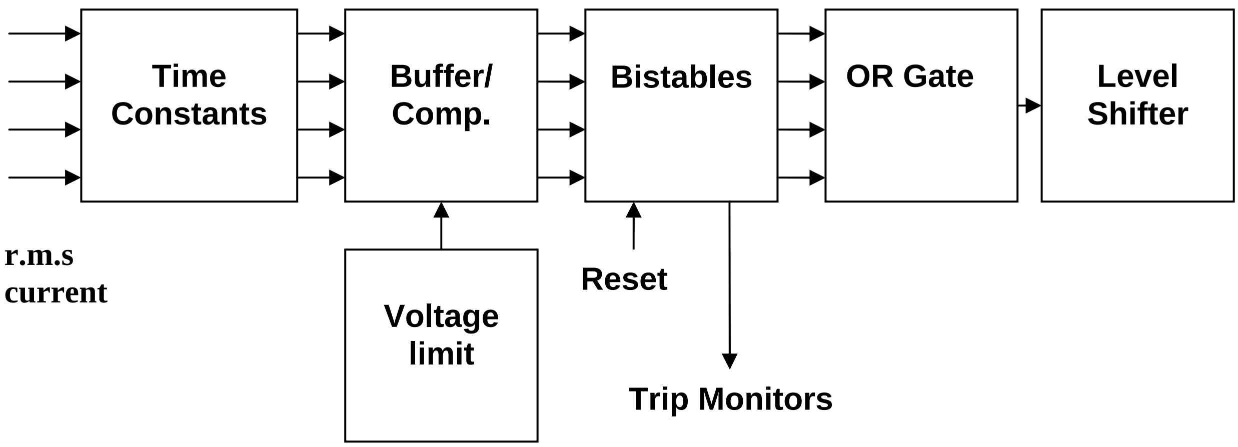
The current limit during acquisition is controlled by a circuit which is common to all driver channels (described below).

The outputs are buffered by unity gain voltage followers which drive the monitor board.

Acquisition Mode Current Limit

The current limit during acquisition mode is controlled by an OSEM protection circuit which is common to all channels.

The RMS output currents are measured on the monitor board, then fed into the OSEM Protection Circuit. This circuit is designed to trip if the r.m.s current into an OSEM exceeds the preset limit for more than a predetermined time.



The OSEM Protection Circuit

The OSEM coils must not be allowed to overheat, as this causes out-gassing. However, during Acquisition, a high current is required for a short period. This period is not long enough to allow the coil to become hot and outgas significantly. However the coils require protection against excessive currents for prolonged periods.

The inputs to the OSEM protection circuit monitor the r.m.s current flowing in each Osem coil. A voltage proportional to the r.m.s current is passed through a delay network. If an OSEM current exceeds the limit by more than a certain time, the threshold level is reached, and the corresponding bistable is set.

The outputs of the four bistables are combined in an OR gated, energising a level shifting circuit which switches off all the drivers. The use of a bistable ensures that oscillation is prevented.

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2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Scope	Tektronix	2225	
PSU	Farnell	LT30-1	
PSU	Farnell	LT30-2	
Calibrator	Time	1044	

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

OK

Links:

Check that the link W4 is present on each channel.
Connect the test lead to ground pins 1,3,5 and 7 on P3, the Monitor Input 16 way header.

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4. Continuity Checks

J2

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
	5	0V	√	
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

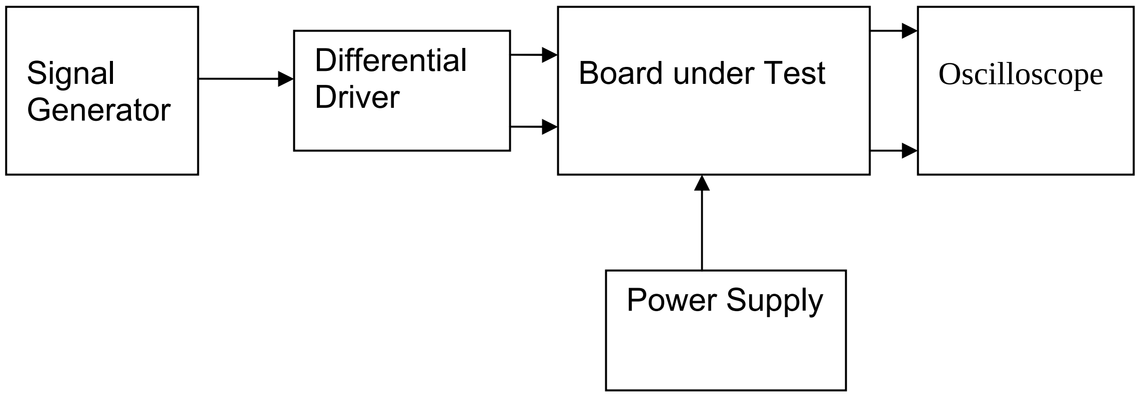
J5

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	√
2	Imon2P		6	√
3	Imon3P		7	√
4	Imon4P		8	√
	5	0V	√	
6	Imon1N		18	√
7	Imon2N		19	√
8	Imon3N		20	√
9	Imon4N		21	√

Power Supply to Satellite box
J1

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	√
10	V+ (TP1)	+17v Supply	√
11	V- (TP2)	-17v Supply	√
12	V- (TP2)	-17v Supply	√
13	0V (TP3)		√
22	0V (TP3)		√
23	0V (TP3)		√
24	0V (TP3)		√
25	0V (TP3)		√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check that the 3 pin power connector is wired correctly: A1 positive, A2 return, A3 Negative.

Set the power supply outputs to zero.
Connect power to the unit
Ensure that the test ribbon cable is connected to P3, and that pins 1,3,5 and 7 are grounded.
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct on TP1 and TP2.
If they are, increase input voltages to +/- 16.5v.
Press the reset button on the test box.
Record the output voltages, measured on a DVM with 4 or more digits, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each regulator output.
Record regulator outputs:

Regulator	**Output voltage**	**Nominal +/- 0.5v?**	**Output noise**
+12v TP5	12.0v	√	1mV p/p
+15v TP4	14.9v	√	1mV p/p
-15v TP6	-15.145v	√	5mV p/p

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	**Current**
+16.5v	0.55A
-16.5v	-0.25A

If the supplies are correct, proceed to the next test.

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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST RELAYS √

Channel	Indicator		OK?
	ON	OFF	
Ch1			√
Ch2			√
Ch3			√
Ch4			√

ACQUISITION RELAYS

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Press the Reset button on the test box. Ensure that the "Not Tripped" indicators are on.

NOT TRIPPED indicators

Channel	Indicator
	ON?
Ch1	
Ch2	
Ch3	
Ch4	

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8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.
With a 20 ohm dummy load on each channel, apply a 1v r.m.s input at 100Hz as measured between TP1 and TP2. Measure the voltage monitor outputs and compare with the voltages between TP10 and TP12.
Measure the current monitor outputs and compare with the voltage between the outputs of R29 and R130. Repeat for each channel.
A ribbon cable grounding pins 1, 3, 5 and 7 is necessary in the r.m.s header socket. Press the Reset button on the test box.
Ensure that the “Not Tripped” lights are on.

8.1 Voltage Monitors

Ch.	Output: TP10 to TP12	Monitor Pins P1	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.200	Pin 1 to Pin 2	1.200	√
2	1.200	Pin 5 to Pin 6	1.200	√
3	1.200	Pin 9 to Pin 10	1.200	√
4	1.200	Pin 13 to Pin 14	1.200	√

8.2 Current monitors

Ch.	Output between R29 and R130	Monitor Pins	Monitor Voltage	Pass/Fail: Equal? (+/- 0.1v)
1	1.187	Pin 3 to Pin 4	1.187	√
2	1.187	Pin 7 to Pin 8	1.187	√
3	1.187	Pin 11 to Pin 12	1.187	√
4	1.187	Pin 15 to Pin 16	1.187	√

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9. Frequency Response Test, Low Noise Mode: Insert link W4 for each channel. Switch in the filter and test the response using the signal generator. With a 1Vrms input signal between TP1 and TP2, measure the output between TP10 and TP12. Alternatively, use the Dynamic Signal analyser.

0.1Hz

	Output	Simulation		Pass/Fail
Ch1	1.I2V	1.0 to 1.3v	0.4 to 2.4dB	√
Ch2	1.I2V	1.0 to 1.3v	0.4 to 2.4dB	√
Ch3	1.I2V	1.0 to 1.3v	0.4 to 2.4dB	√
Ch4	1.I2V	1.0 to 1.3v	0.4 to 2.4dB	√

1Hz

	Output	Simulation		Pass/Fail
Ch1	0.56v	0.48 to 0.6v	-6.5 to -4.5dB	√
Ch2	0.53v	0.48 to 0.6v	-6.5 to -4.5dB	√
Ch3	0.53v	0.48 to 0.6v	-6.5 to -4.5dB	√
Ch4	0.53v	0.48 to 0.6v	-6.5 to -4.5dB	√

10Hz

	Output	Simulation		Pass/Fail
Ch1	0.13v	0.12 to 0.15v	-16.5 to -18.5dB	√
Ch2	0.13v	0.12 to 0.15v	-16.5 to -18.5dB	√
Ch3	0.13v	0.12 to 0.15v	-16.5 to -18.5dB	√
Ch4	0.13v	0.12 to 0.15v	-16.5 to -18.5dB	√

100Hz

	Output	Simulation		Pass/Fail
Ch1	0.468v	0.42 to 0.52v	-5.5 to -7.5dB	√
Ch2	0.479v	0.42 to 0.52v	-5.5 to -7.5dB	√
Ch3	0.475v	0.42 to 0.52v	-5.5 to -7.5dB	√
Ch4	0.474v	0.42 to 0.52v	-5.5 to -7.5dB	√

1 KHz

	Output	Simulation		Pass/Fail
Ch1	1.16v	1.0 to 1.28v	0.34 to 2.34dB	√
Ch2	1.16v	1.0 to 1.28v	0.34 to 2.34dB	√
Ch3	1.16v	1.0 to 1.28v	0.34 to 2.34dB	√
Ch4	1.16v	1.0 to 1.28v	0.34 to 2.34dB	√

5 KHz

	Output	Simulation		Pass/Fail
Ch1	1.19v	1.0 to 1.3v	0.5 to 2.5dB	√
Ch2	1.19v	1.0 to 1.3v	0.5 to 2.5dB	√
Ch3	1.19v	1.0 to 1.3v	0.5 to 2.5dB	√
Ch4	1.19v	1.0 to 1.3v	0.5 to 2.5dB	√

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10. Frequency Response Test, Acquisition Mode: Switch the filter off and Acquisition mode on. Connect a 20 ohm load resistor each channel. Test the response using the signal generator. With a 1v rms input signal between TP1 and TP2, measure the output across the load resistor.

0.1Hz

	Output	Simulation		Pass/Fail
Ch1	12mV	0.3 to 0.4mV	-70dB to -65dB	
Ch2	12mV	0.3 to 0.4mV	-70dB to -65dB	
Ch3	12mV	0.3 to 0.4mV	-70dB to -65dB	
Ch4	12mV	0.3 to 0.4mV	-70dB to -65dB	

1Hz

	Output	Simulation		Pass/Fail
Ch1	12mV	3.3 to 4.2mV	-50dB to -45dB	
Ch2	12mV	3.3 to 4.2mV	-50dB to -45dB	
Ch3	12mV	3.3 to 4.2mV	-50dB to -45dB	
Ch4	12mV	3.3 to 4.2mV	-50dB to -45dB	

10Hz

	Output	Simulation		Pass/Fail
Ch1	27mV	33 to 45mV	-30dB to -27dB	
Ch2	30mV	33 to 45mV	-30dB to -27dB	
Ch3	28mV	33 to 45mV	-30dB to -27dB	
Ch4	30mV	33 to 45mV	-30dB to -27dB	

100Hz

	Output	Simulation		Pass/Fail
Ch1	291.7mV	0.275 to 0.32V	-12dB to -9dB	√
Ch2	291.5mV	0.275 to 0.32V	-12dB to -9dB	√
Ch3	290.2mV	0.275 to 0.32V	-12dB to -9dB	√
Ch4	292.4mV	0.275 to 0.32V	-12dB to -9dB	√

1 KHz

	Output	Simulation		Pass/Fail
Ch1	473mV	0.46 to 0.49V	-7dB to -6dB	√
Ch2	473mV	0.46 to 0.49V	-7dB to -6dB	√
Ch3	474mV	0.46 to 0.49V	-7dB to -6dB	√
Ch4	473mV	0.46 to 0.49V	-7dB to -6dB	√

5 KHz

	Output	Simulation		Pass/Fail
Ch1	474mV	0.47 to 0.49V	-7dB to -6dB	√
Ch2	474mV	0.47 to 0.49V	-7dB to -6dB	√
Ch3	475mV	0.47 to 0.49V	-7dB to -6dB	√
Ch4	473mV	0.47 to 0.49V	-7dB to -6dB	√

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11. Distortion

Switch the filters out. Increase input voltage to 10v peak, f = 1KHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	**Non-Acquisition Mode: Distortion Free?**
Ch1	√	√
Ch2	√	√
Ch3	√	√
Ch4	√	√

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12. Trip Circuit Tests

A test cable may be used for these tests, consisting of a ribbon cable which plugs into the 16 way header P3. It is convenient to common pins 1, 3, 5, 7, and apply a test voltage to them.

Alternatively an external test box may be used, enabling each input to be tested in turn.

Apply a test voltage to the inputs, and observe the OP400 outputs. An exponential rise in the outputs will be observed. When the logic threshold is reached, the bistable will become set, causing the OR gate output TP25 to go to logic 1. The collector of Q1 will go to high causing the trip pins on each of the drivers to be pulled down to the negative rail, switching them off,

Connect the test lead.
Observe TP25. It should initially be at 0v. If not, turn off all signal inputs and cycle the power supply.

Set the precision voltage source to 1v, representing an r.m.s current of 150mA, and connect it to the ribbon cable input. Observe TP25 for several minutes. It should not go high.

Stays low?	√

Very slowly increase the voltage, and observe the level at which it trips.

Trip voltage?	1.2V

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 1.66v representing 250mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2.5 seconds

Reduce the input voltage to 0v, and wait for the capacitors to discharge.
Cycle the power supply.

Remove the voltage source, set it to 2.66v representing 400mA. Reconnect it, measuring how long it is before TP25 goes high.

Time taken to trip?	2 seconds

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12 Load tests

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

12.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below.
Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)
Ch1	0.234v	11.7mA
Ch2	0.234v	11.7mA
Ch3	0.235v	11.75mA
Ch4	0.234v	11.7mA

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.401v	20.0mA	16mA	√
Ch2	0.402v	20.0mA	16mA	√
Ch3	0.405v	20.2mA	16mA	√
Ch4	0.403v	20.1mA	16mA	√

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.724v	36.2mA	16mA	√
Ch2	0.724v	36.2mA	16mA	√
Ch3	0.724v	36.2mA	16mA	√
Ch4	0.72v	36.0mA	16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	0.765v	38.25mA	16mA	√
Ch2	0.765v	38.25mA	16mA	√
Ch3	0.765v	38.25mA	16mA	√
Ch4	0.764v	37.5mA	16mA	√

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12.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s, at the frequencies below. Calculate the output current in each case (Vout/20).

100Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	90.22 mV	4.51mA		
Ch2	92.5 mV	4.625 mA		
Ch3	92.5 mV	4.625 mA		
Ch4	90 mV	4.5 mA		

200Hz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	255 mV	12.75 mA	16mA	
Ch2	258 mV	12.9 mA	16mA	
Ch3	260 mV	13.0 mA	16mA	
Ch4	258 mV	12.9 mA	16mA	

1 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	702 mV	35.1mA	16mA	√
Ch2	702 mV	35.1mA	16mA	√
Ch3	703 mV	35.1mA	16mA	√
Ch4	700 mV	35.0 mA	16mA	√

5 KHz

	Vo r.m.s	Io r.m.s (Vo/20)	Specification	Pass/Fail
Ch1	760 mV	38 mA	16mA	√
Ch2	730 mV	36.5 mA	16mA	√
Ch3	760 mV	38 mA	16mA	√
Ch4	750 mV	37.5 mA	16mA	√

Unit……………………PUM1P…Serial No ………………………………
Test Engineer ………RMC
Date …………………20/12/09

12.3 Acquisition Mode

With the acquisition mode switched in, and filters switched out, apply 10v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20). Do not leave the board running with a 10v input for long, especially if the heat sink is not fitted.

100Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	4.12	5.82	291mA		
Ch2	4.12	5.82	291mA		
Ch3	4.10	5.80	289mA		
Ch4	4.17	5.89	294mA		

200Hz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	5.62	7.94	397mA	**400mA**	
Ch2	5.62	7.94	397mA	**400mA**	
Ch3	5.62	7.94	397mA	**400mA**	
Ch4	5.66	8.00	400mA	**400mA**	

1 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.68	9.44	372mA	**400mA**	√
Ch2	6.68	9.44	372mA	**400mA**	√
Ch3	6.69	9.46	372mA	**400mA**	√
Ch4	6.70	9.475	373mA	**400mA**	√

5 KHz

	Vo r.m.s	Vo pk.	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	6.83	9.66	482.9mA	**400mA**	√
Ch2	6.83	9.66	482.9mA	**400mA**	√
Ch3	6.83	9.66	482.9mA	**400mA**	√
Ch4	6.74	9.53	476.0mA	**400mA**	√