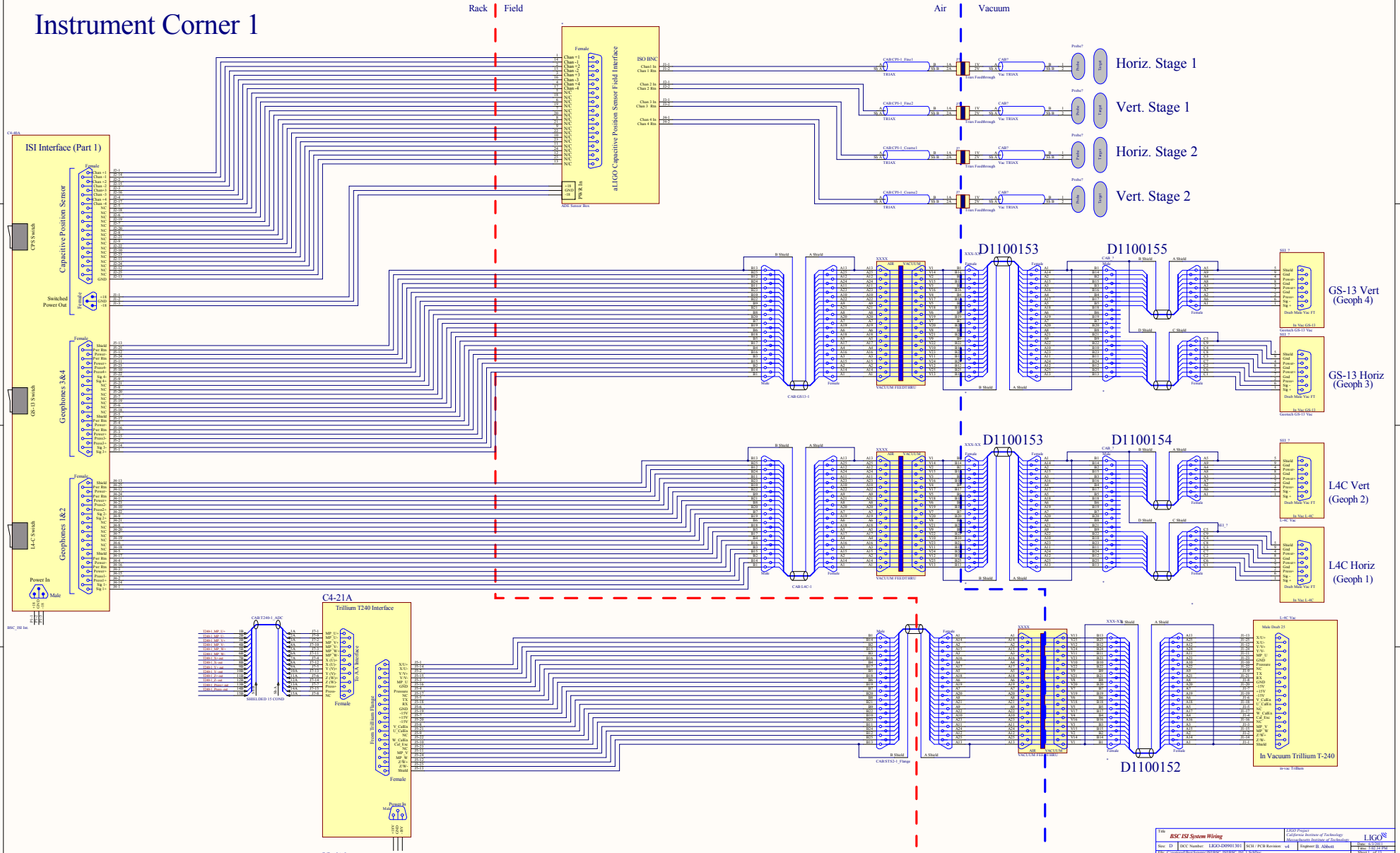
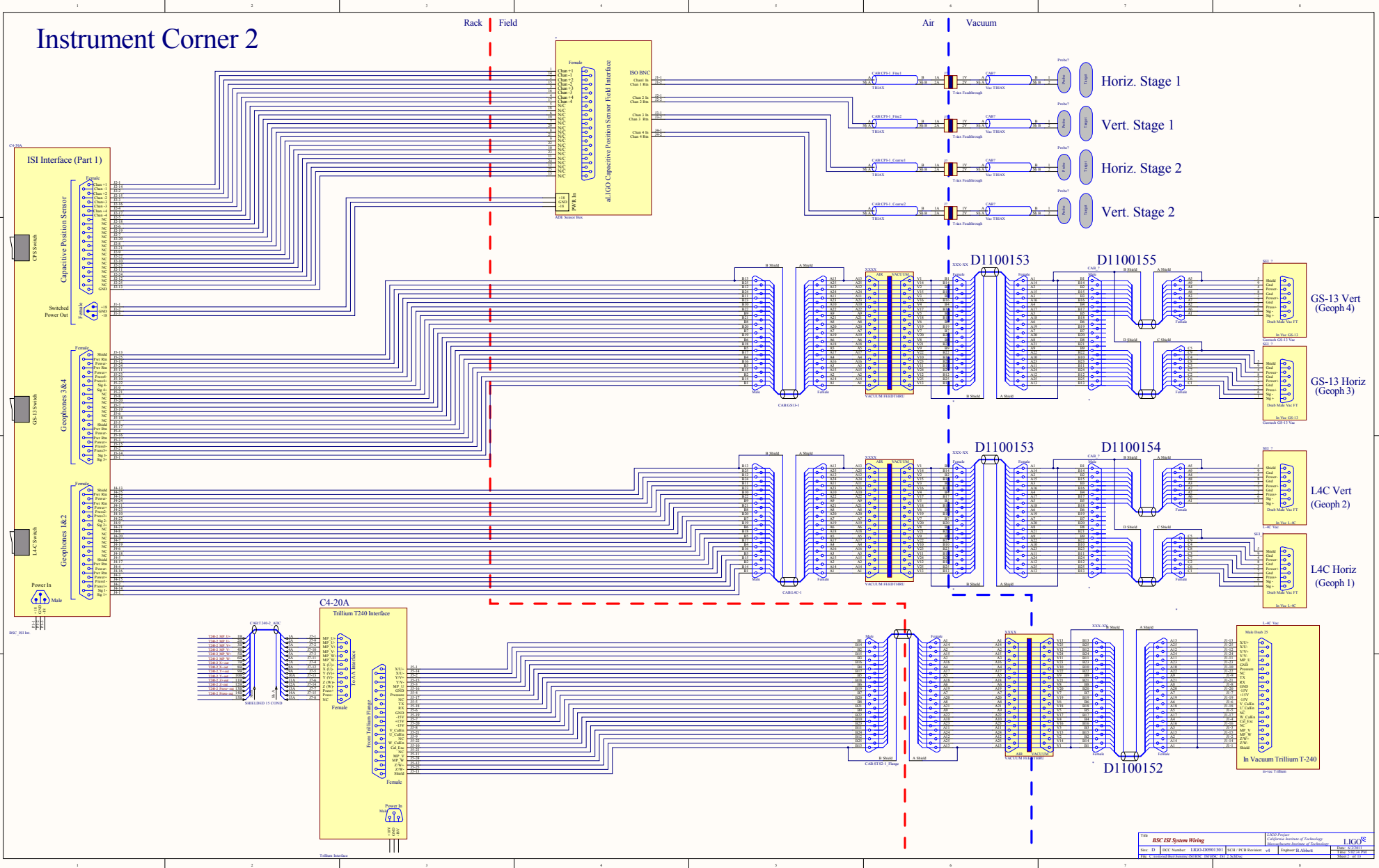


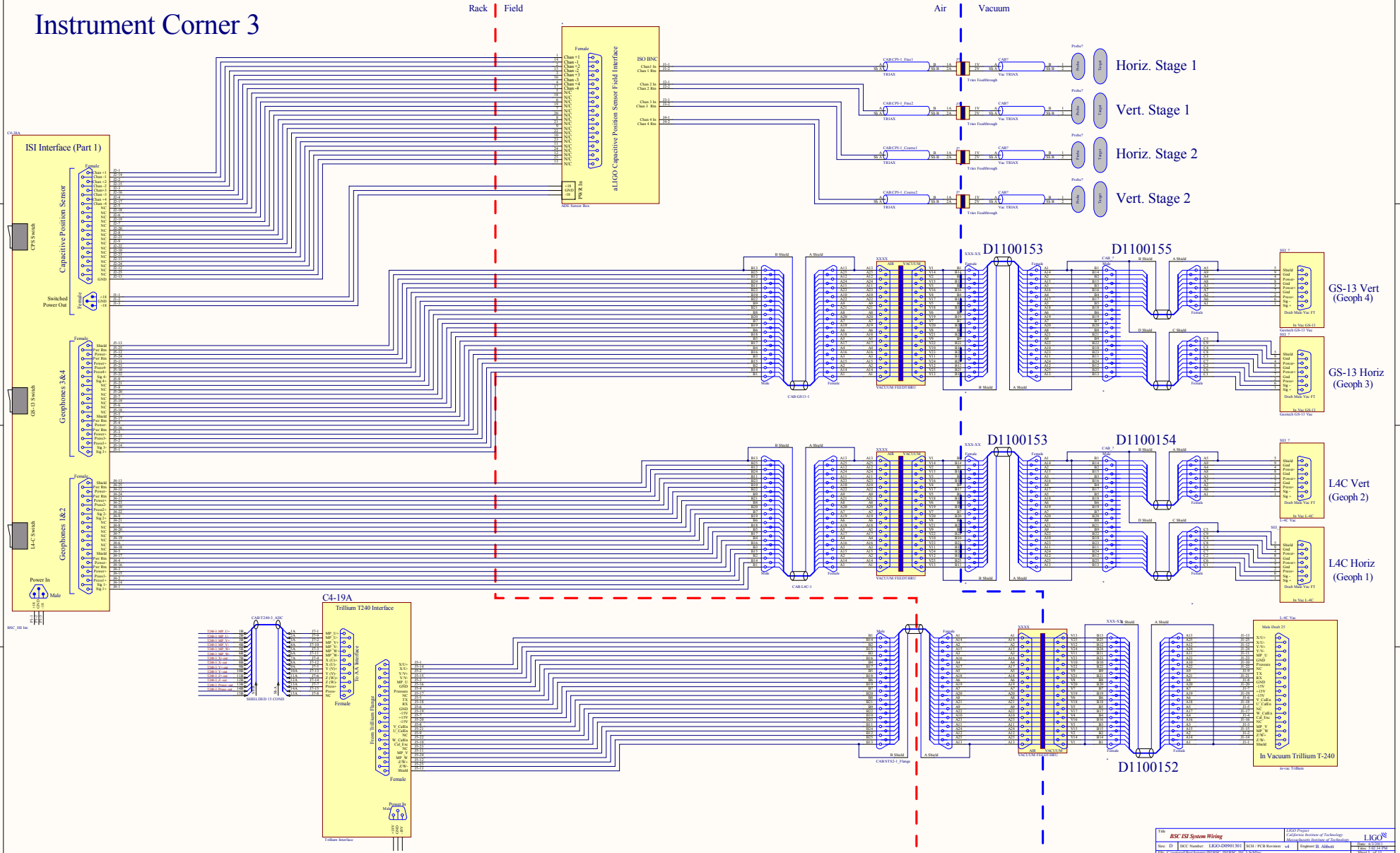
Instrument Corner 1



Instrument Corner 2

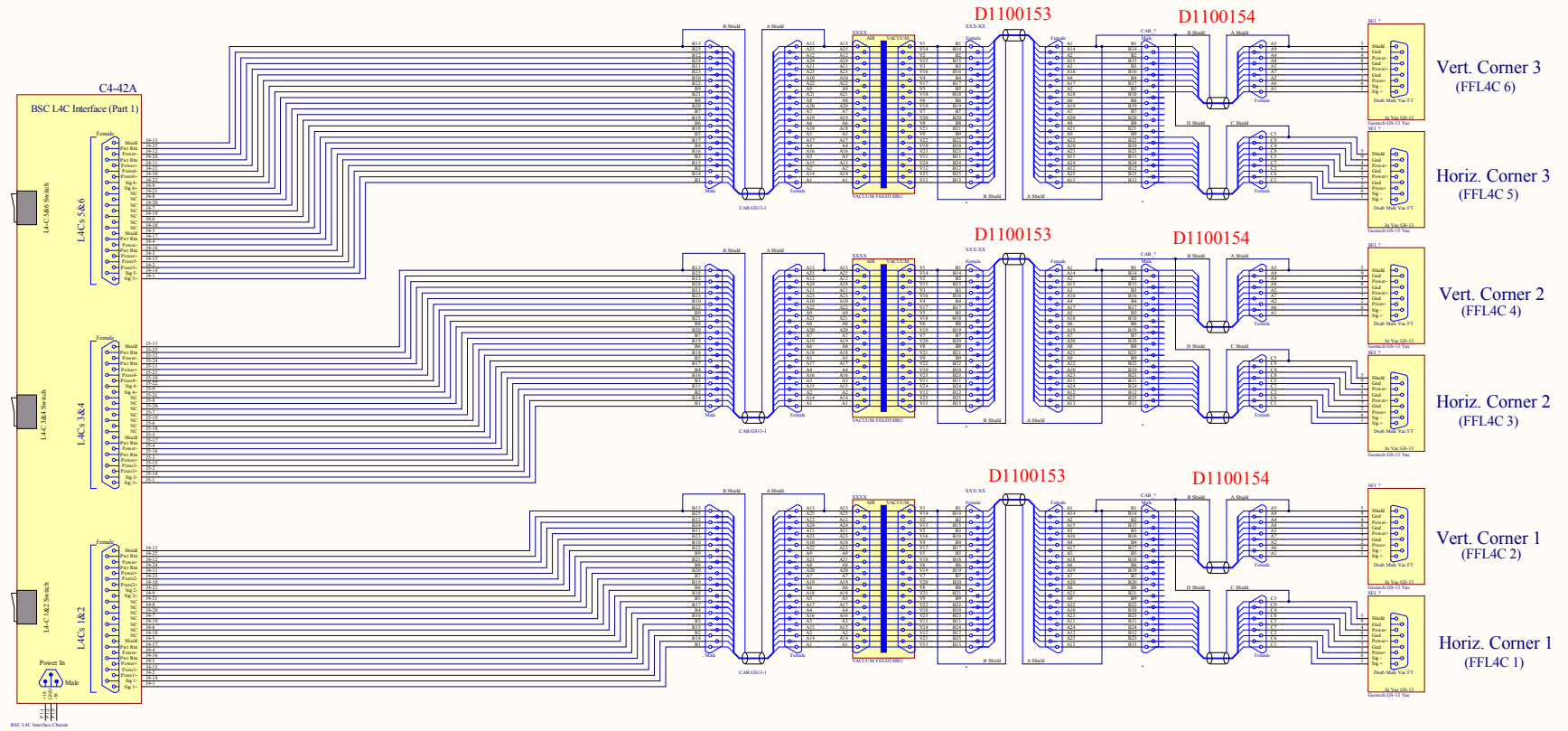


Instrument Corner 3

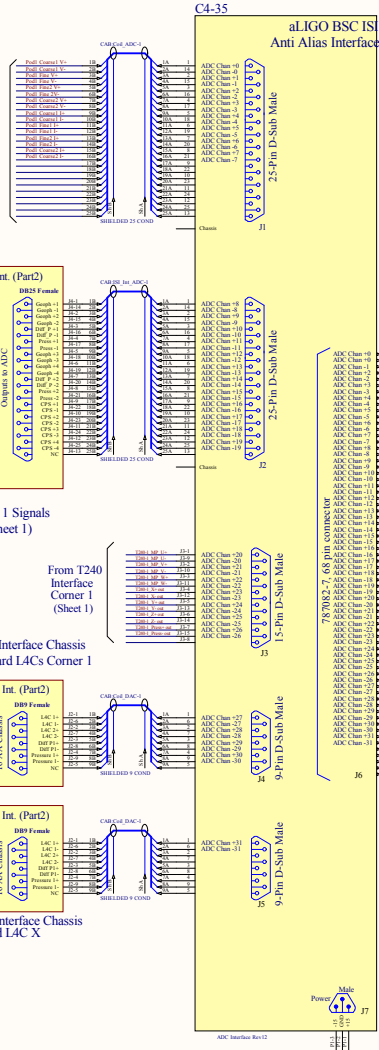


L4C Feed Forward Geophones

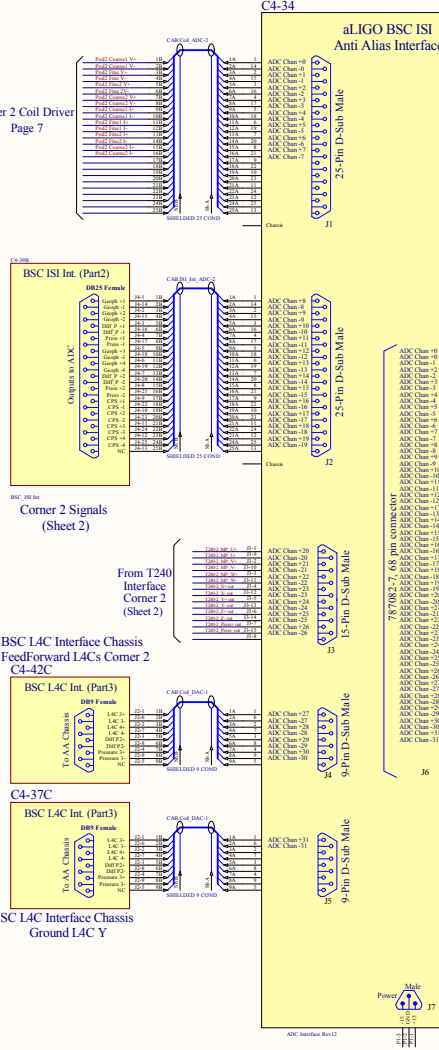
Red cables have not been ordered yet.



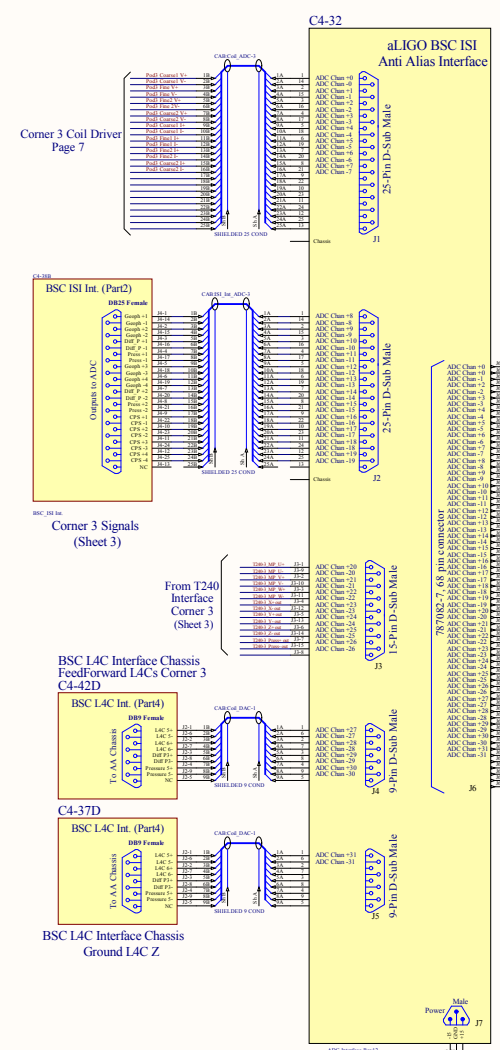
Corner 1 Coil Driver
Page 7

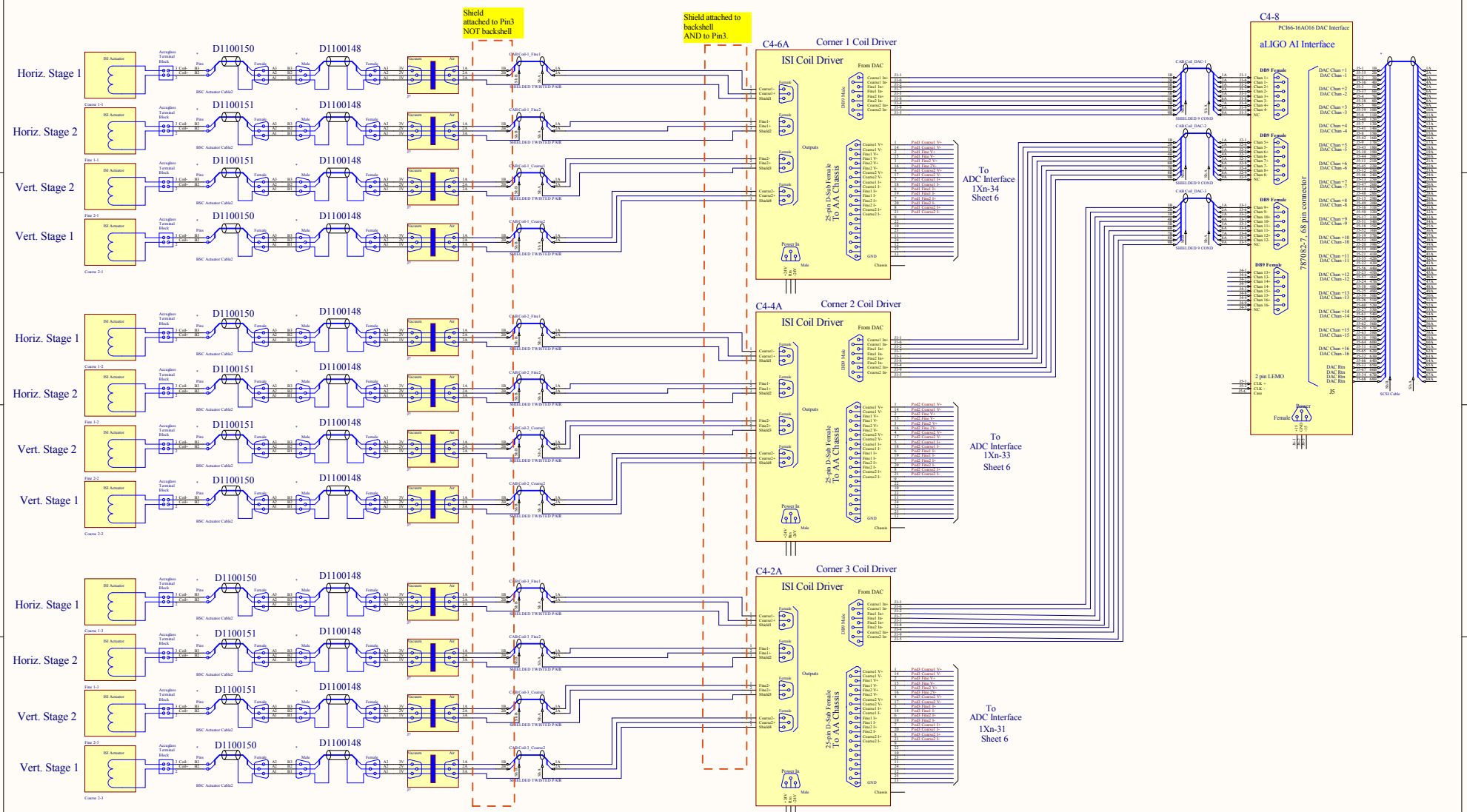


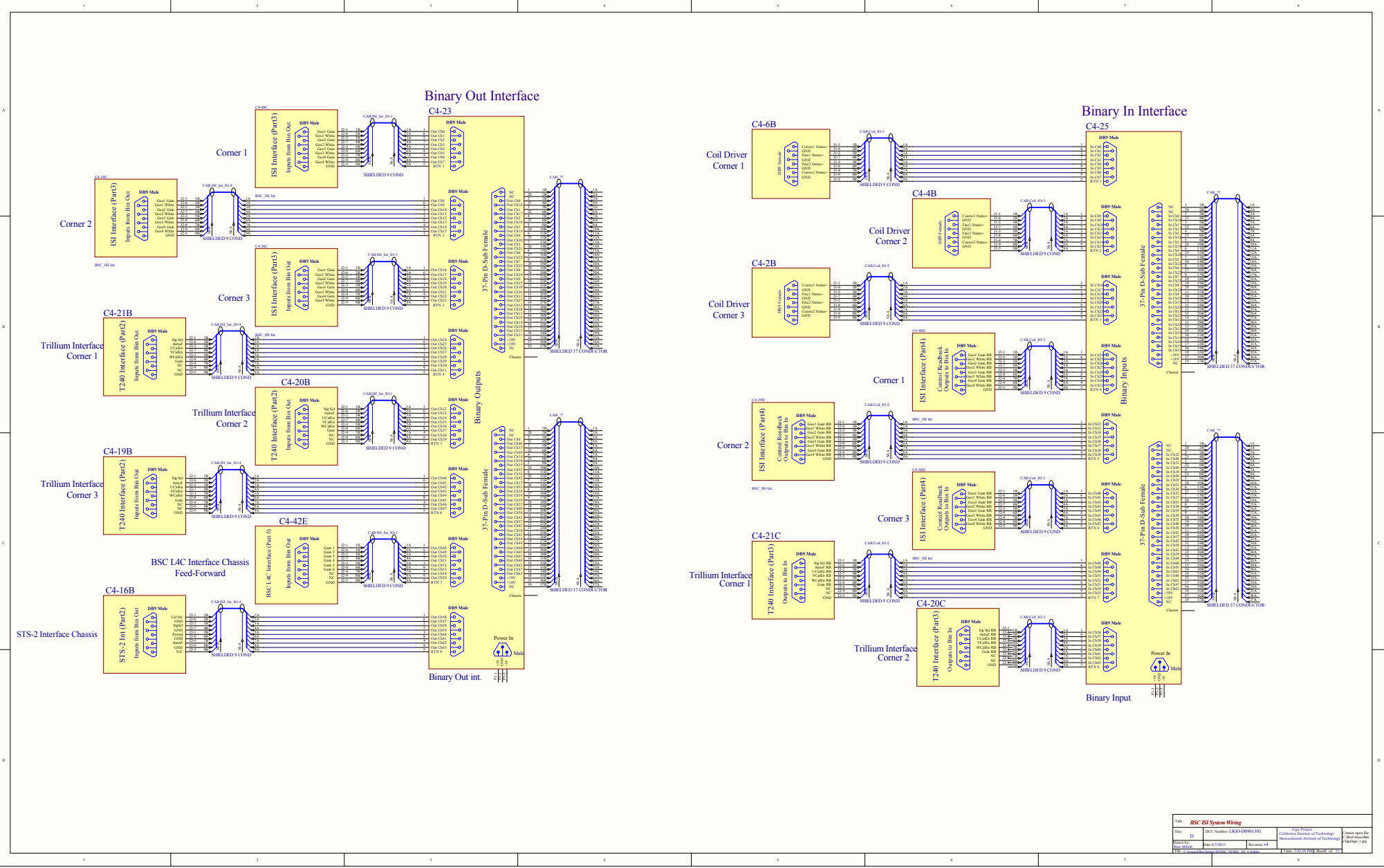
Corner 2 Coil Driver
Page 7



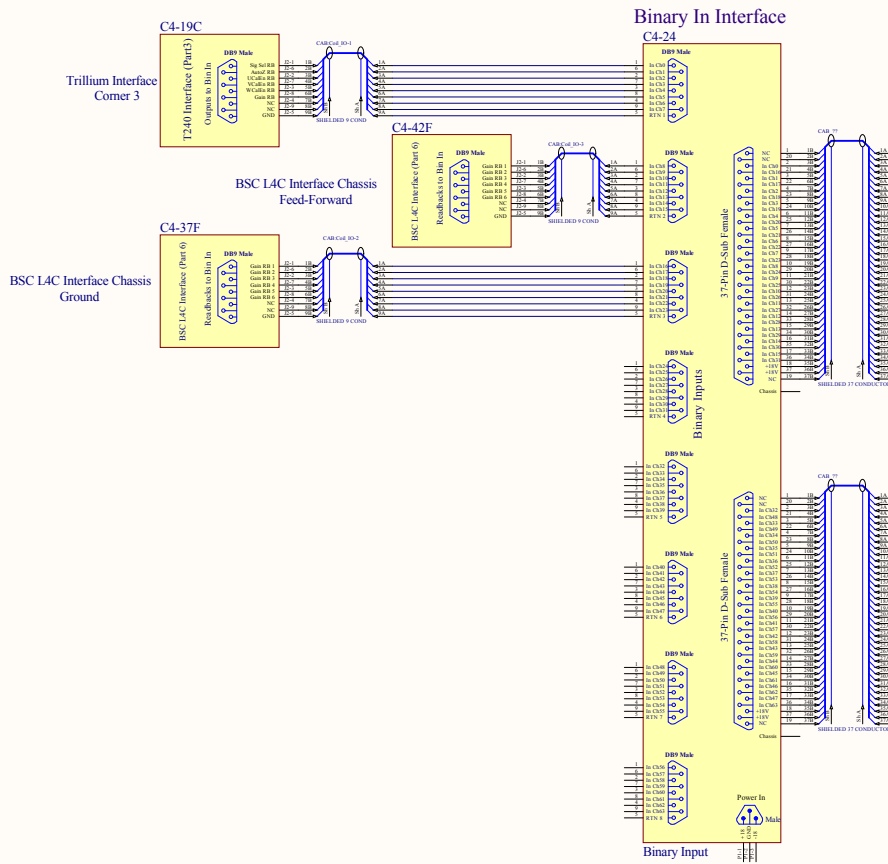
Corner 3 Coil Driver
Page 7

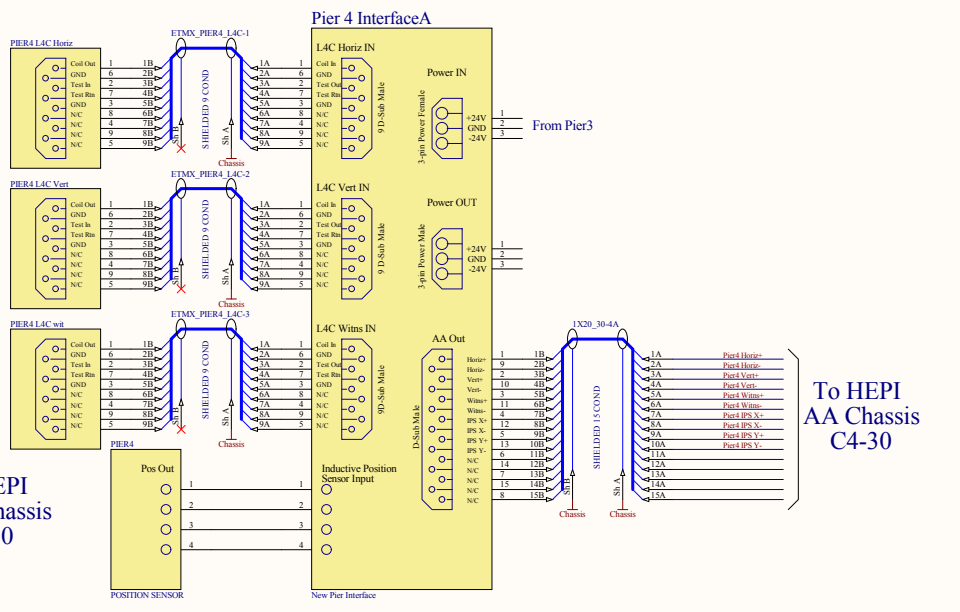
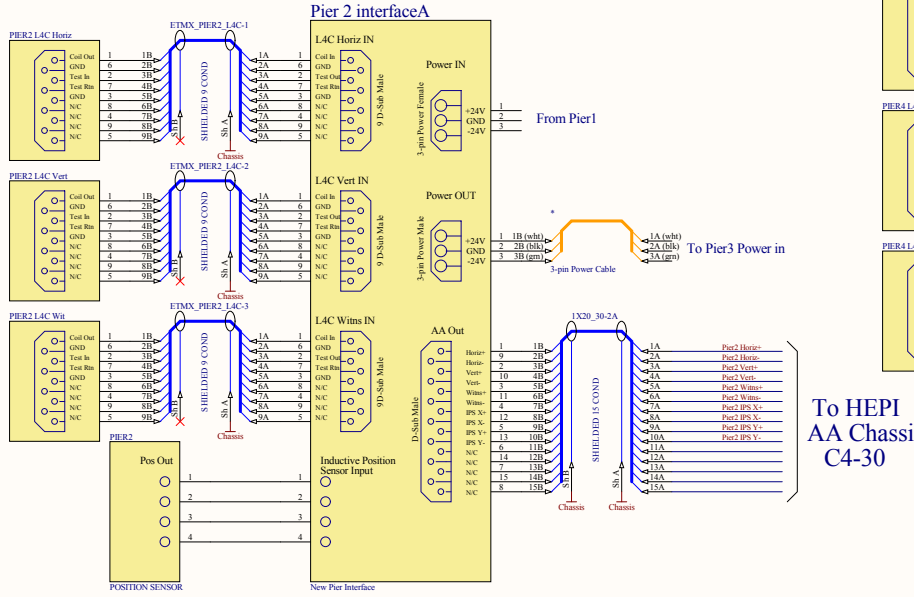
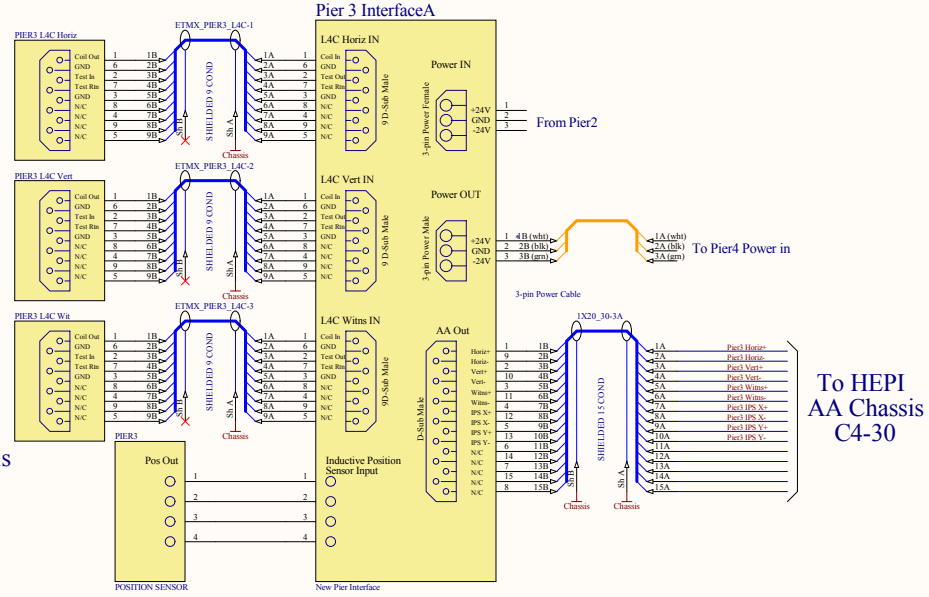
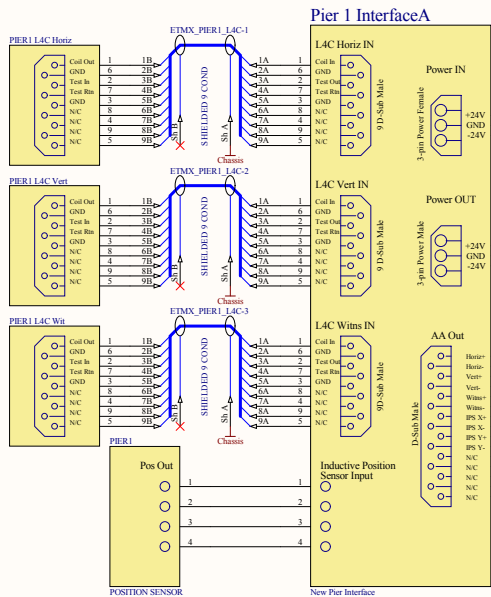




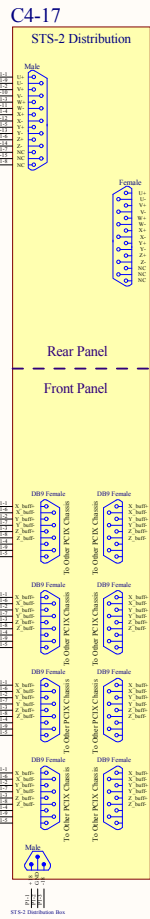
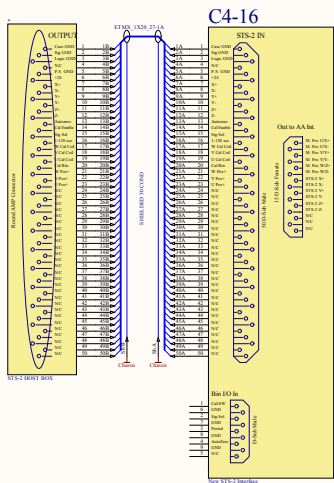


ASC X3 System Wiring			
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D:		Rev: 1	Customer: Institute of Technology
Rev:	1	Rev: 1	Manufacturer: Institute of Technology
Rev:	1	Rev: 1	Rev: 1





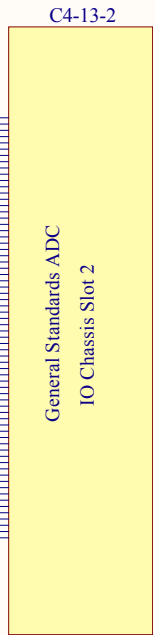
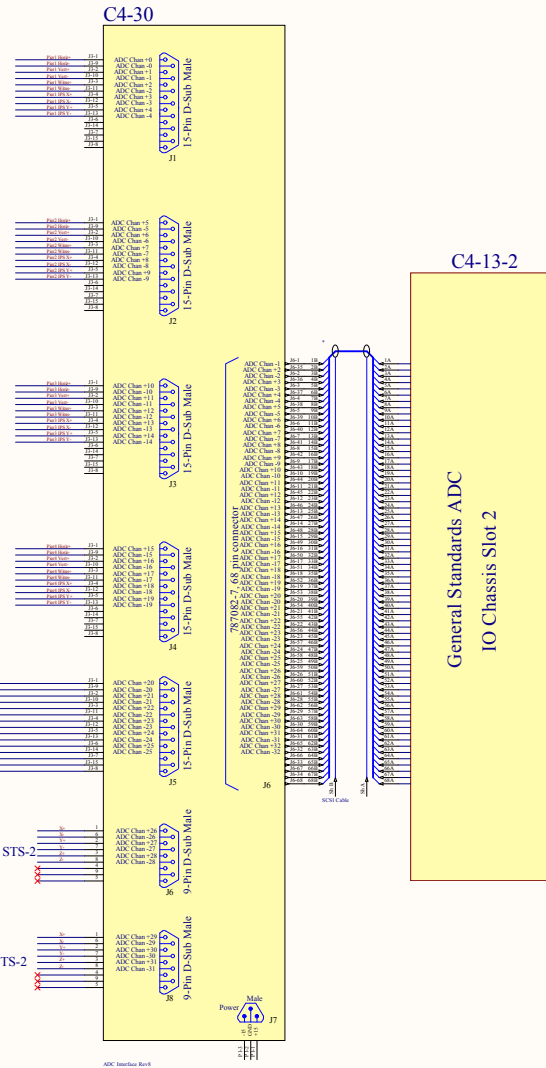
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Drawn by:	Ben Abbott	Date:	6/3/2011
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		Ligo Project California Institute of Technology Massachusetts Institute of Technology	
		Cannot open file C:\Ben\misc\lan \ylog11.jpg	
		Time: 5:02:56 PM Sheet 10 of 13	



These signals go
To the HAM ISI
Spare ADC Inputs

These signals go
To the other 2
BSC ADC Inputs
Like these:

These signals go
To the HAM ISI
Spare ADC Inputs

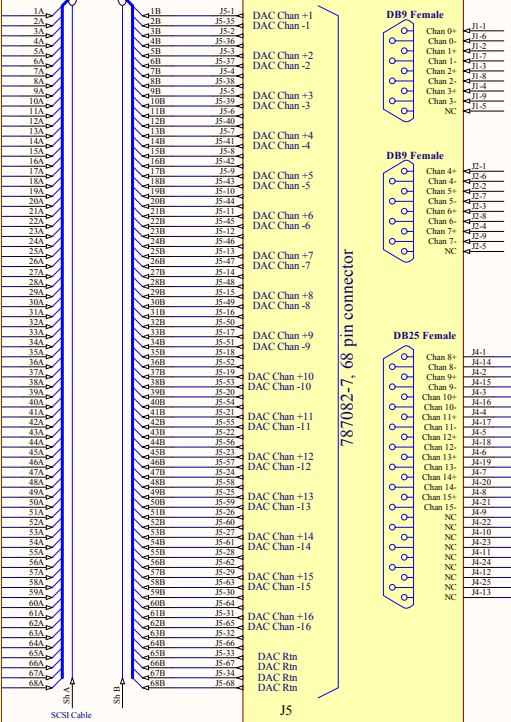


1X1-13-4

IO Chassis Slot 4
General Standards DAC

C4-29

aLIGO HEPI AI Chassis



787082-7, 68 pin connector

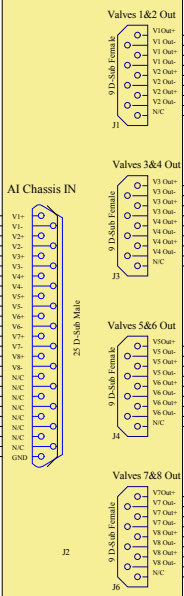


HEPI AI Interface

C4-27

AI Chassis IN

New 8-CH Valve Driver



ETMX_1X20_34-2A

ETMX_1X20_34-3A

ETMX_1X20_34-4A

ETMX_1X20_34-5A

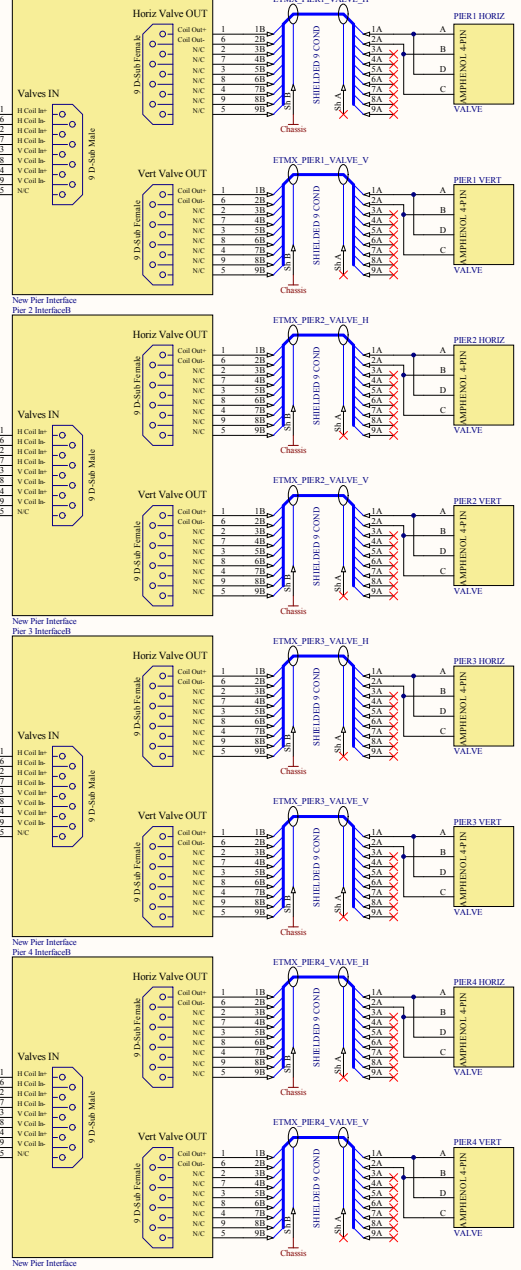
Pier 1 InterfaceB

New Pier Interface
Pier 2 InterfaceC

New Pier Interface
Pier 3 InterfaceB

New Pier Interface
Pier 4 InterfaceB

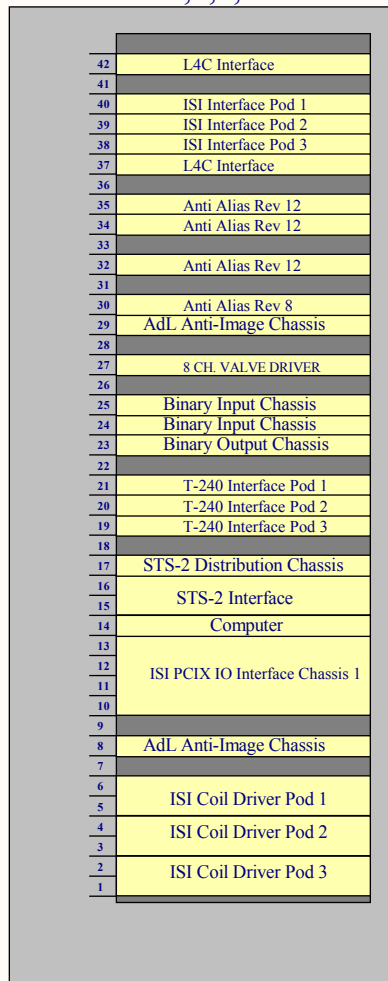
New Pier Interface



Title	aLIGO BSC ISI HEPI System Schematics			
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Drawn by:	Ben Abbott	Date: 6/3/2011	Revision: v4	
File:	C:\renated\Ben\BSC\ISI\BSC_ISIHEPI.schDoc			Time: 5:02:56 PM Sheet 12 of 13

L1-SEI-C4, C5, C6, and Ends
BSC 1,2,3,4&5

BSC AA Chassis = 3
HEPI AA Chassis = 1
HEPI AI Chassis = 1
aLIGO AI Chassis = 1
Filter Boards = 20
Binary In Chassis = 2
Binary Out Chassis = 1



HEPI Components

STS-2 Input /Distribution

Title BSC ISI System Wiring			
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