LIGO Laboratory / LIGO Scientific Collaboration

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UIM Coil Driver Board Test Report

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

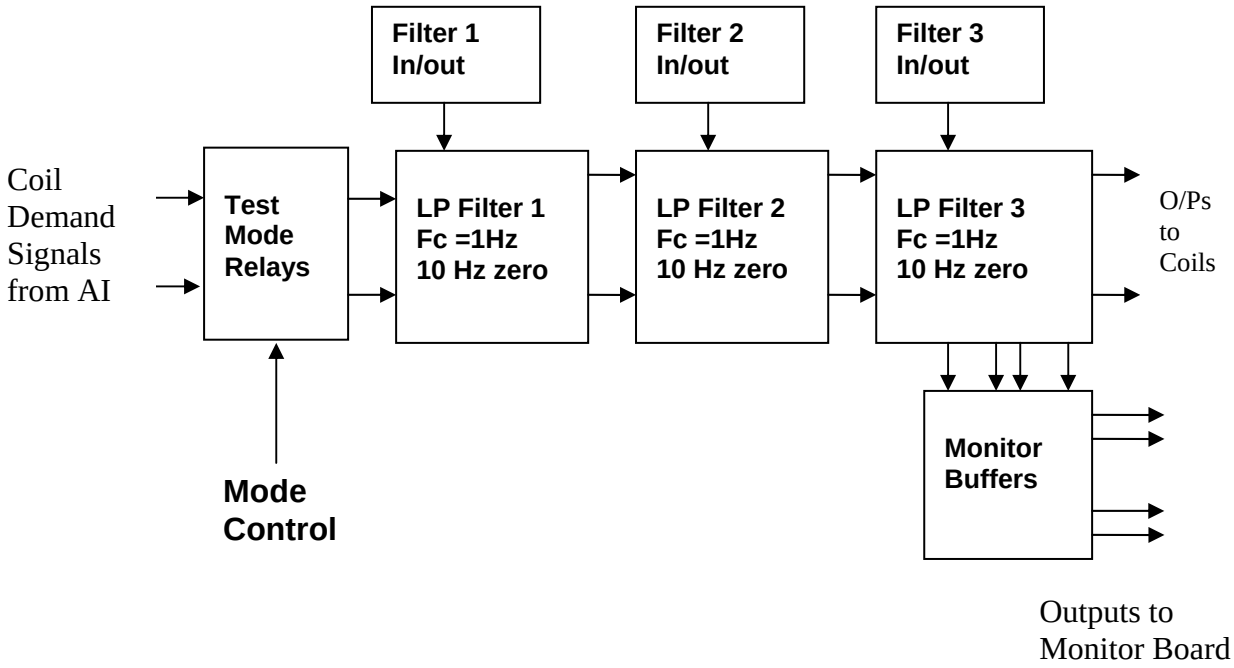

FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM19
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

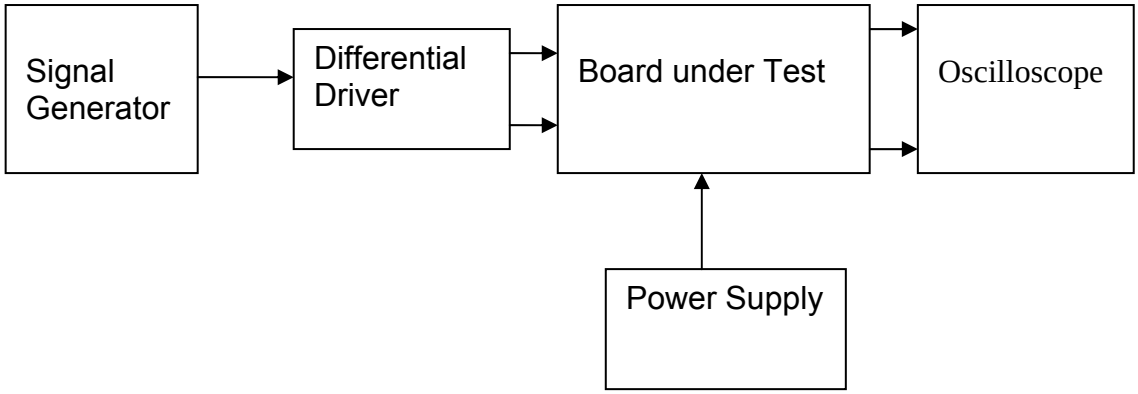
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.01	1mV
+15v	TP4	14.97	1mV
-15v	TP6	14.92	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM19
Test Engineer …….XEN
Date ……14/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.5	3.5	3.5	3.3v to 3.7v	√
Ch2	3.5	3.5	3.5	3.3v to 3.7v	√
Ch3	3.5	3.5	3.5	3.3v to 3.7v	√
Ch4	3.5	3.5	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM19
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9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.1	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.6	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.8	√	2.7	√	2.8	√
5v	13.2	√	13.5	√	13.5	√	13.0	√
7v	18.8	√	19.0	√	18.9	√	19.5	√
10v	26.9	√	27.0	√	27.0	√	26.7	√

Unit……UIM19
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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-104dB	-96dB	758Hz
Channel 2	Channel 1	-102dB	-93dB	1KHz
Channel 2	Channel 3	-102dB	-95dB	1KHz
Channel 3	Channel 2	-102dB	-95dB	933Hz
Channel 3	Channel 4	-101dB	-95dB	933Hz
Channel 4	Channel 3	-100dB	-95dB	1KHz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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UIM COIL DRIVER BOARD
TEST REPORT

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

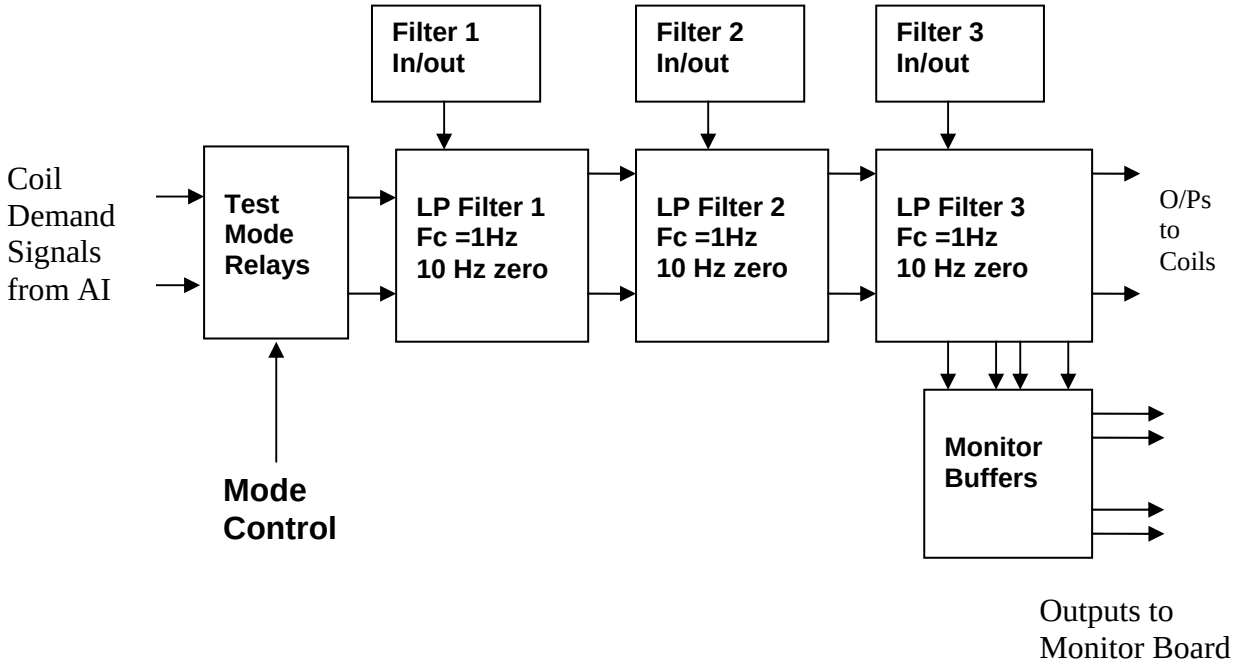


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	**FLUKE**	**115**
V/C calibrator	**TIME ELECTRONICS**	**1044**
Signal Generator	**Agilent**	**332504**
Oscilloscope	**Iso Tech**	**ISR622**
PSU	**Farnell**	**LR39-2**
PSU	**Farnell**	**LR39-2**

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

4. Continuity Checks

Use a multi-meter to check the connections below exist

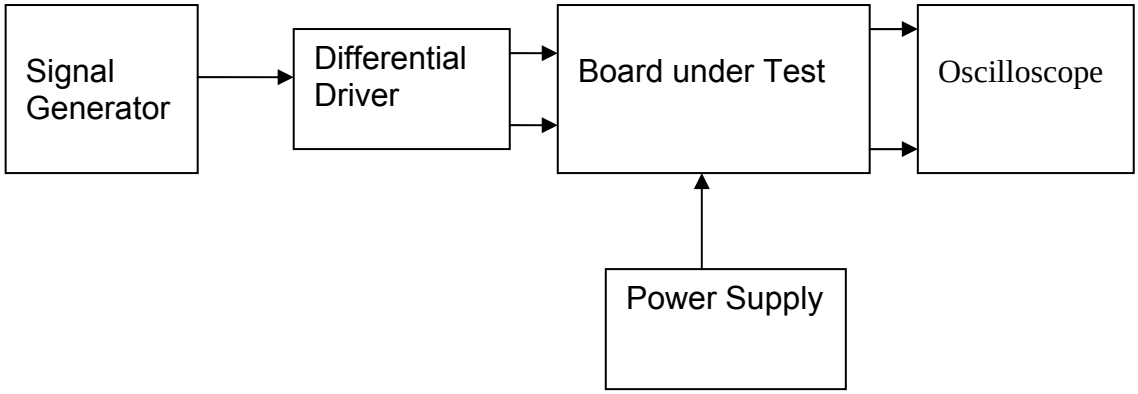
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.05	1mV
+15v	TP4	14.93	1mV
-15v	TP6	-15.02	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	275 mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On?

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	**LED Operation**					
	Filter 1		**Filter 2**		**Filter 2**	
	ON	**OFF**	**ON**	**OFF**	**ON**	**OFF**
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**29/7/09**

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.8	4.8	4.8v to 5v	√
Ch2	4.8	4.8	4.8	4.8v to 5v	√
Ch3	4.9	5.0	5.0	4.8v to 5v	√
Ch4	4.8	4.9	4.9	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	4.9	4.9	4.9	4.9 to 5.1v	√
Ch2	4.9	4.9	4.9	4.9 to 5.1v	√
Ch3	4.9	4.9	4.9	4.9 to 5.1v	√
Ch4	4.9	4.9	4.9	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**30/7/09**

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	4.9	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.6	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	4.9	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.7	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.7	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.7	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27	√	-26.9	√	26.9	√	-27	√
-7v	-19	√	-18.9	√	-18.7	√	-19	√
-5v	-13.5	√	-13.5	√	-13.3	√	-13.5	√
-1v	-2.8	√	-2.6	√	-2.6	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.7	√	2.7	√	2.6	√
5v	13.0	√	13.5	√	13.5	√	13.0	√
7v	18.5	√	18.9	√	18.9	√	18.5	√
10v	26.5	√	27	√	26.9	√	26.9	√

Unit……**UIM1**
Test Engineer ……**XEN**
Date ……**30/7/09**

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-101	-101	Flat
Channel 2	Channel 1	-101	-92	1KHz
Channel 2	Channel 3	-101	-98	269Hz
Channel 3	Channel 2	-101	-98	467Hz
Channel 3	Channel 4	-101	-99	407Hz
Channel 4	Channel 3	-101	-97	154Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……**UIM2**
Test Engineer …….**RMC**
Date ……**22/3/11**

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

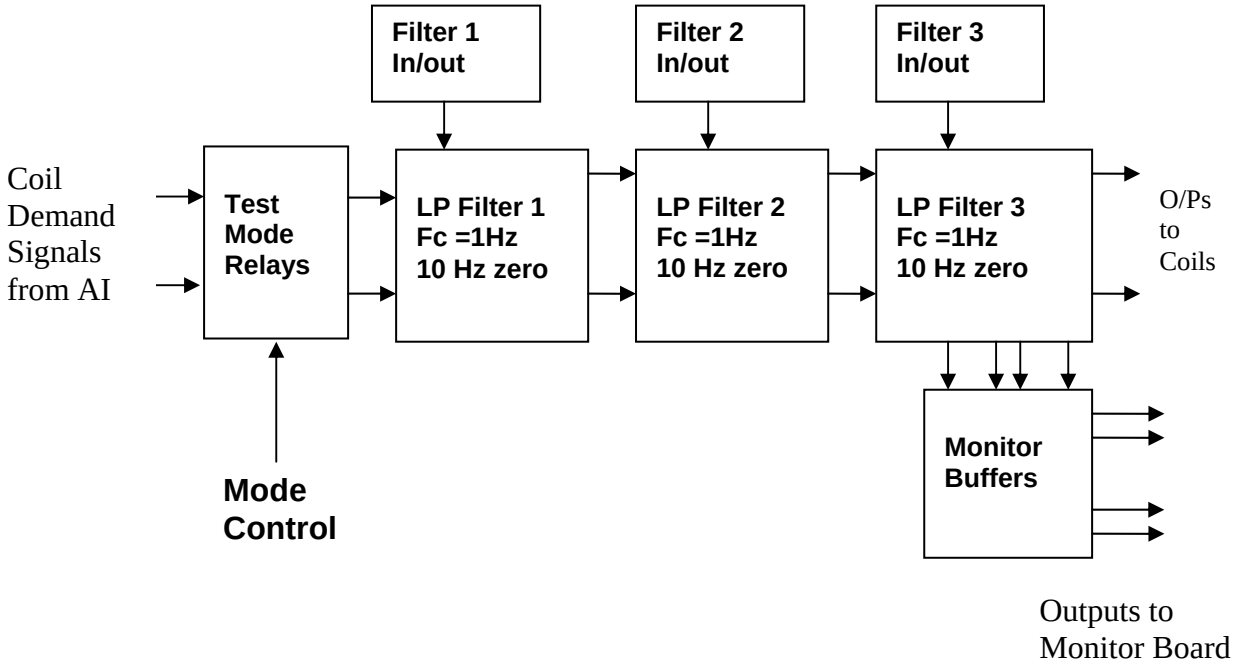


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	**FLUKE**	**115**
V/C calibrator	**TIME ELECTRONICS**	**1044**
Signal Generator	**Agilent**	**332504**
Oscilloscope	**Iso Tech**	**ISR622**
PSU	**Farnell**	**LR39-2**
PSU	**Farnell**	**LR39-2**

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

4. Continuity Checks

Use a multi-meter to check the connections below exist

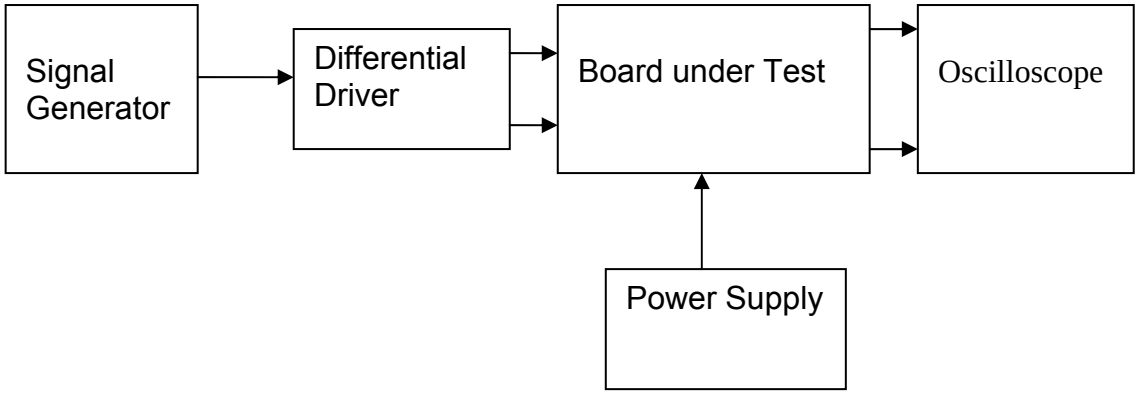
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.01	1mV
+15v	TP4	14.91	1mV
-15v	TP6	-14.92	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mV
-16.5v	200mV

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	**LED Operation**					
	Filter 1		**Filter 2**		**Filter 2**	
	ON	**OFF**	**ON**	**OFF**	**ON**	**OFF**
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……**UIM2**
Test Engineer ……**XEN**
Date ……**30/7/09**

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	4.8v to 5v	√
Ch2	4.8	4.9	4.9	4.8v to 5v	√
Ch3	4.8	4.9	4.9	4.8v to 5v	√
Ch4	4.8	4.9	4.9	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……**UIM2**
Test Engineer ……**XEN**
Date ……**30/7/09**

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.7	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.7	√	-26.5	√	-27.0	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.7	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.7	√	2.8	√	2.7	√
5v	13.0	√	13.0	√	13.5	√	13.3	√
7v	18.5	√	18.5	√	19.0	√	18.9	√
10v	26.5	√	26.9	√	27.0	√	27.0	√

Unit……**UIM2**
Test Engineer …….**XEN**
Date ……**30/7/09**

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-96.2dB	917Hz
Channel 2	Channel 1	-102dB	-93.9dB	870Hz
Channel 2	Channel 3	-102dB	-95.7dB	1KHz
Channel 3	Channel 2	-101dB	-96.4dB	933Hz
Channel 3	Channel 4	-101dB	-96.1dB	812Hz
Channel 4	Channel 3	-101dB	-96.9dB	501Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

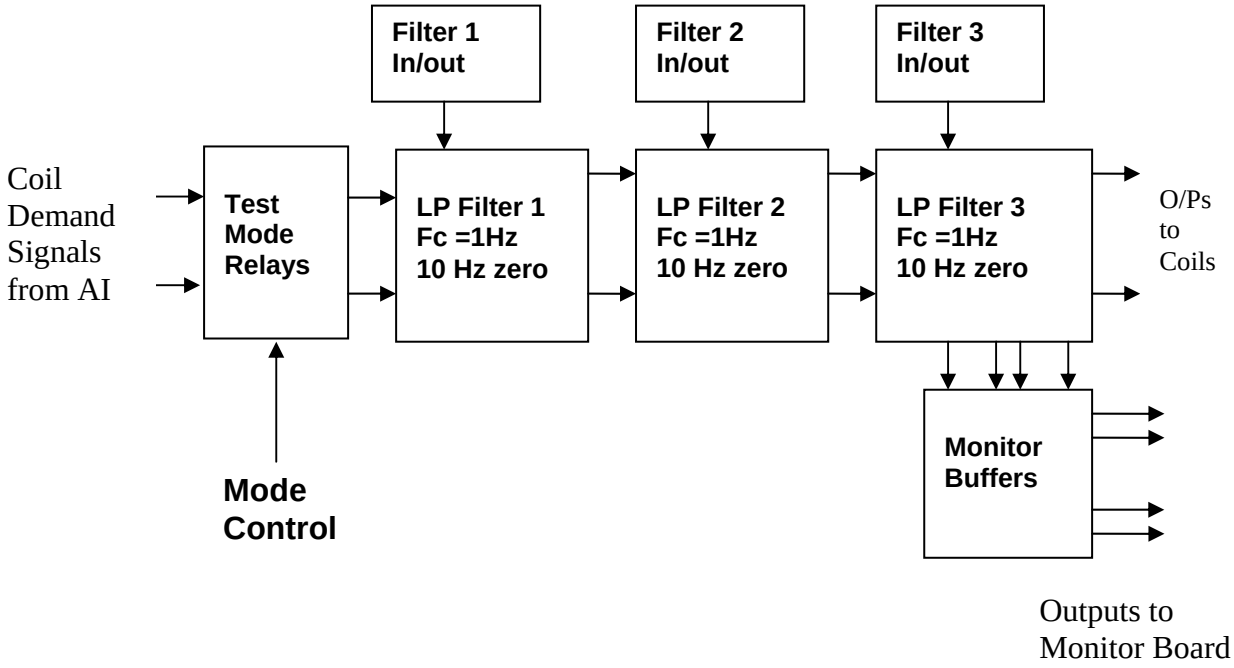


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

4. Continuity Checks

Use a multi-meter to check the connections below exist

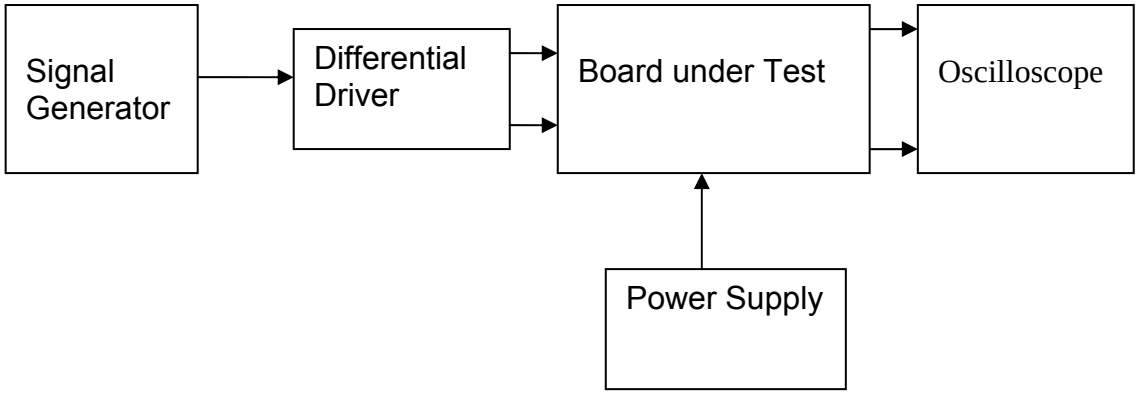
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.04	1mV
+15v	TP4	14.79	1mV
-15v	TP6	-15.01	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	260mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	4.8v to 5v	√
Ch2	4.9	4.9	4.9	4.8v to 5v	√
Ch3	4.8	4.9	4.9	4.8v to 5v	√
Ch4	4.8	4.9	4.9	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	**1.65**	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	**1.7**	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	**1.65**	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	**1.7**	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	**-26.9**	√	**-26.9**	√	**-27.0**	√	**-27.0**	√
-7v	**-18.9**	√	**-18.9**	√	**-18.9**	√	**-18.9**	√
-5v	**-13.5**	√	**-13.5**	√	**-13.5**	√	**-13.5**	√
-1v	**-2.8**	√	**-2.7**	√	**-2.8**	√	**-2.7**	√
0v	**0**	√	**0**	√	**0**	√	**0**	√
1v	**2.6**	√	**2.8**	√	**2.6**	√	**2.8**	√
5v	**13.5**	√	**13.5**	√	**13.0**	√	**13.5**	√
7v	**18.9**	√	**19.0**	√	**18.5**	√	**18.9**	√
10v	**26.9**	√	**27.0**	√	**26.5**	√	**26.9**	√

Unit……...UIM3
Test Engineer ……XEN
Date ……31/7/09

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	**-101dB**	**93.3dB**	**933 Hz**
Channel 2	Channel 1	**-101dB**	**96.1dB**	**901Hz**
Channel 2	Channel 3	**-101dB**	**93.4dB**	**949Hz**
Channel 3	Channel 2	**-101dB**	**94.4dB**	**812Hz**
Channel 3	Channel 4	**-100dB**	**93.2dB**	**707Hz**
Channel 4	Channel 3	**-100dB**	**91.6dB**	**91.6Hz**

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

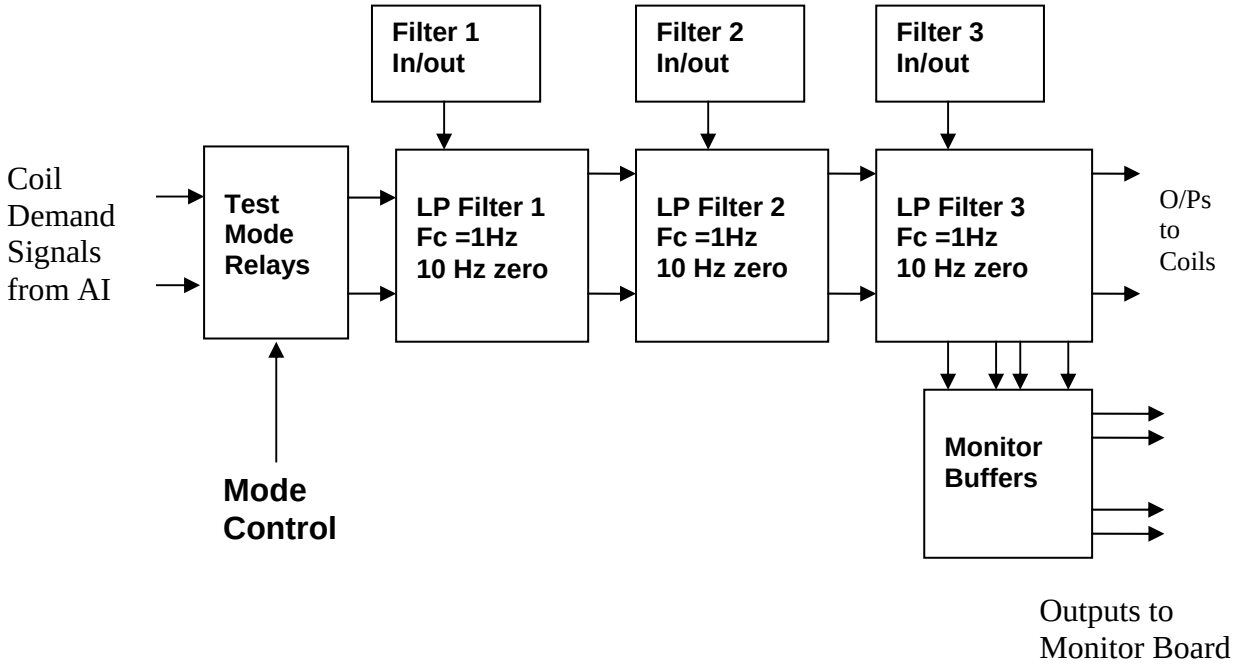


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

4. Continuity Checks

Use a multi-meter to check the connections below exist

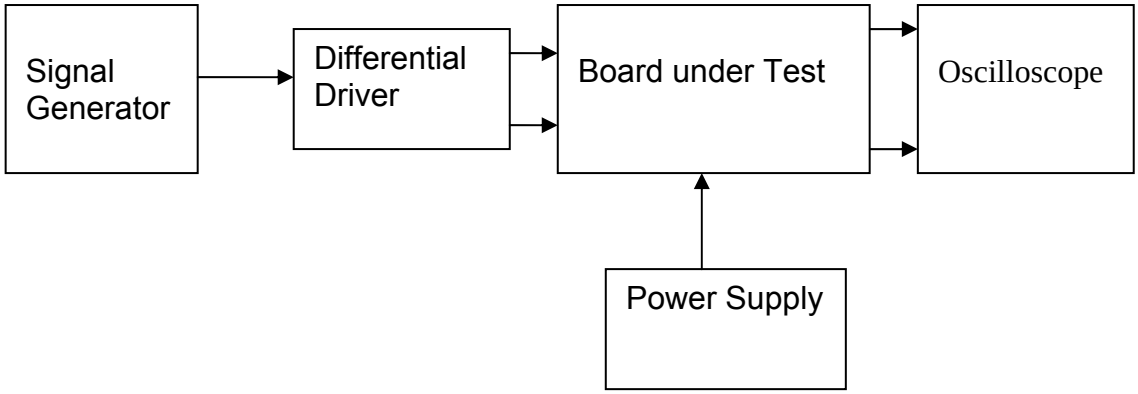
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	11.97	1mV
+15v	TP4	14.88	1mV
-15v	TP6	-14.9	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	260mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	4.9	4.9	4.8v to 5v	√
Ch2	4.8	4.9	4.9	4.8v to 5v	√
Ch3	4.8	4.9	4.9	4.8v to 5v	√
Ch4	4.8	4.9	4.9	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM4
Test Engineer ……XEN
Date ……31/7/09

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	**1.65**	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	**1.65**	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	**1.65**	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	**5.0**	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	**1.65**	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.5	√	-27.0	√	-27.1	√	-26.9	√
-7v	-19.0	√	-19.0	√	-19.1	√	-18.9	√
-5v	-13.9	√	-13.5	√	-13.9	√	-13.5	√
-1v	-2.9	√	-2.7	√	-2.9	√	-2.7	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.8	√	2.6	√	2.8	√
5v	13.0	√	13.2	√	13.1	√	13.5	√
7v	18.2	√	18.5	√	18.5	√	18.0	√
10v	26.5	√	26.5	√	26.5	√	26.9	√

Unit……UIM4
Test Engineer ……XEN
Date ……3/8/09

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-95.2dB	707Hz
Channel 2	Channel 1	-101dB	-94.0dB	616Hz
Channel 2	Channel 3	-101dB	-94.3dB	436Hz
Channel 3	Channel 2	-101dB	-95.8dB	870Hz
Channel 3	Channel 4	-101dB	-94.6dB	812Hz
Channel 4	Channel 3	-101dB	-94.7dB	1KHz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

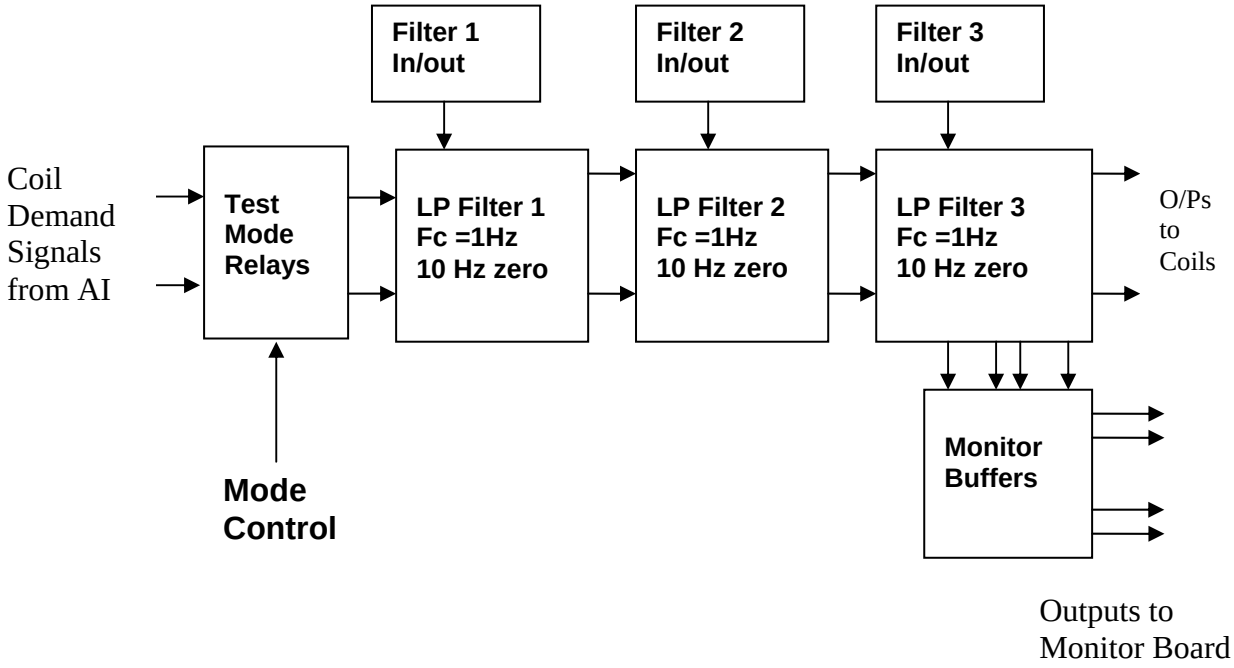


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

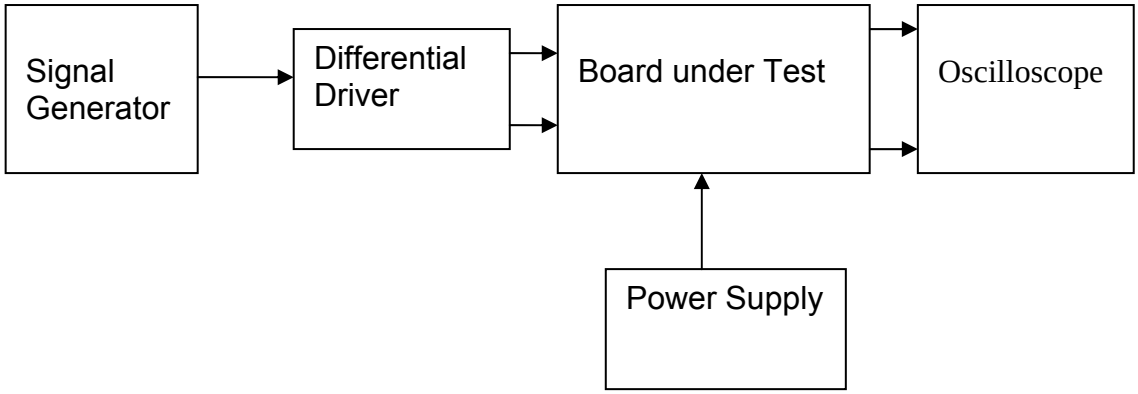
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	11.98	
+15v	TP4	14.79	
-15v	TP6	-14.95	

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	225 mA
-16.5v	200 mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……
Test Engineer ……
Date ……

9. Monitor Outputs

Switch out the filters.

With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.0	√
-7v	-19.0	√	-18.9	√	-19.0	√	-18.9	√
-5v	-13.5	√	-13.5	√	-13.7	√	-13.5	√
-1v	-2.8	√	-2.6	√	-2.8	√	-2.7	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	3.0	√	2.7	√	2.8	√
5v	13.5	√	14.0	√	13.2	√	13.5	√
7v	19.0	√	19.1	√	18.9	√	19.0	√
10v	27.0	√	27.1	√	26.9	√	27.0	√

Unit……..UIM5
Test Engineer ……XEN
Date ……3/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-104dB	-94.6dB	812Hz
Channel 2	Channel 1	-102dB	-94.6dB	436Hz
Channel 2	Channel 3	-101dB	-94.8dB	707Hz
Channel 3	Channel 2	-101dB	-94.5dB	467Hz
Channel 3	Channel 4	-101dB	-96.5dB	917Hz
Channel 4	Channel 3	-101dB	-92.7dB	155Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

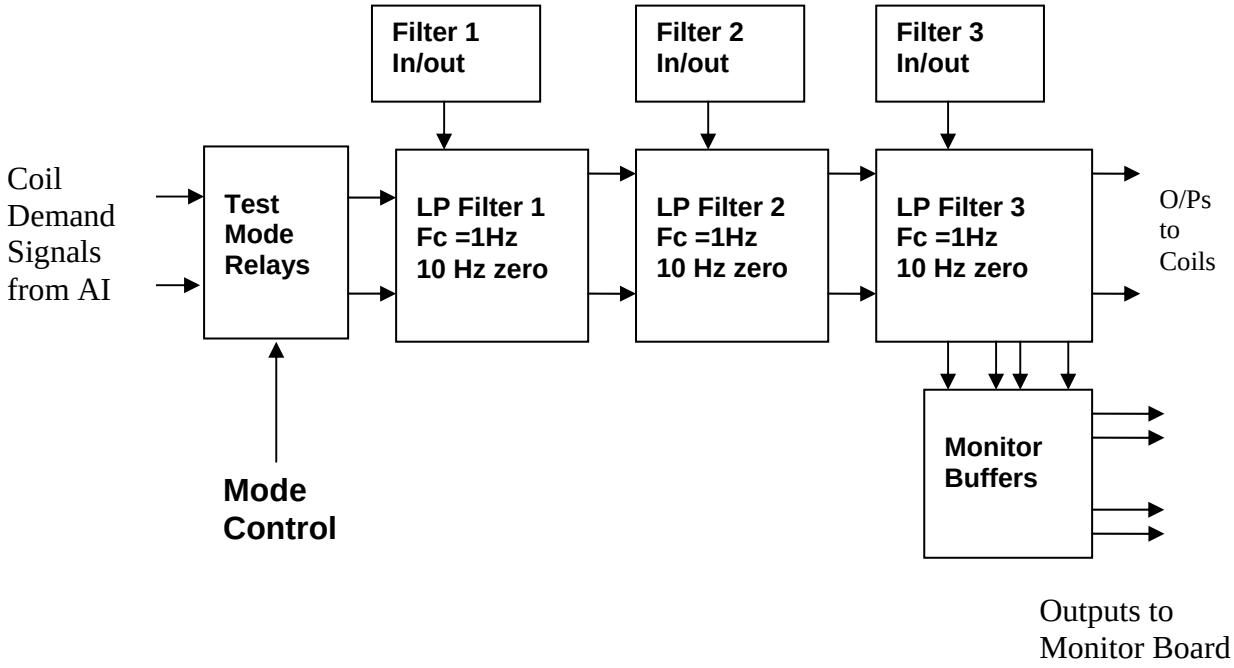


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

A solder joint on C104 Ch2 not soldered. Re-soldered.

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

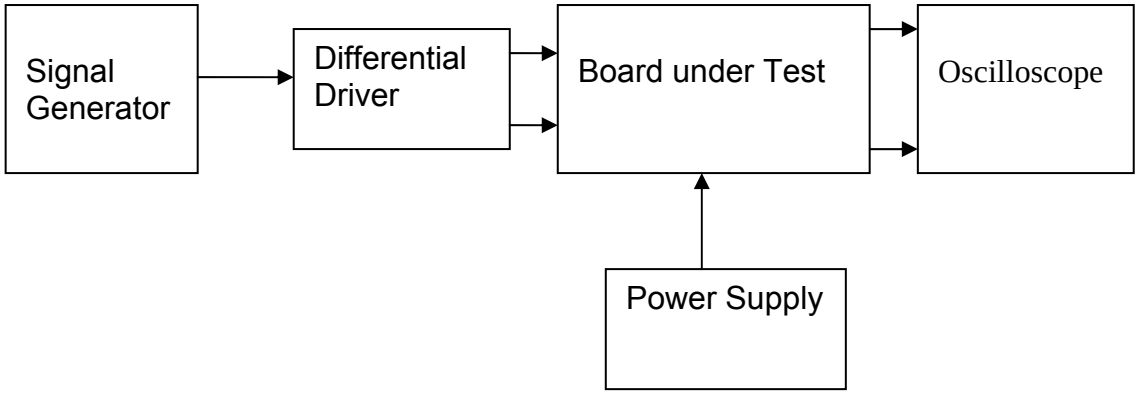
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.08	1mV
+15v	TP4	14.95	1mV
-15v	TP6	-15.04	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270 mA
-16.5v	200 mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.9 to 5.1v	√
Ch2	4.8	5.0	5.0	4.9 to 5.1v	√
Ch3	4.8	5.0	5.0	4.9 to 5.1v	√
Ch4	4.8	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.3	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.3	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.9	√	-27.0	√	-27.4	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.1	√	-18.9	√
-5v	-13.5	√	-13.5	√	-13.9	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.9	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.8	√	2.7	√	2.9	√
5v	13.0	√	13.5	√	13.1	√	13.5	√
7v	18.5	√	19.0	√	18.9	√	19.0	√
10v	26.9	√	27.0	√	26.9	√	27.0	√

Unit……UIM6
Test Engineer …….XEN
Date ……4/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-101dB	-93.5dB	144Hz
Channel 2	Channel 1	-101dB	-93.1dB	1KHz
Channel 2	Channel 3	-100dB	-93.3dB	933Hz
Channel 3	Channel 2	-100dB	-93.9dB	807Hz
Channel 3	Channel 4	-100dB	-95.9dB	933Hz
Channel 4	Channel 3	-100dB	-95.3dB	758Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM7
Test Engineer …….XEN
Date ……..4/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

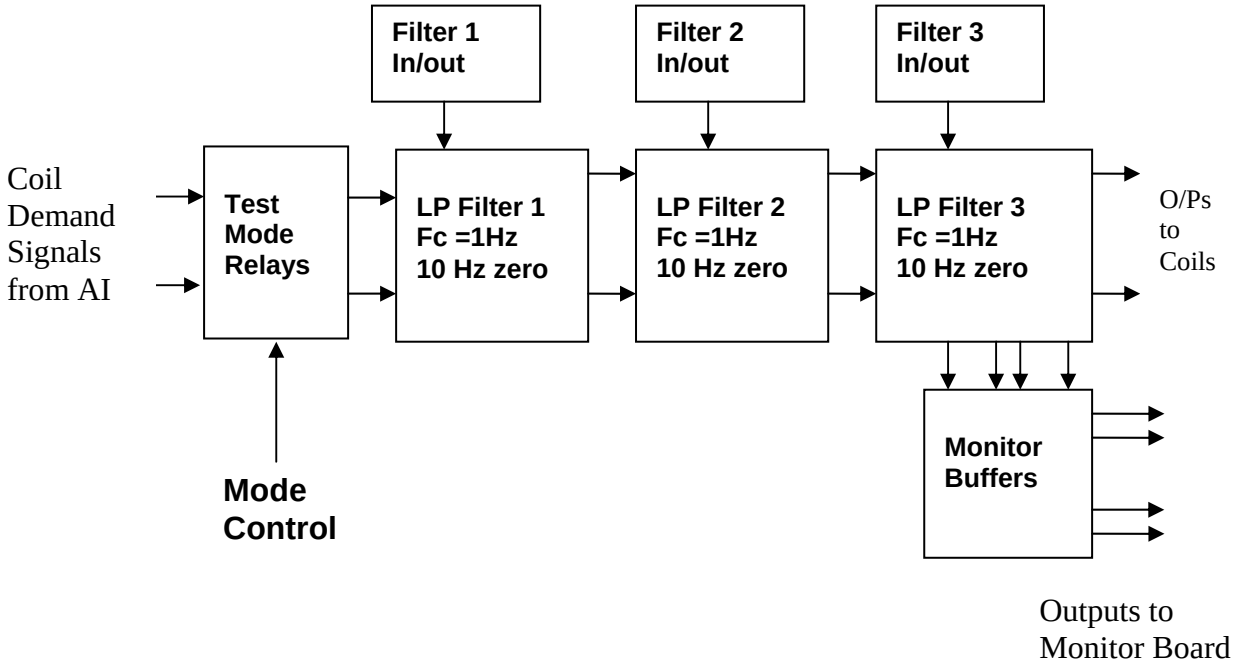

FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM7
Test Engineer …….XEN
Date ……..4/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM7
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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM7
Test Engineer …….XEN
Date ……..4/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

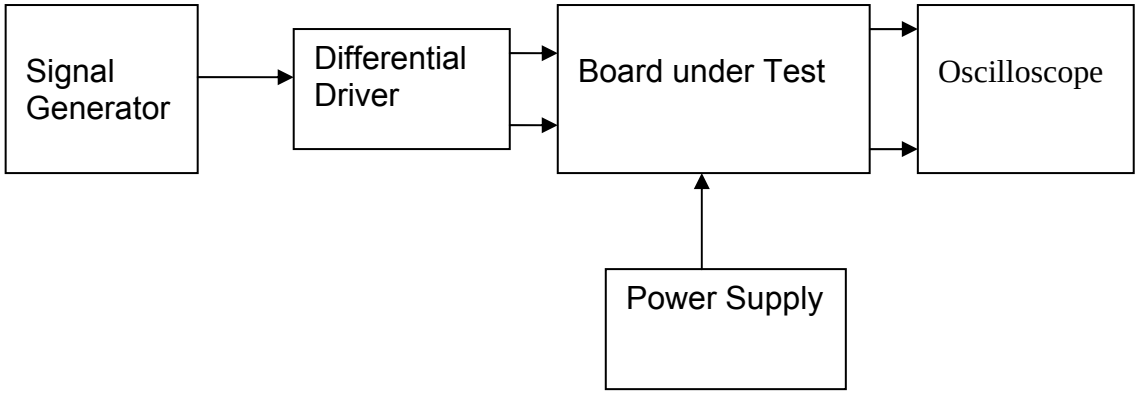
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM7
Test Engineer …….XEN
Date ……..4/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.00	1mV
+15v	TP4	14.94	1mV
-15v	TP6	-14.92	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM7
Test Engineer …….XEN
Date ……..4/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM7
Test Engineer …….XEN
Date ……..5/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM7
Test Engineer …….XEN
Date ……..5/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.0	√
-7v	-19.0	√	-18.9	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.9	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.9	√	-2.7	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	3.0	√	2.7	√	2.9	√
5v	13.5	√	13.9	√	13.5	√	13.5	√
7v	19.0	√	19.1	√	18.5	√	19.0	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIM7
Test Engineer …….XEN
Date ……..5/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-103dB	-96.8dB	501Hz
Channel 2	Channel 1	-102dB	-94.5dB	870Hz
Channel 2	Channel 3	-101dB	-95.8dB	1KHz
Channel 3	Channel 2	-101dB	-95.6dB	154Hz
Channel 3	Channel 4	-101dB	-92.2dB	1KHz
Channel 4	Channel 3	-101dB	-96.1dB	933Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM8
Test Engineer …….XEN
Date ……5/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

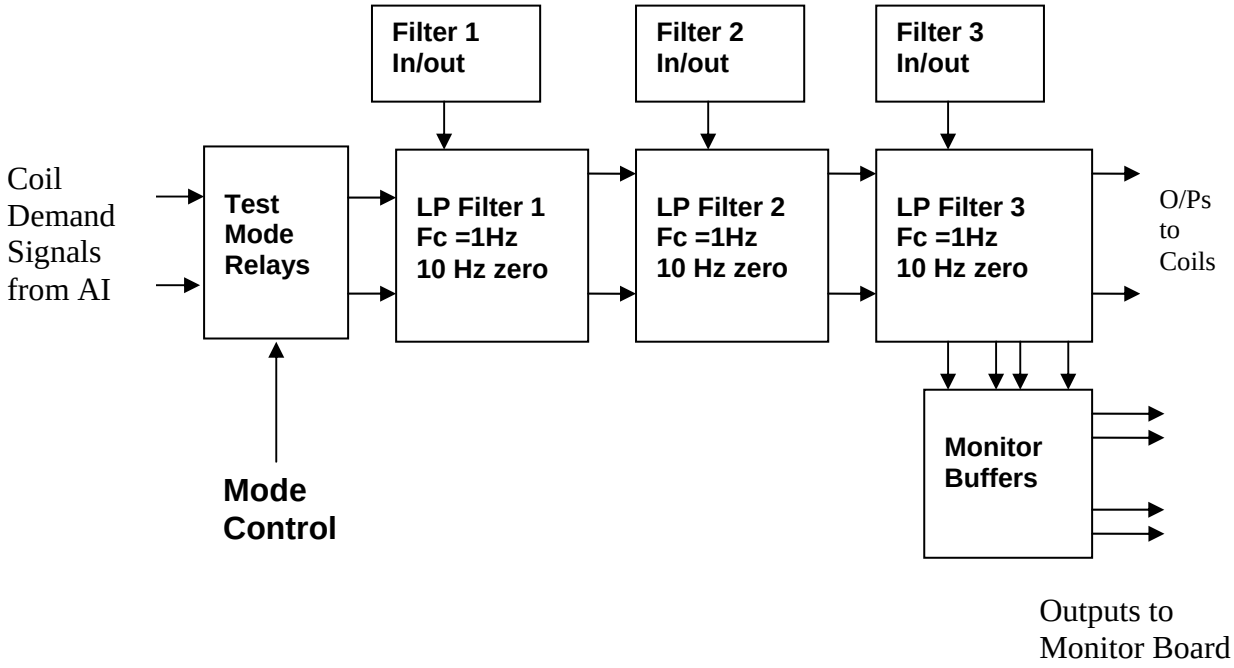

FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

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2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

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4. Continuity Checks

Use a multi-meter to check the connections below exist

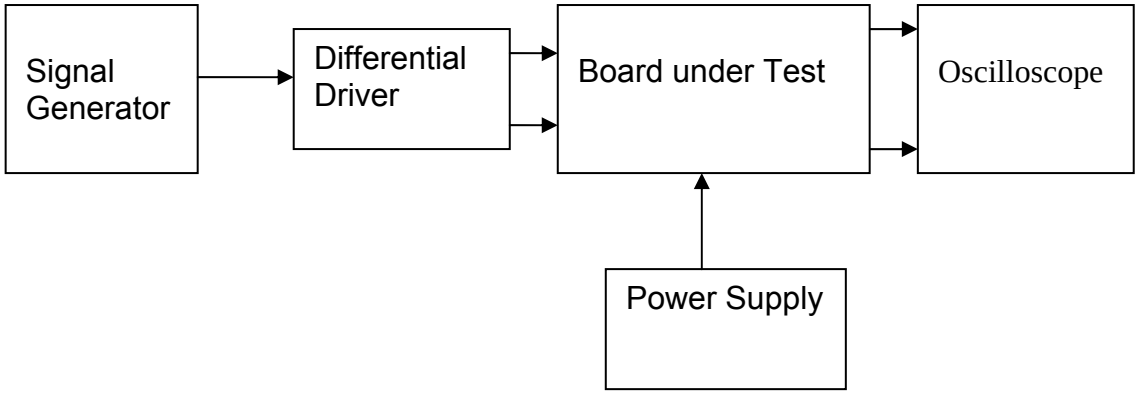
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.06	1mV
+15v	TP4	14.85	1mV
-15v	TP6	-14.96	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

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7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

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9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-26.5	√
-7v	-19.0	√	-18.9	√	-18.9	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.2	√	-13.7	√
-1v	-2.9	√	-2.7	√	-2.7	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	3.0	√	2.6	√	2.6	√
5v	13.2	√	13.9	√	13.2	√	13.5	√
7v	18.9	√	19.0	√	18.5	√	18.7	√
10v	27.0	√	27.0	√	26.9	√	26.9	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-103dB	-96.0dB	771Hz
Channel 2	Channel 1	-101dB	-92.7dB	870Hz
Channel 2	Channel 3	-100dB	-94.5dB	933Hz
Channel 3	Channel 2	-100dB	-93.5dB	707Hz
Channel 3	Channel 4	-100dB	-96.7dB	475Hz
Channel 4	Channel 3	-100dB	-94.7dB	436Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM9
Test Engineer …….XEN
Date ……7/8.9

Contents

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The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

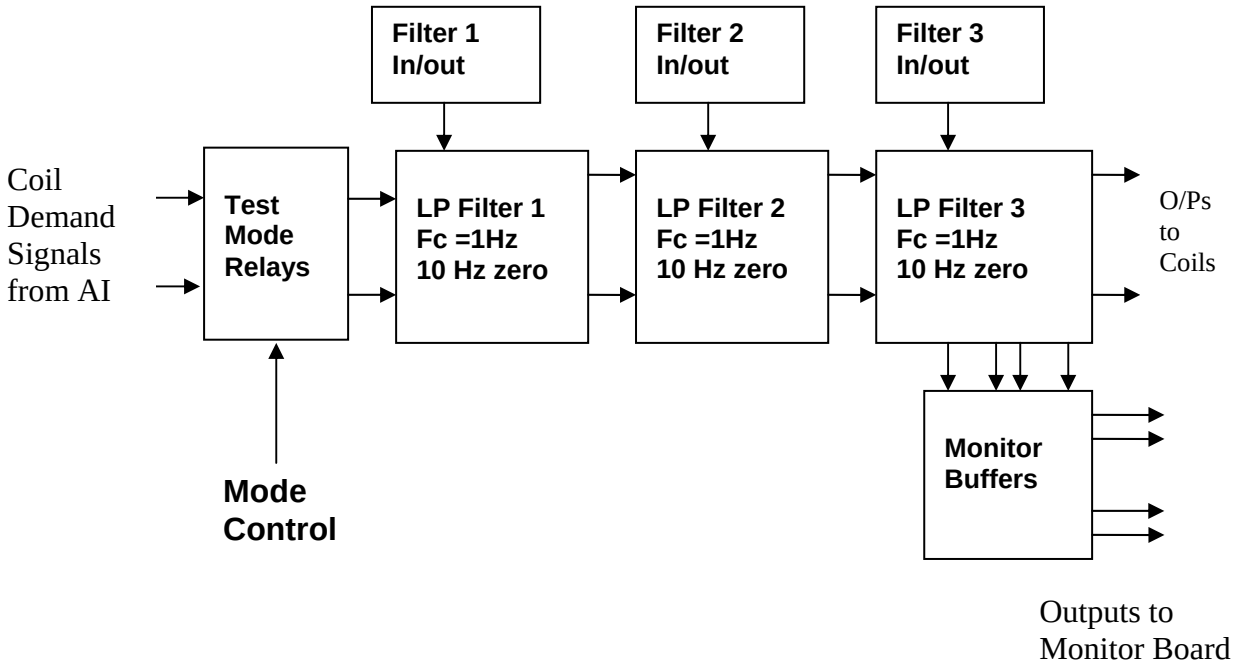

FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

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2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

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4. Continuity Checks

Use a multi-meter to check the connections below exist

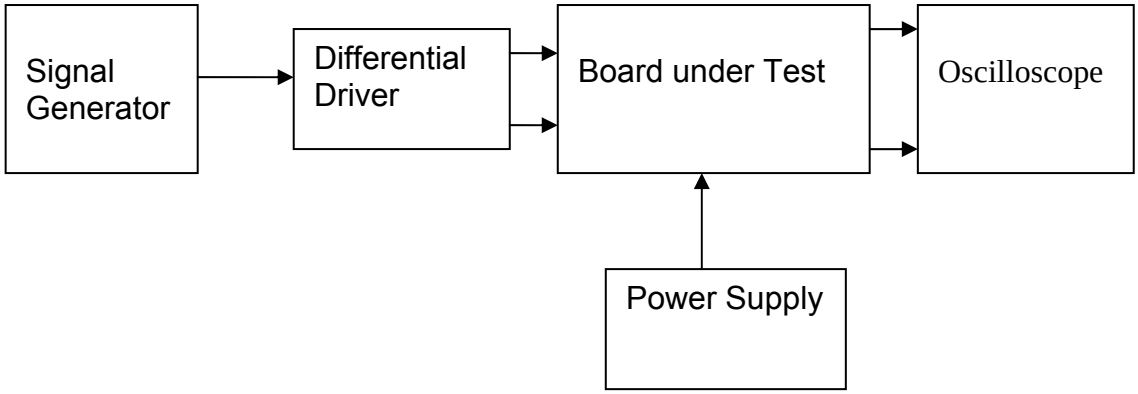
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.08	1mV
+15v	TP4	14.98	1mV
-15v	TP6	-14.92	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

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7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM9
Test Engineer …….XEN
Date ……7/8.9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.9	√	-27.0	√	-27.0	√	-26.5	√
-7v	-19.0	√	-19.5	√	-19.5	√	-19.0	√
-5v	-13.5	√	-14.0	√	-14.0	√	-13.6	√
-1v	-2.8	√	-3.0	√	-3.0	√	-2.9	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.6	√	2.7	√	2.6	√
5v	13.5	√	13.0	√	13.0	√	13.5	√
7v	18.9	√	18.9	√	18.7	√	18.9	√
10v	27.0	√	26.9	√	26.9	√	27.0	√

Unit……UIM9
Test Engineer …….XEN
Date ……7/8.9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-95.5dB	933hz
Channel 2	Channel 1	-101dB	-92.1dB	1KHz
Channel 2	Channel 3	-100dB	-95.6dB	616Hz
Channel 3	Channel 2	-100dB	-95.1dB	1KHz
Channel 3	Channel 4	-100dB	-95.5dB	758Hz
Channel 4	Channel 3	-105dB	-95.9dB	841Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

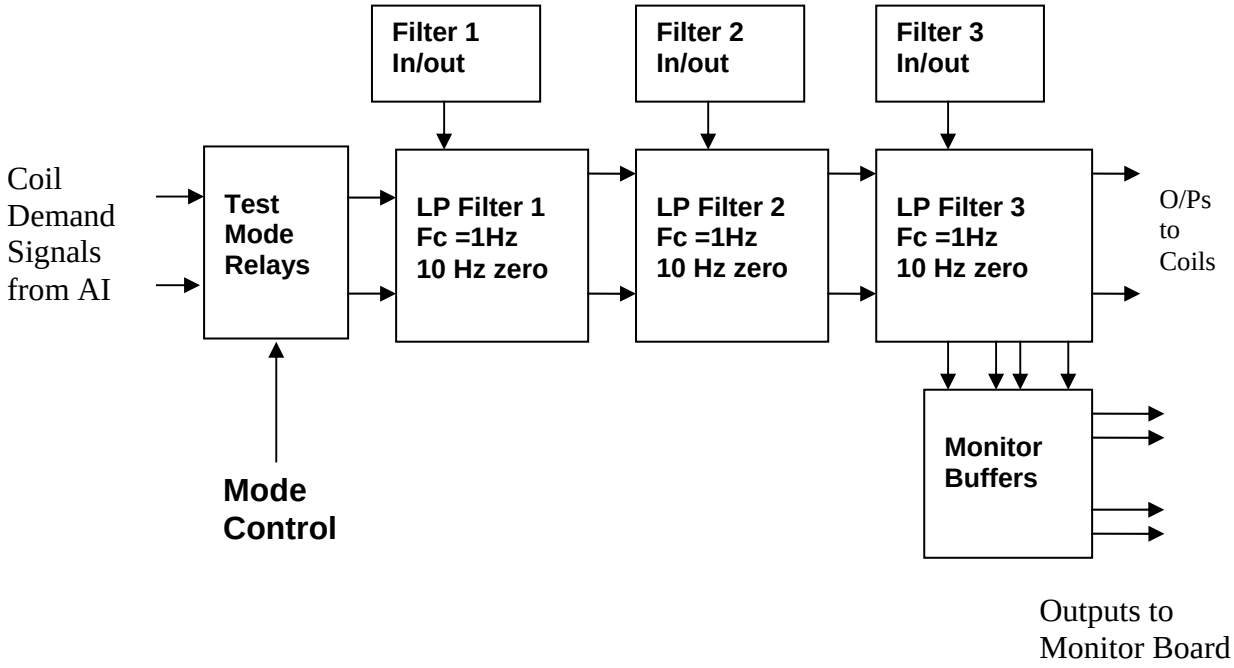


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

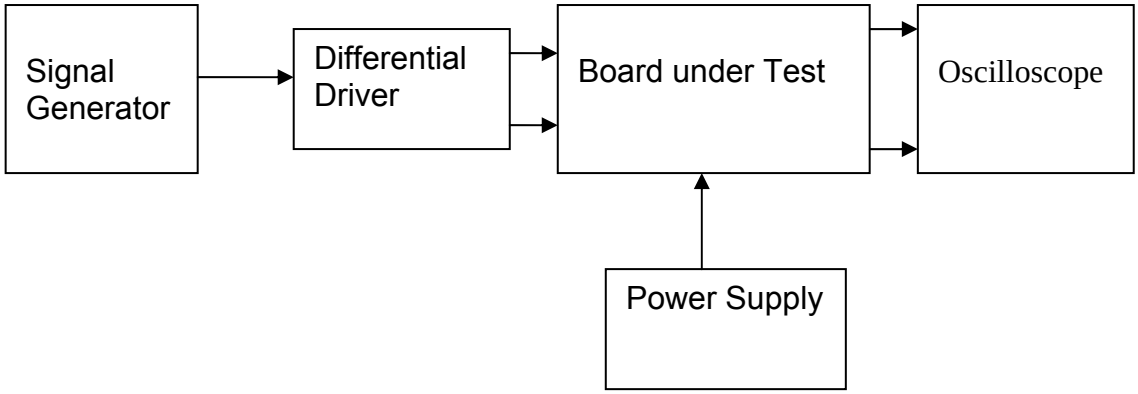
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	11.98	1mV
+15v	TP4	14.8	1mV
-15v	TP6	-14.94	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.5	3.5	3.5	3.3v to 3.7v	√
Ch2	3.5	3.5	3.5	3.3v to 3.7v	√
Ch3	3.5	3.5	3.5	3.3v to 3.7v	√
Ch4	3.5	3.5	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	0.4v to 0.5v	√
Ch2	5.0	5.0	5.0	0.4v to 0.5v	√
Ch3	5.0	5.0	5.0	0.4v to 0.5v	√
Ch4	5.0	5.0	5.0	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	0.4v to 0.5v	√
Ch2	5.0	5.0	5.0	0.4v to 0.5v	√
Ch3	5.0	5.0	5.0	0.4v to 0.5v	√
Ch4	5.0	5.0	5.0	0.4v to 0.5v	√

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.9	√	-26.9	√	-26.9	√	-26.9	√
-7v	-19.0	√	-19.5	√	-19.0	√	-19.0	√
-5v	-13.5	√	-14.0	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.9	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.6	√	2.7	√	2.7	√
5v	13.5	√	13.5	√	13.5	√	13.5	√
7v	18.9	√	18.8	√	18.8	√	18.9	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIM10
Test Engineer …… RMC
Date ……..7/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-103dB	-100dB	707Hz
Channel 2	Channel 1	-101dB	-95.3dB	758Hz
Channel 2	Channel 3	-101dB	-96.1dB	660Hz
Channel 3	Channel 2	-100dB	-99dB	1KHz
Channel 3	Channel 4	-100dB	-96dB	813Hz
Channel 4	Channel 3	-100dB	-97dB	616Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

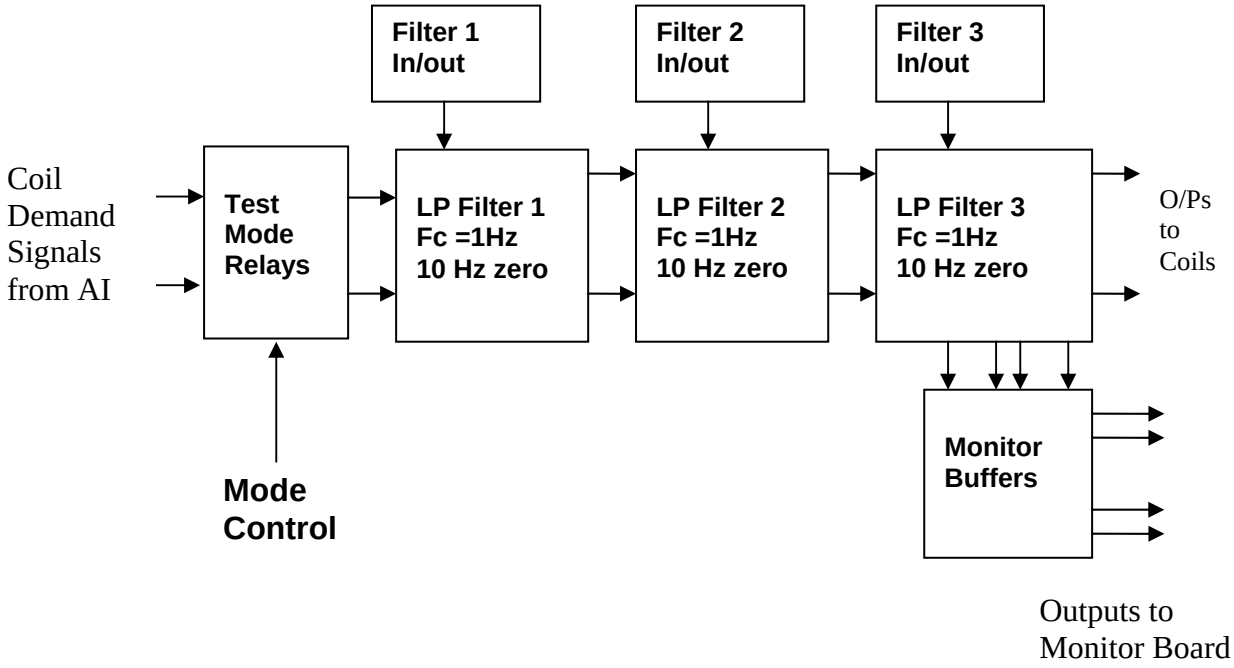


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM11
Test Engineer ……..XEN
Date ……..7/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

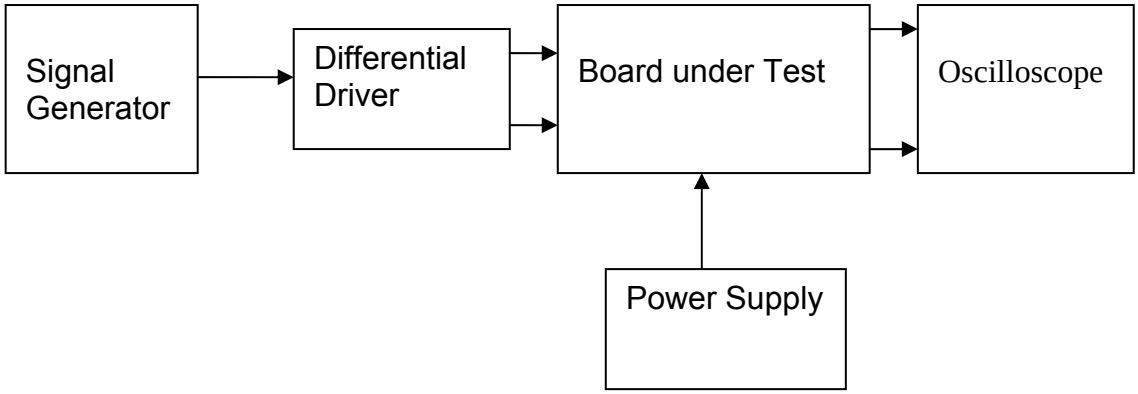
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM11
Test Engineer ……..XEN
Date ……..7/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.02	1mV
+15v	TP4	14.96	1mV
-15v	TP6	-14.98	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.5	3.5	3.5	3.3v to 3.7v	√
Ch2	3.5	3.5	3.5	3.3v to 3.7v	√
Ch3	3.5	3.5	3.5	3.3v to 3.7v	√
Ch4	3.5	3.5	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-26.9	√	-26.9	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.6	√	2.6	√	2.7	√
5v	13.0	√	13.5	√	13.0	√	13.3	√
7v	18.5	√	18.7	√	18.5	√	18.5	√
10v	26.9	√	26.9	√	26.9	√	27.0	√

Unit……UIM11
Test Engineer ……..XEN
Date ……...7/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-96.4dB	1KHz
Channel 2	Channel 1	-101dB	-96.0dB	436Hz
Channel 2	Channel 3	-101dB	-95.3dB	870Hz
Channel 3	Channel 2	-100dB	-95.0dB	436Hz
Channel 3	Channel 4	-100dB	-95.0dB	812Hz
Channel 4	Channel 3	-100dB	-95.0dB	785Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

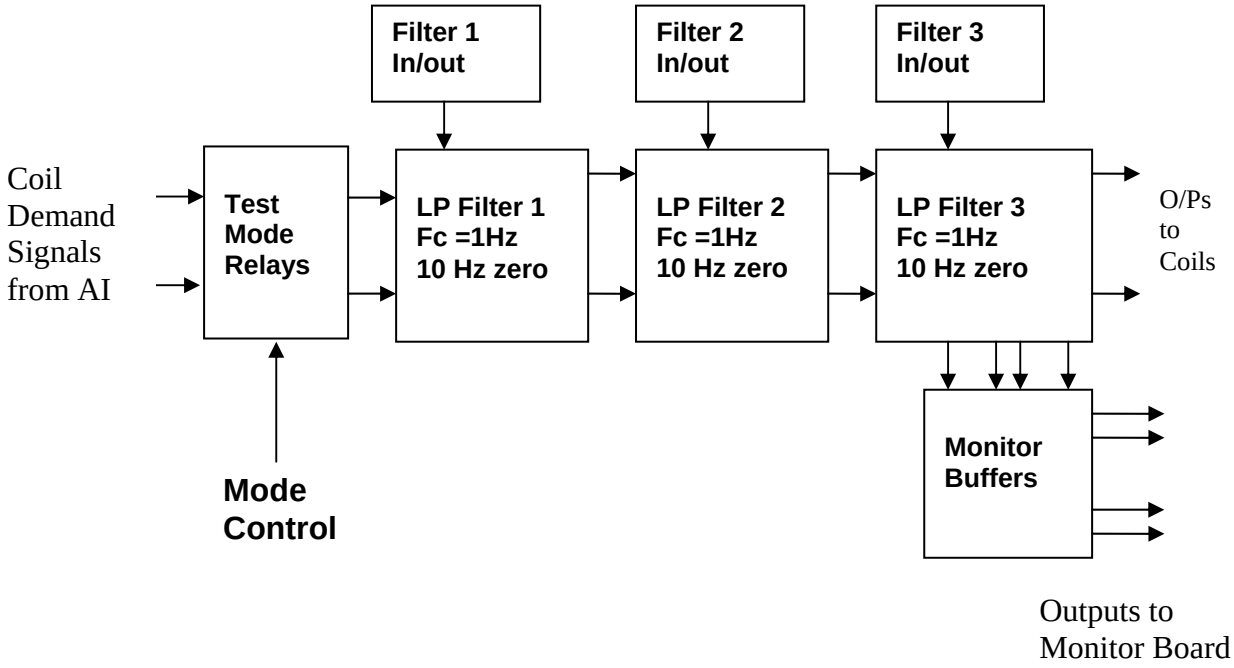


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

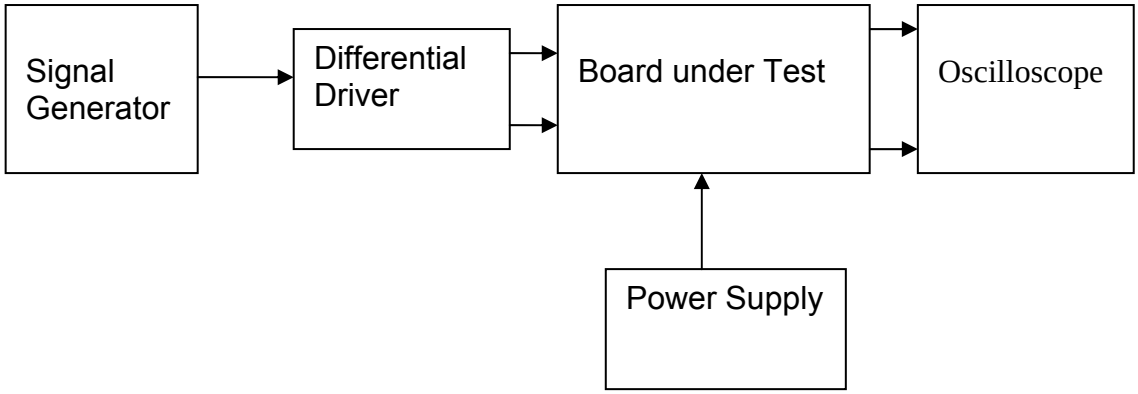
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.6	1mV
+15v	TP4	14.9	1mV
-15v	TP6	-14.95	1mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.7	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.7	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.7	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.7	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.8	√	-26.9	√	-26.9	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.6	√
-1v	-2.8	√	-2.8	√	-2.7	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.6	√	2.6	√	2.7	√
5v	13.1	√	13.3	√	13.1	√	13.3	√
7v	18.8	√	18.8	√	18.5	√	18.8	√
10v	26.9	√	27.0	√	27.0	√	27.0	√

Unit……UIM12
Test Engineer ……..XEN
Date ……..10/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-103dB	-96dB	707Hz
Channel 2	Channel 1	-101dB	-95dB	707Hz
Channel 2	Channel 3	-101dB	-95dB	982Hz
Channel 3	Channel 2	-100dB	-96dB	660Hz
Channel 3	Channel 4	-101dB	-95dB	707Hz
Channel 4	Channel 3	-101dB	-96dB	707Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

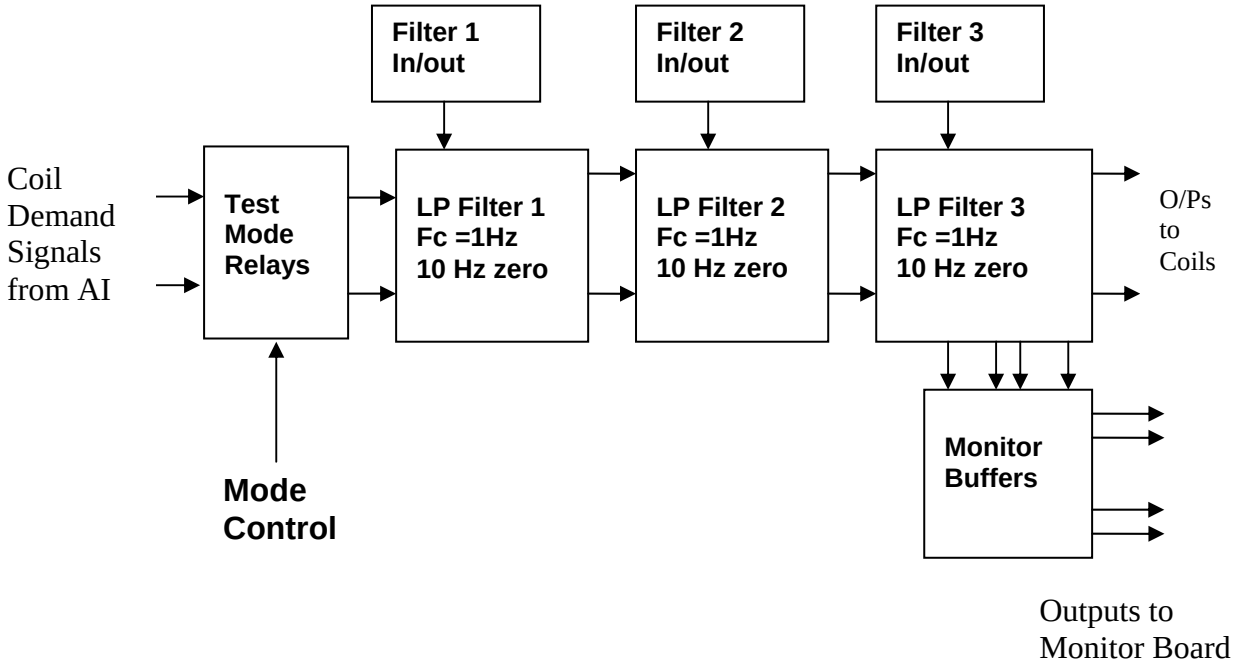


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

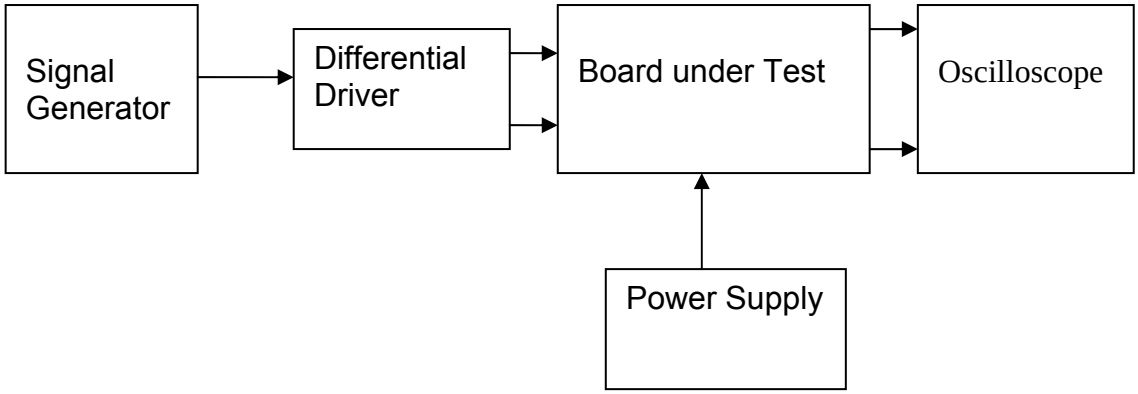
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.10	1mV
+15v	TP4	15.03	1mV
-15v	TP6	-15.03	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.5	3.5	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM13P
Test Engineer ……..…XEN
Date ……..…10/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-26.5	√	-26.9	√	-27.0	√	-27.0	√
-7v	-18.9	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.6	√	2.8	√	2.7	√
5v	13.5	√	13.5	√	13.5	√	13.5	√
7v	19.0	√	18.8	√	18.9	√	19.0	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIM13P
Test Engineer ……..….XEN
Date ……..…10/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-94dB	933Hz
Channel 2	Channel 1	-101dB	-94dB	575Hz
Channel 2	Channel 3	-101dB	-94dB	812Hz
Channel 3	Channel 2	-100dB	-94dB	1KHz
Channel 3	Channel 4	-101dB	-94dB	575Hz
Channel 4	Channel 3	-101dB	-94dB	917Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

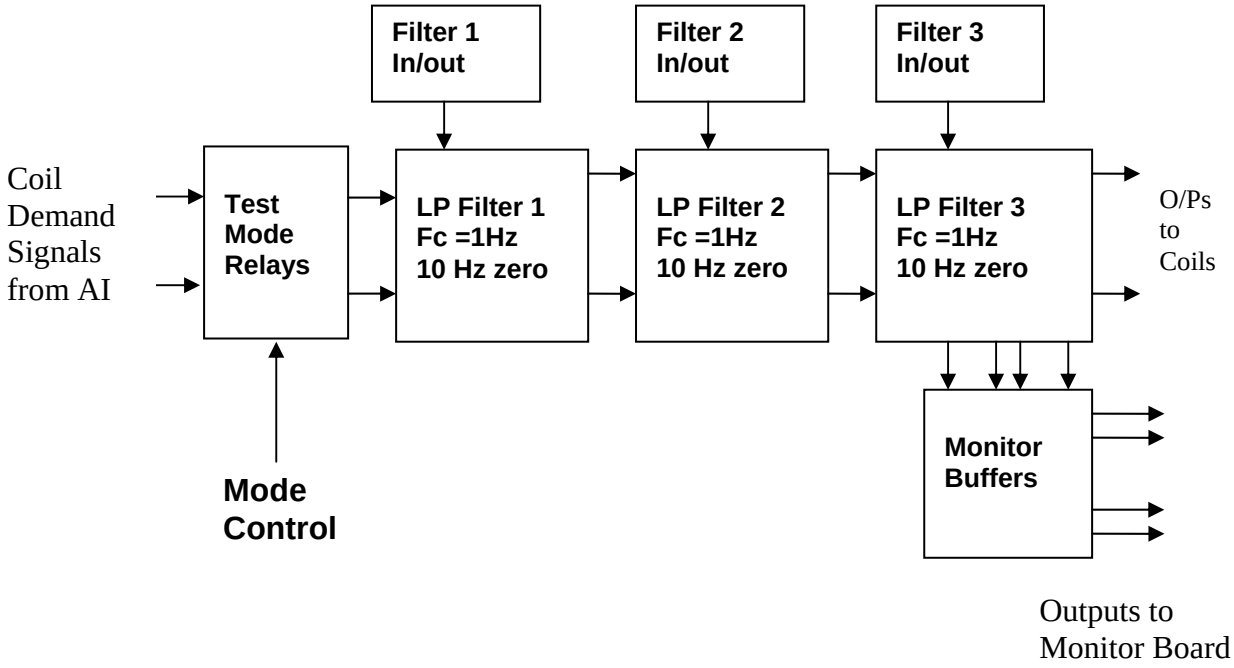


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

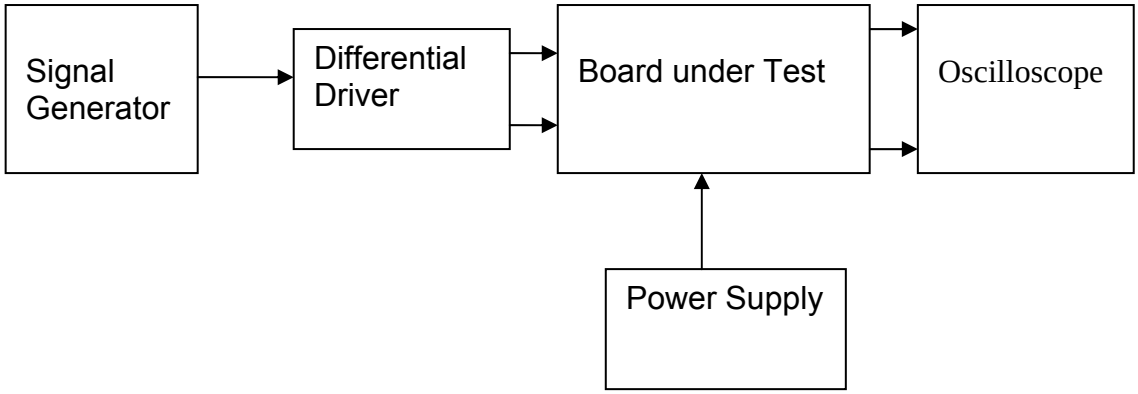
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.04	1mV
+15v	TP4	14.78	1 mV
-15v	TP6	-14.99	5 mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.1	5.1	5.1	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.5	3.5	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-26.9	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.6	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.8	√	2.7	√	2.8	√
5v	13.5	√	13.5	√	13.5	√	13.5	√
7v	18.9	√	19.0	√	18.9	√	19.0	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIM14
Test Engineer ……..XEN
Date ……10/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-123dB	-107dB	1KHz
Channel 2	Channel 1	-115dB	-103dB	933Hz
Channel 2	Channel 3	-115dB	-106dB	870Hz
Channel 3	Channel 2	-118dB	-109dB	660Hz
Channel 3	Channel 4	-120dB	-106dB	933Hz
Channel 4	Channel 3	-135dB	-107dB	144Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

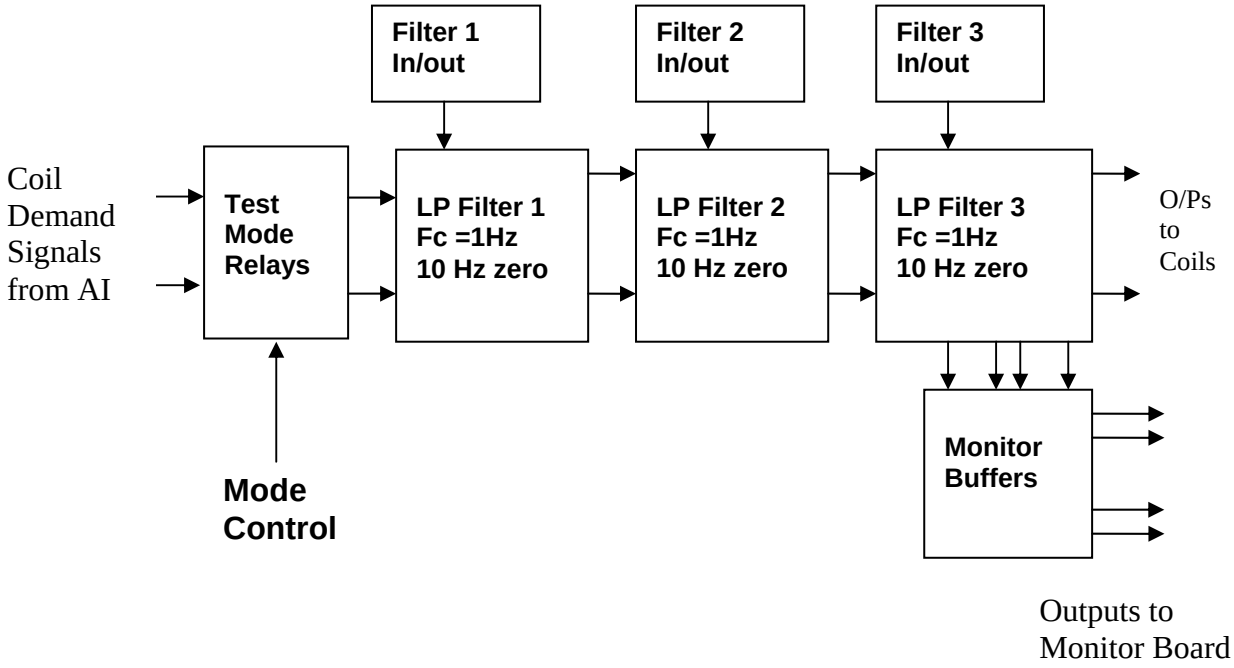


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

LED DS1 slightly off flush with the PCB – adjusted.

One pin on the +15v regulator was not soldered to the PCB - resoldered

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

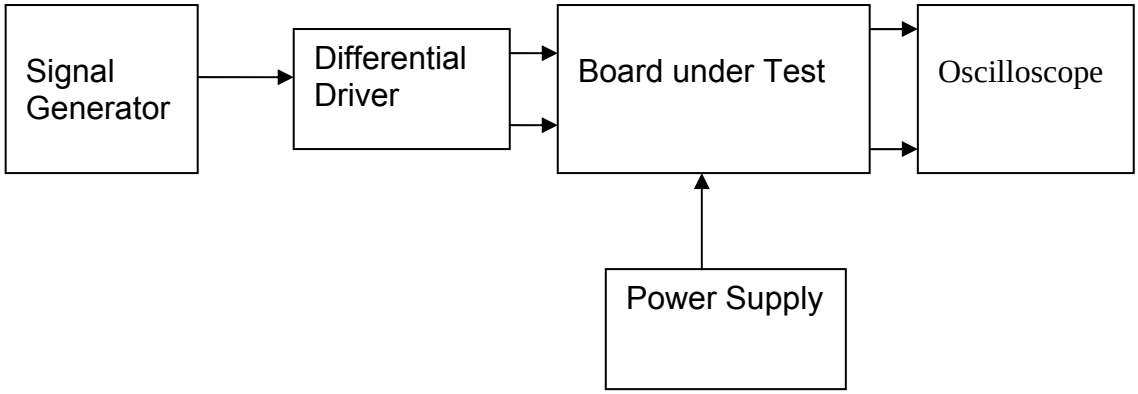
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.01	1mV
+15v	TP4	15.02	1mV
-15v	TP6	-14.93	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270 mA
-16.5v	200 mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.67	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.67	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.67	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.67	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-26.8	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.6	√	2.7	√	2.6	√	2.6	√
5v	13.3	√	13.5	√	13.3	√	13.3	√
7v	18.7	√	18.9	√	18.5	√	18.8	√
10v	27.0	√	27.0	√	26.9	√	26.8	√

Unit……UIM15
Test Engineer ……..XEN
Date ……..11/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-96dB	1KHz
Channel 2	Channel 1	-101dB	-95dB	144Hz
Channel 2	Channel 3	-101dB	-97dB	826Hz
Channel 3	Channel 2	-101dB	-96dB	1KHz
Channel 3	Channel 4	-101dB	-96dB	537Hz
Channel 4	Channel 3	-101dB	-96dB	537Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

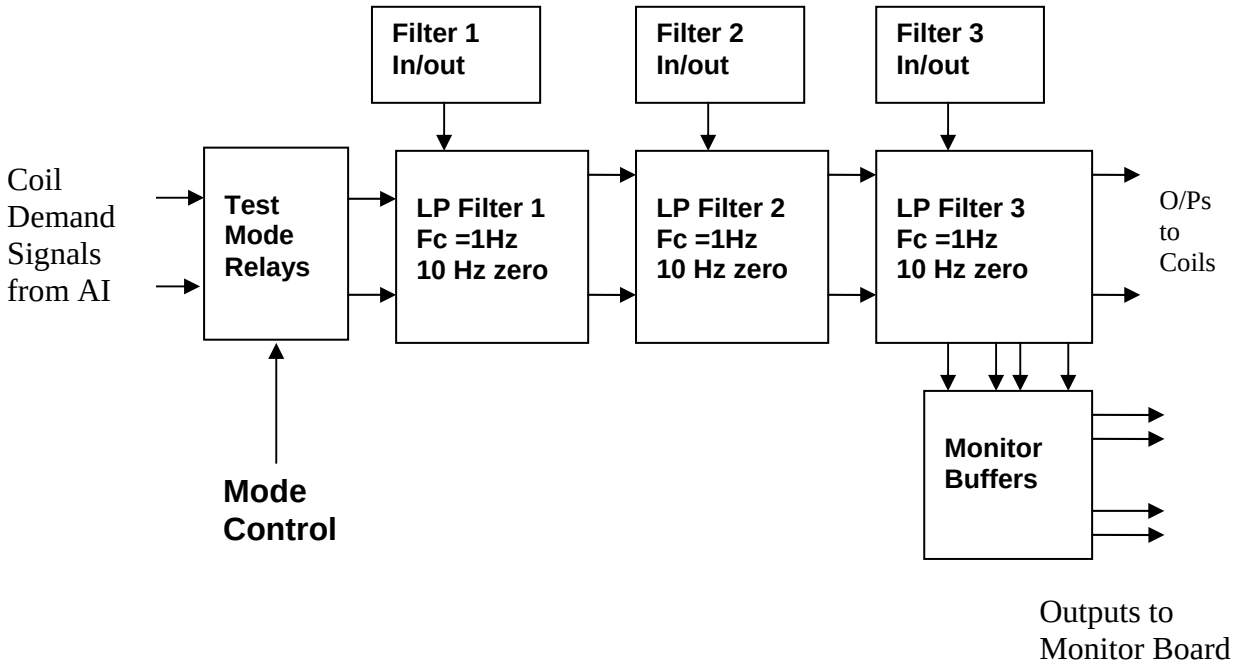


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

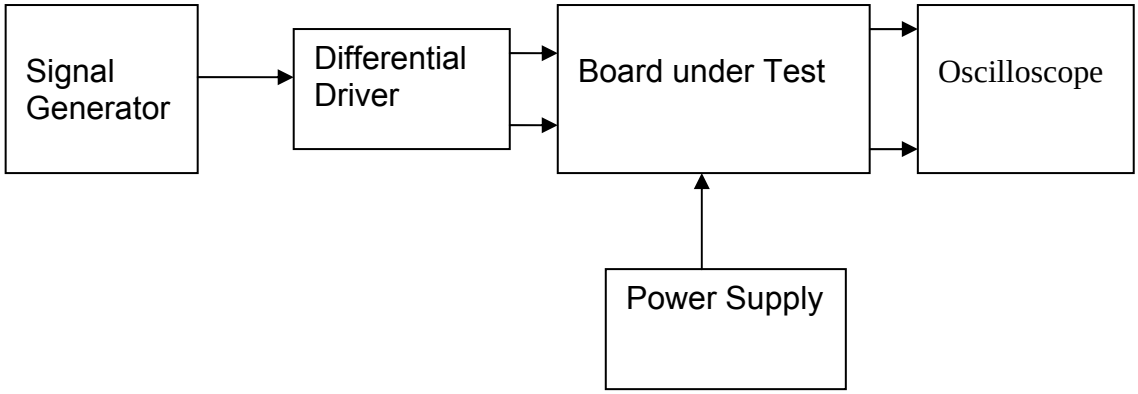
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.01	1mV
+15v	TP4	14.93	1mV
-15v	TP6	-14.97	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.4	3.3v to 3.7v	√
Ch2	3.4	3.4	3.4	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-18.9	√
-5v	-13.5	√	-13.5	√	-12.6	√	-13.8	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.7	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.6	√	2.8	√	2.8	√
5v	13.5	√	13.1	√	13.5	√	13.5	√
7v	19.0	√	18.6	√	19.0	√	18.9	√
10v	27.0	√	26.9	√	27.0	√	27.0	√

Unit……UIM16
Test Engineer …….XEN
Date ……12/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-96dB	870Hz
Channel 2	Channel 1	-101dB	-95dB	870Hz
Channel 2	Channel 3	-100dB	-94dB	933Hz
Channel 3	Channel 2	-100dB	-96dB	870Hz
Channel 3	Channel 4	-103dB	-97dB	501Hz
Channel 4	Channel 3	-101dB	-94dB	812Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

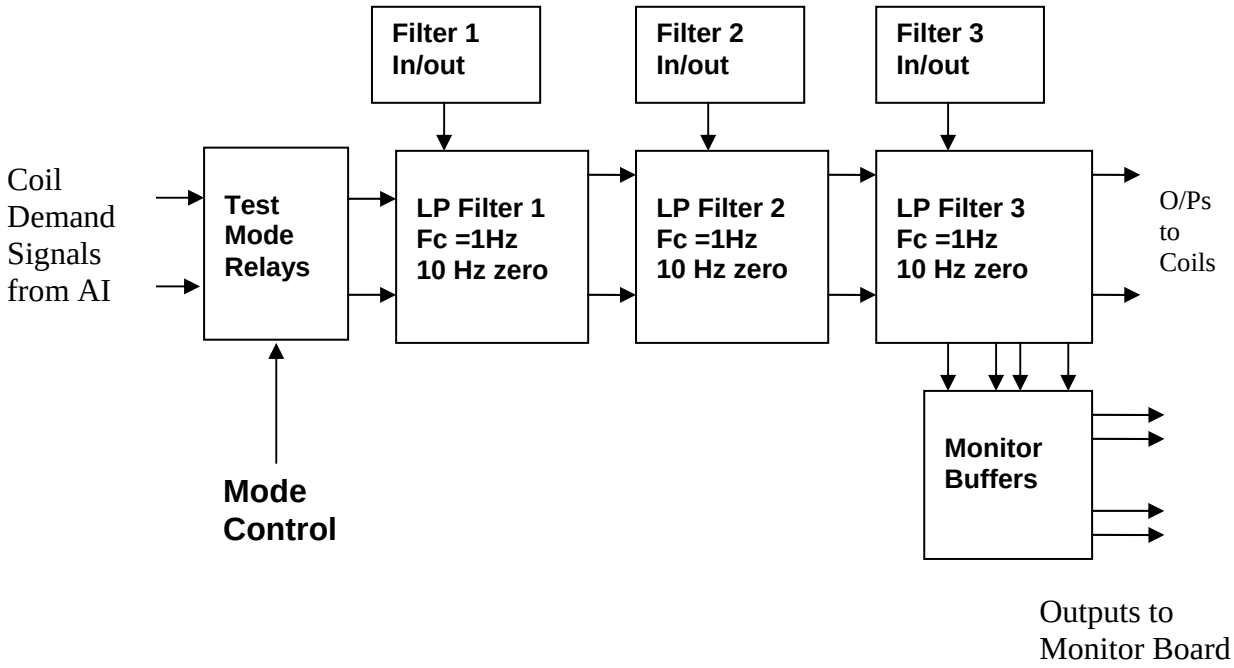


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

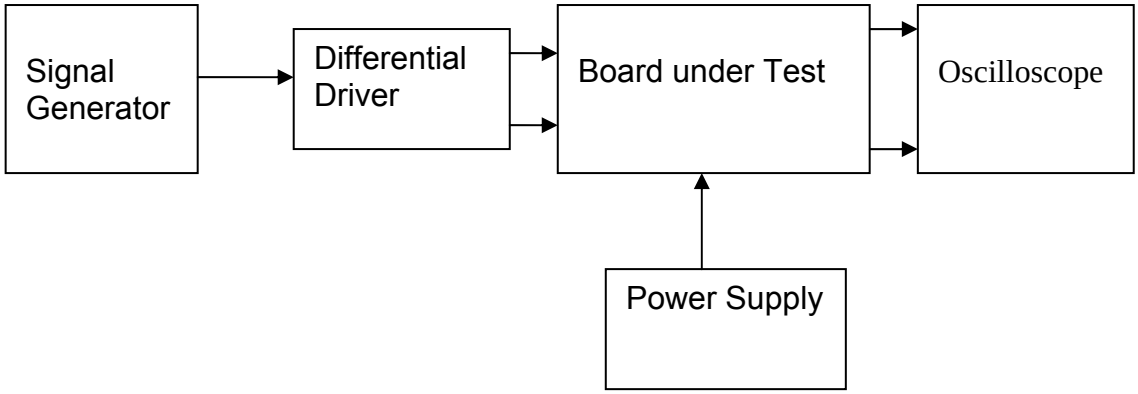
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.02	1mV
+15v	TP4	14.94	1mV
-15v	TP6	14.99	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.5	3.3v to 3.7v	√
Ch2	3.4	3.4	3.5	3.3v to 3.7v	√
Ch3	3.4	3.4	3.5	3.3v to 3.7v	√
Ch4	3.4	3.4	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-26.9	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.7	√	-13.8	√	-13.7	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.7	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.8	√	2.6	√	2.7	√
5v	13.3	√	13.5	√	13.3	√	13.4	√
7v	18.8	√	19.0	√	18.9	√	18.9	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIM17
Test Engineer …….XEN
Date ……13/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-102dB	-96dB	812Hz
Channel 2	Channel 1	-101dB	-95dB	812Hz
Channel 2	Channel 3	-101dB	-96dB	467Hz
Channel 3	Channel 2	-100dB	-96dB	1KHz
Channel 3	Channel 4	-100dB	-94dB	933Hz
Channel 4	Channel 3	-101dB	-95dB	758Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……
Test Engineer …….XEN
Date …….

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

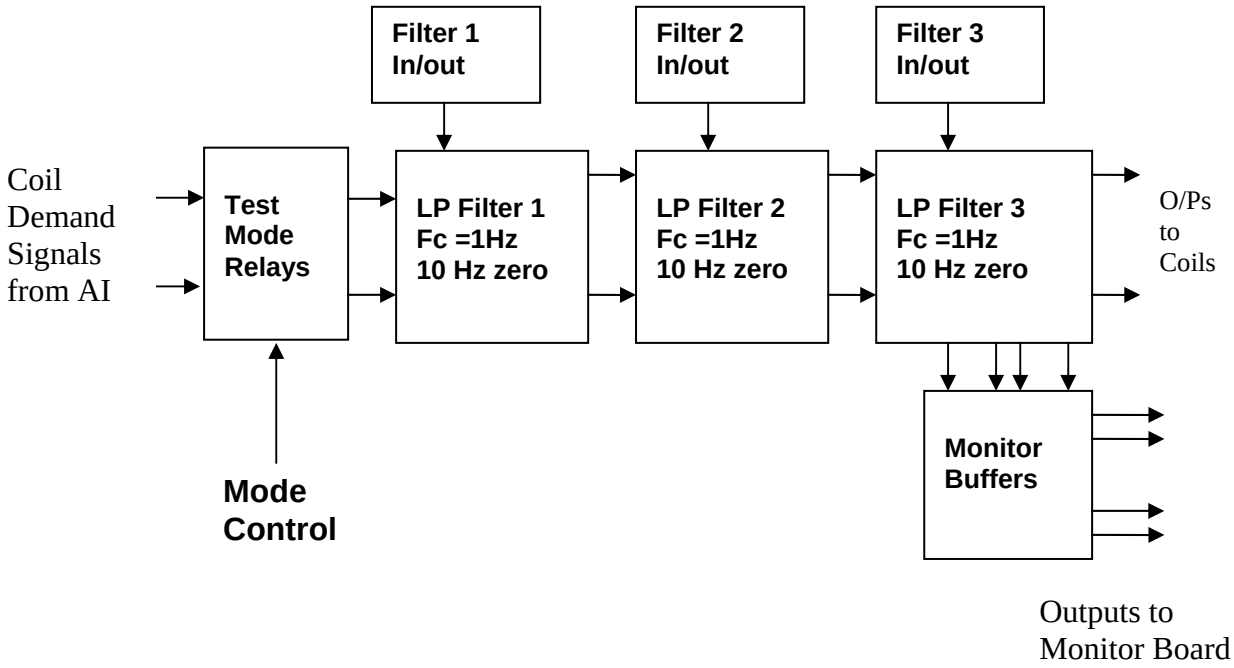


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Loose joint on C103 Ch3
Re-soldered

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

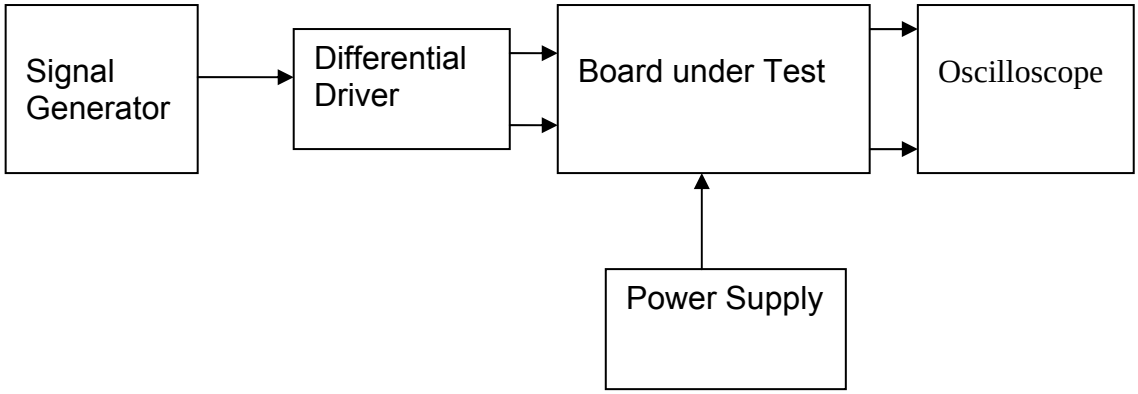
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.08	1mV
+15v	TP4	14.95	1mV
-15v	TP6	-14.90	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.4	3.5	3.3v to 3.7v	√
Ch2	3.4	3.4	3.5	3.3v to 3.7v	√
Ch3	3.4	3.4	3.4	3.3v to 3.7v	√
Ch4	3.4	3.4	3.4	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.5	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.7	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.8	√	2.7	√	2.8	√	2.6	√
5v	13.5	√	13.5	√	13.5	√	13.3	√
7v	18.9	√	19.0	√	19.0	√	18.9	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

Unit……UIN18
Test Engineer …….XEN
Date ……13/8/9

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-101dB	-94dB	758Hz
Channel 2	Channel 1	-101dB	-92dB	1KHz
Channel 2	Channel 3	-101dB	-96dB	933Hz
Channel 3	Channel 2	-100dB	-95dB	933Hz
Channel 3	Channel 4	-105dB	-95dB	933Hz
Channel 4	Channel 3	-102dB	-95dB	933Hz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

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LIGO-T0900237-v1 Advanced LIGO UK 6 May 2009

UIM Coil Driver Board Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

UIM COIL DRIVER BOARD
TEST REPORT

Unit……UIM20
Test Engineer …….XEN
Date ……14/8/9

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

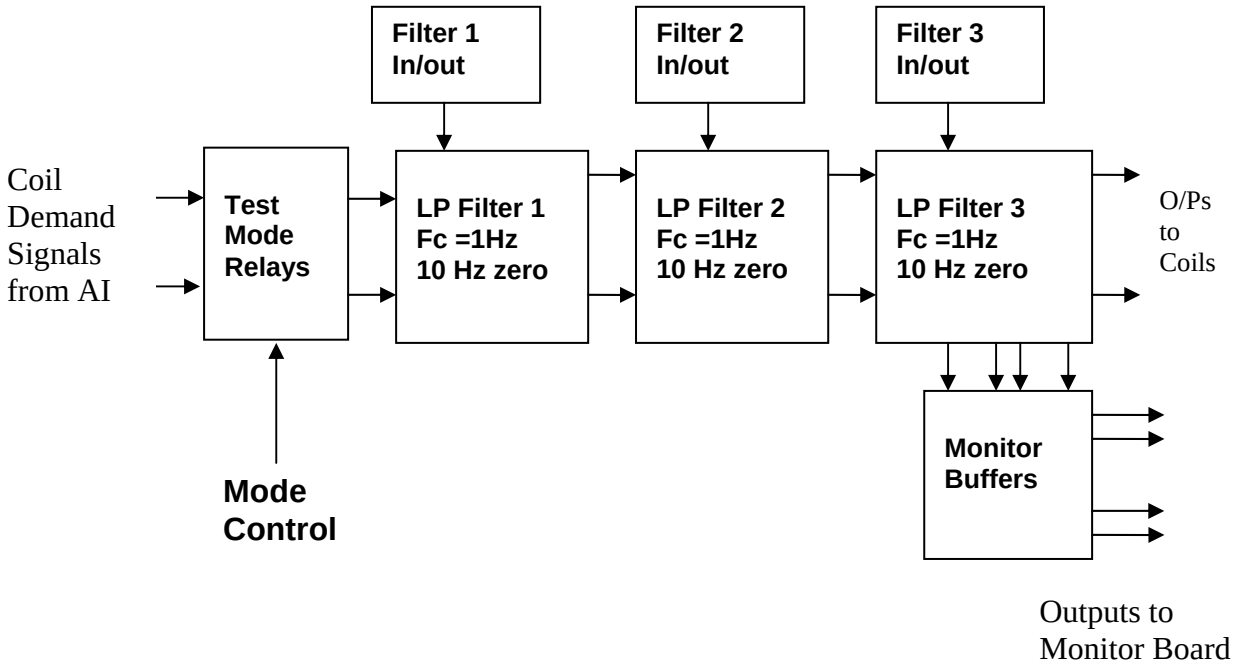


FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

Unit……UIM20
Test Engineer …….XEN
Date ……14/8/9

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model
DVM	FLUKE	115
V/C calibrator	TIME ELECTRONICS	1044
Signal Generator	Agilent	332504
Oscilloscope	Iso Tech	ISR622
PSU	Farnell	LR39-2
PSU	Farnell	LR39-2

Unit……UIM20
Test Engineer …….XEN
Date ……14/8/9

3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Good

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

Unit……UIM20
Test Engineer …….XEN
Date ……14/8/9

4. Continuity Checks

Use a multi-meter to check the connections below exist

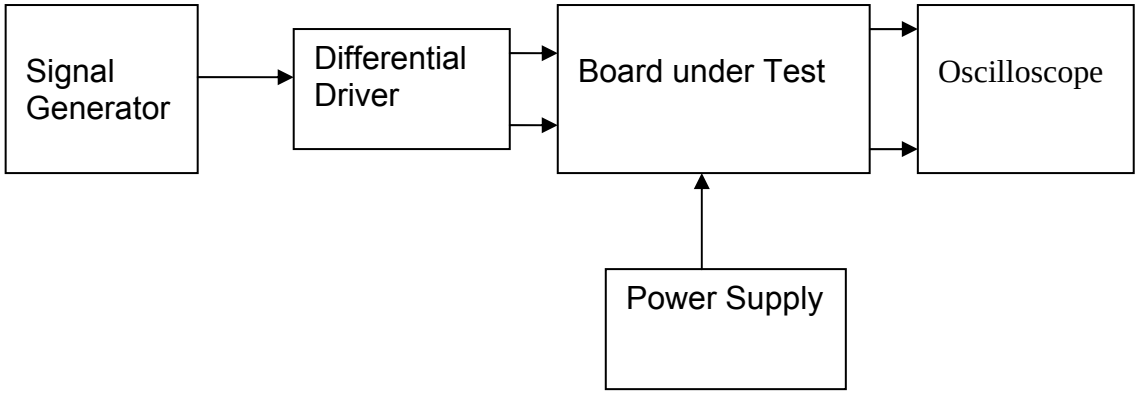
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	√
10	V+	+17v Supply	√
11	V-	-17v Supply	√
12	V-	-17v Supply	√
13	0V	Return	√
22	0V	Return	√
23	0V	Return	√
24	0V	Return	√
25	0V	Return	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

Unit……UIM20
Test Engineer …….XEN
Date ……14/8/9

6. Power

Check the polarity of the wiring: 3 Pin Power Connector
Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5	12.05	1mV
+15v	TP4	14.85	1mV
-15v	TP6	14.95	5mV

All Outputs smooth DC, no oscillation?	OK

Record Power Supply Currents

Supply	Current
+16.5v	270mA
-16.5v	200mA

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On? √

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7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1	√	√	√	√	√	√
Ch2	√	√	√	√	√	√
Ch3	√	√	√	√	√	√
Ch4	√	√	√	√	√	√

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1	4.8	5.0	5.0	4.8v to 5v	√
Ch2	4.8	5.0	5.0	4.8v to 5v	√
Ch3	4.8	5.0	5.0	4.8v to 5v	√
Ch4	4.8	5.0	5.0	4.8v to 5v	√

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	5.0	5.0	5.0	4.9 to 5.1v	√
Ch2	5.0	5.0	5.0	4.9 to 5.1v	√
Ch3	5.0	5.0	5.0	4.9 to 5.1v	√
Ch4	5.0	5.0	5.0	4.9 to 5.1v	√

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	3.4	3.5	3.5	3.3v to 3.7v	√
Ch2	3.4	3.5	3.5	3.3v to 3.7v	√
Ch3	3.5	3.5	3.5	3.3v to 3.7v	√
Ch4	3.4	3.4	3.5	3.3v to 3.7v	√

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.7	0.7	0.7	0.48 to 0.75v	√
Ch2	0.7	0.7	0.7	0.48 to 0.75v	√
Ch3	0.7	0.7	0.7	0.48 to 0.75v	√
Ch4	0.7	0.7	0.7	0.48 to 0.75v	√

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1	0.5	0.5	0.5	0.4v to 0.5v	√
Ch2	0.5	0.5	0.5	0.4v to 0.5v	√
Ch3	0.5	0.5	0.5	0.4v to 0.5v	√
Ch4	0.5	0.5	0.5	0.4v to 0.5v	√

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9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v	1.65	√
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v	1.65	√
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v	1.65	√
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v	5.0	√
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v	1.65	√

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v	-27.0	√	-27.0	√	-27.0	√	-27.0	√
-7v	-19.0	√	-19.0	√	-19.0	√	-19.0	√
-5v	-13.6	√	-13.5	√	-13.5	√	-13.5	√
-1v	-2.8	√	-2.8	√	-2.8	√	-2.8	√
0v	0	√	0	√	0	√	0	√
1v	2.7	√	2.7	√	2.7	√	2.6	√
5v	13.5	√	13.5	√	13.5	√	13.5	√
7v	19.0	√	18.9	√	18.9	√	18.9	√
10v	27.0	√	27.0	√	27.0	√	27.0	√

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the output in dBs at 10 Hz on adjacent channels. Record maximum output and the frequency at which this occurs.

INPUT CHANNEL	OUTPUT CHANNEL	Output at 10Hz	Max o/p	@ Freq
Channel 1	Channel 2	-100dB	-92dB	467Hz
Channel 2	Channel 1	-100dB	-92dB	154Hz
Channel 2	Channel 3	-100dB	-95dB	886Hz
Channel 3	Channel 2	-100dB	-93dB	616Hz
Channel 3	Channel 4	-100dB	-94dB	154Hz
Channel 4	Channel 3	-100dB	-94dB	1KHz

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		