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UIM Drive Unit Design Description

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of the Advanced LIGO Project, prepared by members of the UK team.

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DESIGN AND MANUFACTURE OF THE UIM DRIVER UNIT

CONTENTS

1, INTRODUCTION

This document describes the philosophy and methods used to produce the UIM Coil Drive Electronics Unit for Advanced LIGO. Estimates of the performance are given, together with performance measurements from the pre-production units.

1.1 Context

The UIM Driver unit contains four channels of amplification and filtering. The outputs from the unit control the position of the UIM stage in the Advanced LIGO Quad Suspension.

The output currents from the unit energise four coils which attract magnets mounted on the UIM section of the suspension, giving a force which moves the UIM to the desired position.

Monitoring circuits are included in the unit to monitor its activity. The monitor circuits are housed on a separate PCB within the unit.

2. MONITORS

2.1 Specification

The following monitors are required by the specification [(1)] :-

(1) Output Voltage Monitors which cover the full dynamic range of the outputs.

(2) Monitors capable of seeing the noise floor of the outputs for 10Hz<freq<1 KHz

(3) Monitors of fast instantaneous measurement of the output current.

(4) Monitors of the RMS current with a time constant of 1 second capable of monitoring the full current range of the drivers

(5) Status (position) monitors/read backs for all switches used in the design.

2.2 Monitors Provided

(1) The Output Voltage Monitor. A monitor which measures the voltage between the two output operational amplifiers is provided. It has a gain of 1/3, so the highest possible output voltage within the constraints of the power rails (+/- 15v) gives a monitor output of 10v

(2) The Noise Monitor. This is a high gain AC coupled amplifier with a low noise front end. The corner frequency of each of the stages is 5 Hz.

(3) The Output Current monitor. This is a four input summing amplifier which measures the sum of the voltages across the two output resistors. It has a gain of 1/3.

(4) The R.M.S monitor. A true RMS integrated circuit is used to convert the output of the current monitor into an RMS value. Its overall gain is 1, which combined with the current monitor gain, gives an overall gain of 1/3.

The settling time of this circuit varies with the applied input voltage.

(5) Status outputs for all switches. In the case of the filter relays, a spare relay contact is used to indicate the position of the relay. In the case of the test relay, all the contacts on the relay are already used, so a transistor circuit was added to monitor the state of the test relay coil voltage.

2.3 Monitor Design Details

2.3.1 Voltage Monitor

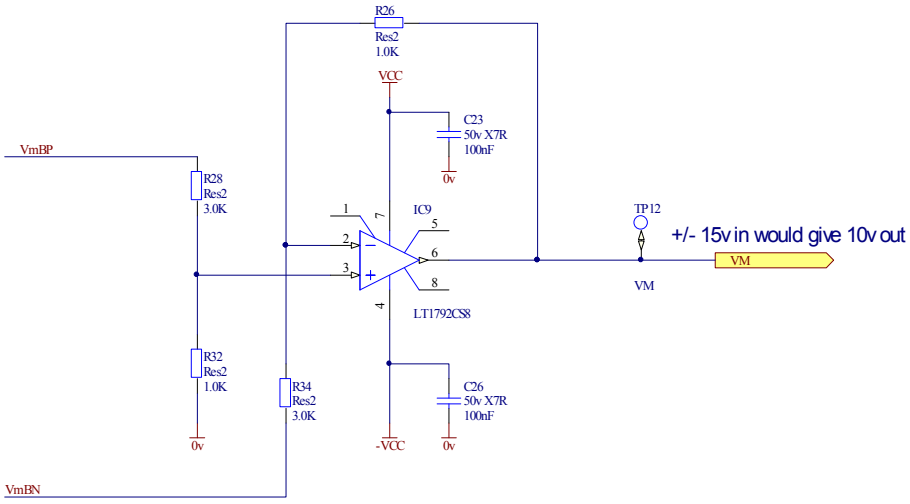


Fig 1 The Voltage Monitor Circuit

The Voltage Monitor Circuit consists of a summing amplifier, which subtracts the positive amplifier output from the negative amplifier output. This gives the total output voltage. The voltage gain of the circuit is ⅓ , which means that if the inputs are at their maximum voltage, +/-15v (rail voltage) the output is +10v.
There is one voltage monitor circuit per Drive Amplifier channel.

2.3.2 Current Monitor and R.M.S Circuit
Current Monitor

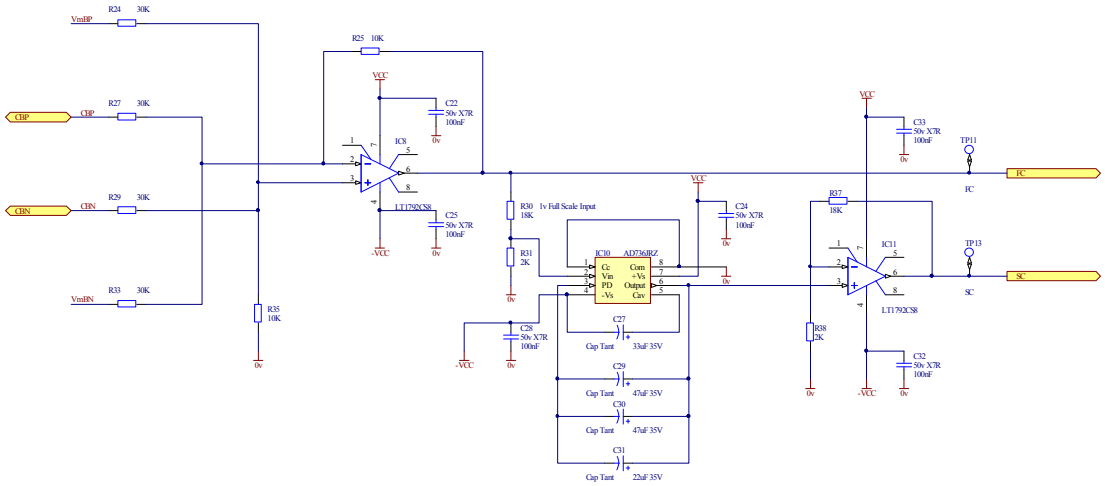


Fig 2 The Current Monitor and RMS circuit

The Current Monitor section consists of a 4 input Summing Amplifier. This calculates the voltages across the two output resistors, as this is proportional to the instantaneous output current. The sum performed is:

(Pos. Amplifier Output – Pos. Coil Voltage) + (Neg. Coil Voltage - Neg. Amplifier Output).

The gain of the amplifier is set to ⅓, which means that if the inputs are at their maximum possible voltage, the output is +10v.

At low frequencies, 1 volt out represents 1.5 volts across each driver output resistor.
As the output resistors are each 3.9K, this represents a current of 0.3846 mA.
1mA out would therefore produce a current monitor output of 2.6 volts.

RMS
The r.m.s circuit uses a true r.m.s convertor integrated circuit type AD736, to convert the output signal from the Current Monitor into an r.m.s. measurement. As large signals into the AD736 result in a reduced accuracy, the circuit is preceded by a 10:1 attenuator and followed by a 10x gain stage. This gives the r.m.s circuit the same overall gain as the current monitor. The settling time of this circuit varies with the applied voltage:

IC Input Voltage	Output from the Amplifier	Settling time.
10mV	0.1 volt	1 Second
100mV	1 volt	100milliseconds
1V	10 volts	10 milliseconds

There is one current monitor and r.m.s circuit per Drive Amplifier channel, and there are four channels in each UIM Drive Unit.

2.3.3 Noise Monitor

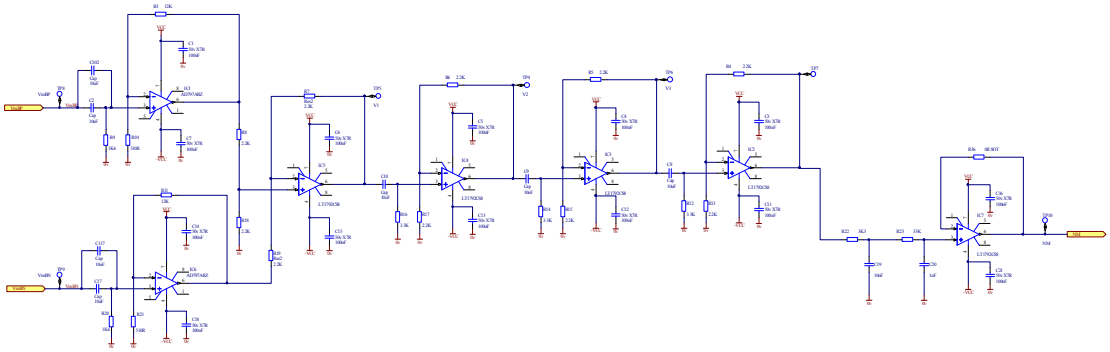


Fig 3 The Noise Monitor circuit

The noise monitor circuit is designed to amplify the ac noise voltage across the Drive Amplifier output, while rejecting dc signals.

An ac coupled, low noise differential amplifier front end is followed by a series of 3 gain stages, each ac coupled. Each stage has a gain of 2, and a corner frequency of 5Hz. These high pass stages are followed by a two pole low pass filter stage, each stage having a corner frequency of 5 KHz.

3. COIL DRIVE CIRCUITS

3.1 Specification

3.1.1 Input Signals

The specification [1] defines the following:

Input signals: Voltage Range: +/-10V ($20V_{p-p}$)

Noise Voltage: 100nV/√Hz over the frequency range of interest for the coil driver.

3.1.2 Dynamic range

Output current for each UIM coil driver should be at least $2mA_{rms}$

For frequencies less than 1 Hz, each coil driver must be capable of supplying the full $2mA_{rms}$

Each driver must also be capable of supplying currents of up to $16uA_{rms}$ at 100Hz.

3.1.3 Noise

Frequency	Current Noise Requirement
1 Hz	0.500 nA/√Hz
10 Hz	3 pA/√Hz
100 Hz	200 nA/√Hz
1000 Hz	1000 nA/√Hz

4. COIL DRIVE DESIGN PHILOSOPHY

4.1 Dynamic range

Achieving the required dynamic range is not a problem, as 2mA may be comfortably supplied by an operational amplifier. The output current may then be controlled by means of a series resistor. The dynamic range at 100 Hz and above is boosted by means of an RC network which bypasses the series output resistor.

4.2 Noise

The main difficulty in meeting the specification is the noise requirement at 10 Hz. The noise level is required to be less than 3 pA/√Hz, which is difficult to achieve.

Noise will emanate from several different sources.

The main noise sources are:
(1) Input noise
(2) Ground noise
(3) EMC
(4) Component noise

(1) Input Noise

As a high dynamic range is required at < 1Hz, and a low noise level is required at 10Hz, input noise at 10 Hz is attenuated by means of three low pass filter stages. Each filter stage may be remotely switched in or out as required, permitting a range of operational modes with varying noise/dynamic requirements.

(2) Ground Noise

Ground noise is always a problem in large complex low noise systems, particularly when there are long cable runs. LIGO is a very large, very complex system with extremely long cable runs, and very tight noise requirements.

This problem is avoided by keeping the signals independent of ground. As the input signals are symmetrical about ground, it is possible to engineer a true four wire system, by using two independent chains of amplifiers. This design also avoids any ground noise problems internal to the unit.

(3) EMC

EMC pick up on the amplifier outputs might also be a problem. The risk of this potential problem has been reduced, as the balanced outputs have identical output impedances. Any noise voltages induced by EMC should be almost entirely common mode, appearing equally across both coil terminals, and so resulting in no noise current in the coils.

(4) Component Noise

Component noise will be generated by all components in the unit. Resistors will unavoidably generate Johnson noise. Low noise metal film resistors are used in these units to minimise voltage dependant noise.

The operational amplifier types used in this design are carefully selected for their low voltage and current noise specifications. The design takes account of the noise voltages generated by the input current noise.

Ceramic capacitors are not used in the signal paths, as they are considered to be a possible source of microphonic noise.

5. COIL DRIVER DESIGN DETAILS

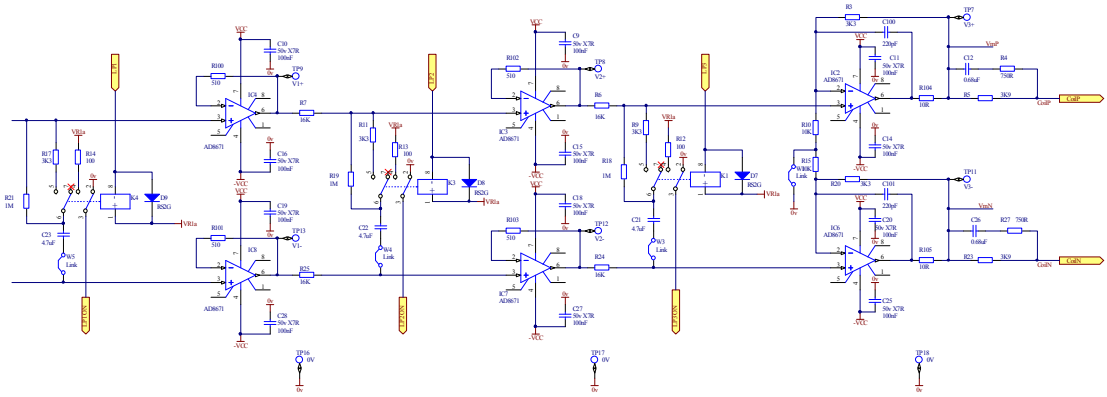


Fig 1. A UIM Driver Channel.

The above diagram shows the active section of a channel of a UIM Driver. There are four such channels in each UIM Driver Unit.

The circuit consists of three low pass filters stages, each followed by a buffer amplifier. As specified in the Design Requirements Document [1], each 1Hz pole in the filter is followed by a zero at 10 Hz. Each filter stage has a relay which may be switched in or out as required, to configure the unit in its various modes of operation.

The circuit is a true four terminal design.

The output stage has a gain of 1.2, and is followed by a series resistor (3.9K) on each of the two outputs. This defines the maximum output current.

The output resistor is bypassed by a 0.68uF capacitor in series with 750 Ohms. This boosts the dynamic range at 100 Hz and above, while having a negligible effect on the noise at 10Hz.

6. THEORETICAL PERFORMANCE

6.1 Dynamic range at Low Frequencies

As the input voltage is specified as 10V, and the gain is 1.2, the voltage swing of each output terminal will be +/-12v. As each output resistor is 3.9K, and the OSEM coil resistance is 40 Ohms, the total output resistance is:

(3K9 + 3K9 + 40 Ω) = 7.84K

The voltage across this resistance will be 24v maximum, so the current =

24/7.84K = 3.03 mA

For a sine wave, this corresponds to 2.16 mA rms, which exceeds the 2mA rms requirement.

6.2 Dynamic range at 100Hz

Simulation shows that the bypass network on the output resistor increases the output current by a factor of 2 (6dB) at 100Hz. Simulation also shows that the attenuation factor for each filter stage at 100Hz is 0.093 (-20.5dB).

With two filter stages switched in, the total attenuation at 100 Hz will therefore be 0.0172 (35dB). The low frequency output current will therefore be attenuated by this figure at 100Hz, giving:

2.16mA x 0.0172 = 37uA.

This exceeds the 16uA requirement.

With all 3 filters switched in, the attenuation at 100Hz will be a factor of 0.00156 (-55.5dB) giving an output current of 3.45uA.

It is recommended that if the full dynamic range is required at 100 Hz, the first filter stage is switched out.

6.3 Noise Requirements

The permitted noise current at 10 Hz is 3 pA/√Hz.

(1) Input Noise

According to the specification, the input noise is 100 nV/√Hz.

By simulation, the attenuation of each stage is 0.166, making a total attenuation of $(0.166)^3$ or 0.00457 with all three filters in place.

The output noise resulting from the input noise is therefore
100 nV/√Hz x 0.00457 = 0.457nV/√Hz.

This will result in an output noise current of
0.457/ 7.84K = **0.058 pA/√Hz**

(2) Ground Noise
As already mentioned, each channel functions as a true 4 terminal system. The input signals are balanced about ground. The bias currents for the inputs to this circuit are supplied by the input signals, and each subsequent stage is biased by the previous one. The dc voltage to ground at the outputs is therefore defined.
As the signals are not referred to any other ground line, there is no possibility of noise from external grounds being injected into the system.
The test input should never be left floating, as this may result in large offsets in the Test Mode. Instead, a dummy connector must be used to terminate it, with all pins connected together. This grounds the inputs in Test Mode, as pin 5 on the test connector is connected to local power supply 0v.

(3) EMC noise
The enclosure will act as a Gaussian screen. The box, as supplied, is floating, as the grounding scheme should be decided on a system basis.

(4) Component Noise
Details of the calculation of component noise are given in Appendix 1. It is shown that the calculated output noise current due to the components will be:

2 pA/√Hz

Total Overall noise
The total overall noise current from known sources at 10 Hz will therefore be:

$\sqrt{[(\text{Input noise})^2 + (\text{Component Noise})^2]}$

$=\sqrt{[(0.058)^2 + (2)^2]}$

= 2.0008 pA/√Hz at 10 Hz

This compares well with the specification of 3 pA/√Hz

7. MEASURED PERFORMANCE

7.1 Dynamic Range

Dynamic range measurements were made on UIM 3. A 10v peak sine wave was applied to the inputs of the unit, and the r.m.s voltage developed across a nominal 39 Ohm resistor connected to each channel output was measured. The r.m.s output current was calculated for each channel/

Results

10 Hz – no filters – equivalent to < 1Hz with filters in but easier to measure.

Channel	Resistor Value	Vout (V r.m.s)	I out (r.m.s)
1	39.14	0.0818	2.0899 mA
2	38.85	0.0811	2.0875 mA
3	39.14	0.0817	2.0874 mA
4	39.91	0.0812	2.0345 mA

All channels met the specification of 2 mA r.m.s dynamic range.

100Hz - all filters in.

Channel	Resistor Value	Vout (r.m.s)	I out (r.m.s)
1	39.14	0.179 mV	4.57uA
2	38.85	0.172 mV	4.24uA
3	39.14	0.179 mV	4.57uA
4	39.91	0.179 mV	4.48uA

This is within reasonable agreement with the theoretical results.

7.2 Noise

Output noise was measured on two completed units (UIM1 and UIM2). Tests on UIM 1 were conducted using the internal noise monitor. Tests on UIM 2 were performed using the SR560 amplifier instead. The test using the Noise monitor yielded the equivalent of 3pA/√Hz.

The appropriate section of the test report for UIM 2 is given in Appendix 2. Measurements on UIM 2 gave slightly better results.

8. CONCLUSION

The dynamic range and noise specifications were shown to meet the specification by calculation and measurement.

The dynamic range at 100 Hz theoretically falls short of the specification when all three filters are switched in, but meets the specification with two filters switched in

9. REFERENCES

(1) T060067-00-C AdL Quad Suspension UK Coil Driver Design requirements

APPENDIX 1

Calculation of Component Noise

The noise from the earlier stages is attenuated at 10 Hz by the low pass filters. It may be shown that the components in the first two stages contribute a total of **0.304nV/Hz** of noise to the output noise voltage, when the filters are in circuit.

Amplifier noise

The sum of the differential noise from the two output operational amplifiers was calculated to be **3.98nV/√Hz**, including the effects of both voltage and current noise.

Filter Resistor noise

The resistors in the last filter stage were calculated to generate **10.24nV/√Hz** of differential noise, when the output amplifier gain is taken into account.

The sum of these three noise sources is

$\sqrt{[(\text{Noise from first stages})^2 + (\text{Amplifier Noise})^2 + (\text{Component Noise})^2]}$

$\sqrt{[(0.304)^2 + (3.98)^2 + (10.24)^2]}$

= 10.99nV/Hz

This will result in a noise current of (10.99 / 7.84) pA/√Hz

= **1.402 pA/√Hz**

Output resistor Noise

The output resistance of 3.9k +3.9k + 40 ohms = 7.84k would generate Johnson noise voltage of 11.2 nV/√Hz, resulting in a noise current of (11.2/7.84) =

1.42pA/√Hz.

Total Noise Component Noise Estimate

The total noise is therefore the sum of these figures, giving:

$\sqrt{[(1.402)^2 + (1.42)^2]}$

Noise Current = **1.995pA/√Hz**

Total component noise is therefore effectively

2pA/√Hz

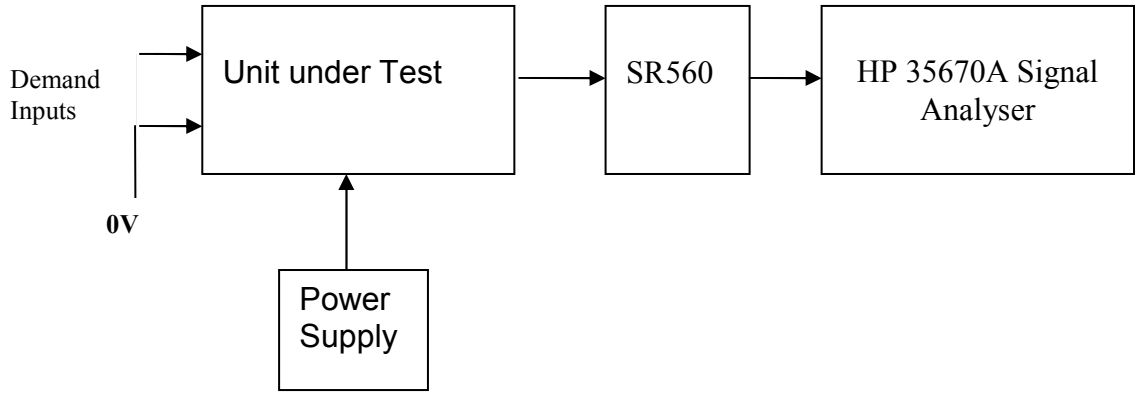
APPENDIX 2

Noise Measurements

The noise measurement section from the test report for the UIM 2 unit test follows.

Test Method

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use the noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz, and readings should be made when the ambient noise is low. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



Test Results

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-152.6	-93	-153
Ch2	-152.6	-94.2	-154.2
Ch3	-152.6	-93.5	-153.5
Ch4	-152.6	-93.45	-153.45

Interpretation.

The specification at 10 Hz is a noise current of 3 pA per root Hz. The total load resistance is 7.8k. The permitted noise voltage from the amplifiers is therefore 23.4 nA/ /√Hz or -152.6 dB. The SR560 is set to a gain of 1000 (60dB) so 60dB needs to be subtracted from the reading.
It will be seen that all channels were within specification.