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TOP Drive Unit Design Description

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This is an internal working note
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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

DESIGN AND MANUFACTURE OF THE TOP DRIVER UNIT

CONTENTS

1, INTRODUCTION

This document describes the philosophy and methods used to produce the TOP Coil Drive Electronics Unit for Advanced LIGO. Estimates of the performance are given, together with performance measurements from the pre-production units.

1.1 Context

The TOP Driver unit contains four channels of amplification and filtering. The outputs from the unit control the position of the TOP stage in the Advanced LIGO Quad Suspension.

The output currents from the unit energise four coils which attract magnets mounted on the TOP section of the suspension, giving a force which moves the TOP section to the desired position.

Monitoring circuits are included in the unit to monitor its activity. The monitor circuits are housed on a separate PCB within the unit.

2. MONITORS

2.1 Specification

The following monitors are required by the specification [(1)]:-

(1) Output voltage monitors which cover the full dynamic range of the outputs.

(2) Monitors capable of seeing the noise floor of the outputs for 10Hz<freq<1 KHz

(3) Monitors of fast instantaneous measurement of the output current.

(4) Monitors of the RMS current with a time constant of 1 second capable of monitoring the full current range of the drivers

(5) Status (position) monitors/read backs for all switches used in the design.

2.2 Monitors Provided

(1) The Output Voltage Monitor. A monitor which measures the voltage between the two output operational amplifiers is provided. It has a gain of 1/3, so the highest possible output voltage within the constraints of the power rails (+/- 15v) gives a monitor output of 10v.

(2) The Noise Monitor. This is a high gain AC coupled amplifier with a low noise front end. The corner frequency of each of the stages is 5 Hz.

(3) The Output Current monitor. This is a four input summing amplifier which measures the sum of the voltages across the two output resistors. It has a gain of 1/3.

(4) The R.M.S monitor. A true RMS integrated circuit is used to convert the output of the current monitor into an RMS value. Its overall gain is 1, which combined with the current monitor gain, gives an overall gain of 1/3.

The settling time of this circuit varies with the applied input voltage.

(5) Status outputs for all switches. In the case of the filter relays, a spare relay contact is used to indicate the position of the relay. In the case of the test relay, all the contacts on the relay are already used, so a transistor circuit was added to monitor the state of the test relay coil voltage.

2.3 Monitor Design Details

2.3.1 Voltage Monitor

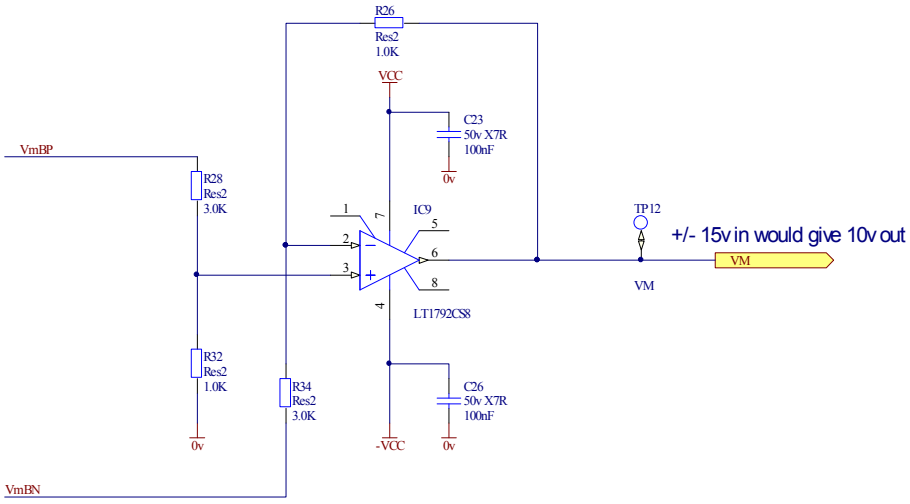

Fig 1 The Voltage Monitor Circuit

The Voltage Monitor Circuit consists of a summing amplifier, which subtracts the positive amplifier output from the negative amplifier output. This gives the total output voltage. The voltage gain of the circuit is ⅓ , which means that if the inputs are at their maximum voltage, +/-15v (rail voltage) the output is +10v.
There is one Voltage Monitor circuit per Drive Amplifier channel.

2.3.2 Current Monitor and R.M.S Circuit
Current Monitor

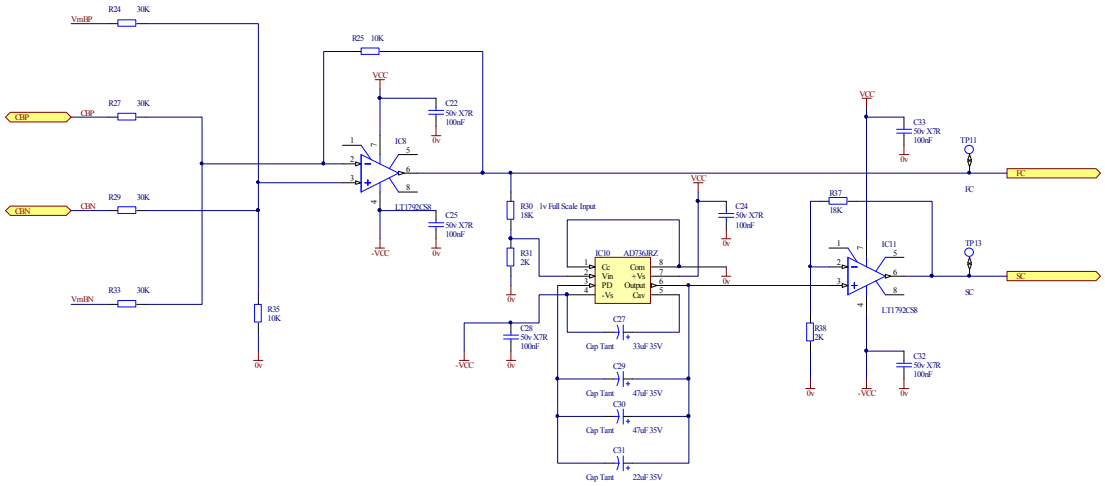

Fig 2 The Current Monitor and RMS circuit

The Current Monitor section consists of a 4 input Summing Amplifier. This calculates the voltages across the two output resistors, as this is proportional to the instantaneous output current. The sum performed is:

(Pos. Amplifier Output – Pos. Coil Voltage) + (Neg. Coil Voltage - Neg. Amplifier Output).

The gain of the amplifier is set to ⅓, which means that if the inputs are at their maximum possible voltage, the output is +10v.

1 volt out of the voltage monitor represents 1.5 volts across each driver output resistor.
As the output resistors are each 40 Ohms, this represents a current of 37.5 mA.
100mA out would therefore produce a current monitor output of 2.66 volts.

RMS

The r.m.s circuit uses a true r.m.s convertor integrated circuit type AD736, to convert the output signal from the Current Monitor into an r.m.s. measurement. As large signals into the AD736 results in a reduced accuracy, the circuit is preceded by a 10:1 attenuator and followed by a 10x gain stage. This gives the r.m.s circuit the same overall gain as the current monitor. The settling time of this circuit varies with the applied voltage:

IC Input Voltage	Output from the Amplifier	Settling time
10mV	0.1 volt	1 Second
100mV	1 volt	100milliseconds
1V	10 volts	10 milliseconds

There is one current monitor and r.m.s circuit per Drive Amplifier channel, and there are four channels in each TOP Drive Unit.

2.3.3 Noise Monitor

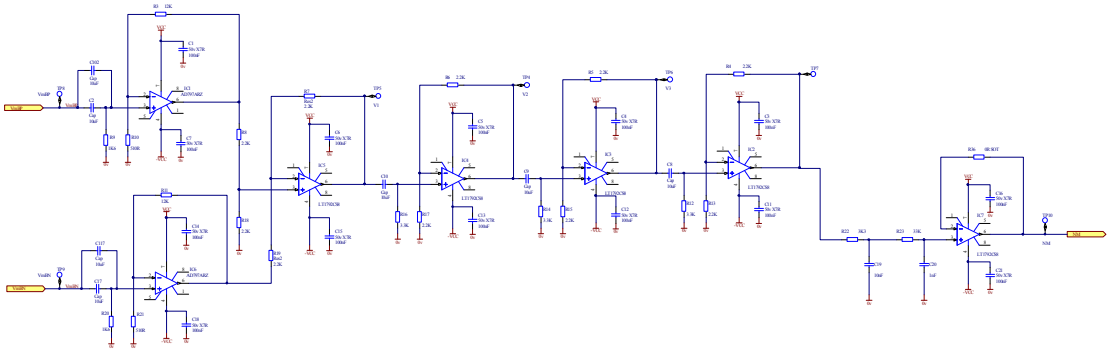

Fig 3 The Noise Monitor circuit

The Noise Monitor circuit is designed to amplify the ac noise voltage across the Drive Amplifier output, while rejecting dc signals.

An ac coupled, low noise differential amplifier front end is followed by a series of 3 gain stages, each ac coupled. Each stage has a gain of 2, and a corner frequency of 5Hz. These high pass stages are followed by a two pole low pass filter stage, each stage having a corner frequency of 5 KHz.

3. COIL DRIVE CIRCUITS
3.1 Specification

3.1.1 Input Signals
The specification [1] defines the following:

Input signals: Voltage Range: +/-10V ($20V_{p-p}$)
Noise Voltage: 100nV/√Hz over the frequency range of interest for the coil driver.

3.1.2 Dynamic range
The maximum output current for each top coil driver shall be +/-200mA continuous.

3.1.3 Noise

Frequency	Current Noise Requirement
1 Hz	1 nA/√Hz
10 Hz	73 pA/√Hz
100 Hz	1000 nA/√Hz
1000 Hz	1000 nA/√Hz

4. COIL DRIVE DESIGN PHILOSOPHY

4.1 Dynamic range

Achieving the required dynamic range requires a high current driver chip, as a continuous current of +/- 200mA is required. As switched mode operation is not suitable, the power dissipation of the output devices will be considerable. As noise is temperature dependant, the choice was made to limit temperature rises by conducting heat to the chassis via an aluminium bar.
A type OPA548 driver was used. This device has a maximum continuous output current of 3 Amps. As only 200 mA is required, this leaves a large margin, which will make for reliable operation. It also features a current limit, and is housed in a convenient 7 lead TO220 package.
As driver devices are all fairly noisy, the OPA548 is enclosed in a feedback loop with an AD797 to reduce noise. A bandwidth limiting compensating capacitor is connected in the feedback path of the AD797 to ensure stability.
The maximum output current is controlled by two series power resistors in parallel with two series trimming resistors.

4.2 Noise

The main difficulty in meeting the specification is the noise requirement at 10 Hz. The noise level is required to be less than 73 pA/√Hz.

Noise will emanate from several different sources.

The main noise sources are:
(1) Input noise
(2) Ground noise
(3) EMC
(4) Component Noise

(1) Input Noise

As a high dynamic range is required at low frequencies, but a low noise level is required at 10Hz, input noise at 10 Hz is attenuated by means of two low pass filter stages. The first filter stage may be remotely switched in or out as required, permitting a low noise mode or a high dynamic range mode to be selected.

(2) Ground noise

Ground noise is always a problem in large complex low noise systems, particularly when there are long cable runs. LIGO is a very large, very complex system with extremely long cable runs, and very tight noise requirements.

This problem is avoided by keeping the signals independent of ground. As the input signals are symmetrical about ground, it is possible to engineer a true four wire system, by using two independent chains of amplifiers. This design also avoids any ground noise problems internal to the unit.

(3) EMC
EMC pick up on the amplifier outputs might also be a problem. The risk of this potential problem has been reduced, as the balanced outputs have identical output impedances. Any noise voltages induced by EMC should be almost entirely common mode, appearing equally across both coil terminals, and so resulting in no noise current in the coils.

(4) Component Noise
Component noise will be generated by all components in the unit. Resistors will unavoidably generate Johnson noise. Low noise metal film resistors are used in these units to minimise voltage dependant noise.

The operational amplifier types used in this design are carefully selected for their low noise specifications.
The resistor value which generates the zero in the second filter is lower than in the first filter, being 270 Ohms, as the Johnson noise from this resistor is one of the dominant noise sources. The capacitor value in this filter is 20uF, which means that the 4K3 input resistors give a 1Hz corner frequency, while minimising Johnson noise and noise due to input current noise on the AD797 op amps.

Ceramic capacitors are not used in the signal paths, as they are considered to be a possible source of microphonic noise.

5. COIL DRIVER DESIGN DETAILS

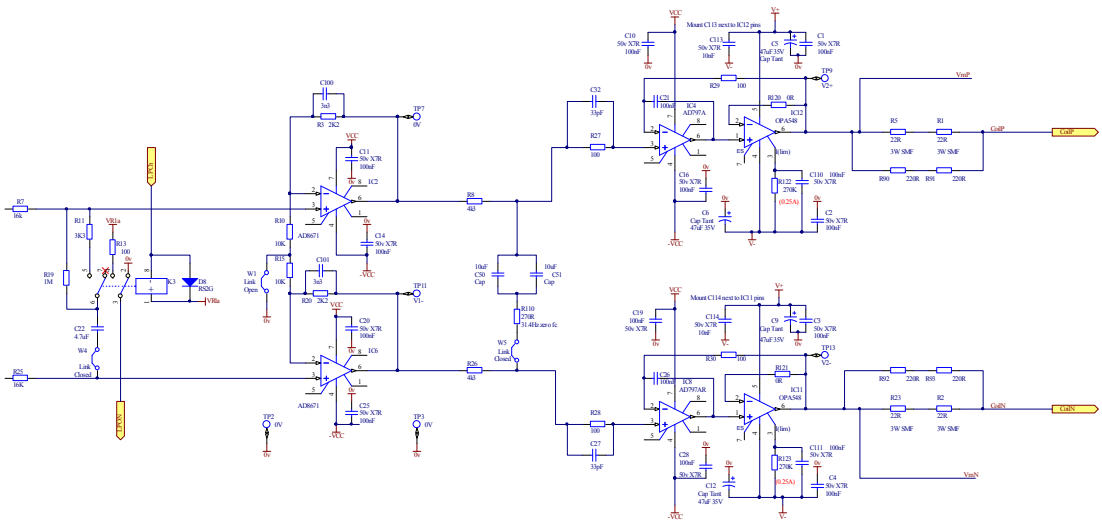

Fig 1. A TOP Driver Channel.

The above diagram shows the active section of a channel of a TOP Driver. There are four such channels in each TOP Driver Unit.

The circuit consists of two low pass filters stages, the first of which is followed by a buffer amplifier with a gain of 1.2. As specified in the Design Requirements Document [(1),] the 1Hz pole in the first filter is followed by a zero at 10 Hz. This filter stage has a relay which may be switched in or out as

required, to configure the operational mode of the unit. The second filter stage is not switchable, allowing more flexibility in the pole/zero ratio, permitting noise to be minimised.

The circuit is a true four terminal design.

The output resistors (40 Ohms) on each of the two outputs define the maximum output current.

6. THEORETICAL PERFORMANCE

6.1 Dynamic range at Low Frequencies

As the input voltage is specified as 10V, and the voltage gain of the circuit is 1.2, the voltage swing of each output terminal will be +/-12v. As each output resistor is 40 Ohms, and the OSEM coil resistance is 40 Ohms, the total output resistance is:

(40 Ω + 40 Ω + 40 Ω) = 120 Ohms

The voltage across this resistance will be 24v maximum, so the current =

24/120 = 200 mA

This meets the maximum output current requirement. .

6.2 Noise Requirements

The permitted noise current at 10 Hz is 73 pA/√Hz.

(1) Input Noise

According to the specification, the input noise is 100 nV/√Hz.

By simulation, the attenuation of the first stage at 10 Hz is 0.133, and the second stage is 0.095 making a total attenuation of 0.095 x 0.133 = 0.0126 with both filters in place.

The output noise resulting from the input noise is therefore
100 nV/√Hz x 0.0126 = 1.26nV/√Hz.

This will result in an output noise current of
1.26/120 = **10.5 pA/√Hz**

(2) Ground Noise

As already mentioned, each channel functions as a true 4 terminal system. The input signals are balanced about ground. The bias currents for the inputs to this circuit are supplied by the input signals, and each subsequent stage is biased by the previous one. The dc voltages to ground are therefore defined throughout the circuit.
As the signals are not referred to any other ground line, there is no possibility of noise from external grounds being injected into the system.
The test input should never be left floating, as this may result in large offsets in the Test Mode. Instead, a dummy connector must be used to terminate it,

with all pins connected together. This grounds the inputs in Test Mode, as pin 5 on the test connector is connected to local power supply 0v.

(3) EMC noise
The enclosure will act as a Gaussian screen. The box, as supplied, is floating, as the grounding scheme should be decided on a system basis.

(4) Component Noise
Calculation of component noise show that the output noise current is:

59 pA/√Hz

Total Overall noise
The total overall noise current from known sources at 10 Hz will therefore be:

$\sqrt{[(\text{Input noise})^2 + (\text{Component Noise})^2]}$

$=\sqrt{[(10.5)^2 + (59)^2]}$ pA/√Hz

= 59.9 pA/√Hz at 10 Hz

This is within the specification of 73 pA/√Hz

7. MEASURED PERFORMANCE

7.1 Dynamic Range

A sine wave with a peak value of 10 volts was applied to each input, and the voltage across the load resistor was measured. The exact values of the load resistors were measured, and the r.m.s output currents were calculated. This was compared with the expected r.m.s output.
In all cases, the measurements exceeded the specification, the target value being 141.4 mA r.m.s.
A typical measurement was 145mA r.m.s

7.2 Noise

Measurements were made using the HP35670A Signal Analyser, preceded by a SR560 amplifier in differential mode with a gain of 1000.
The specified noise represents -161.15 dB. Measurements generally ranged from -160dB to -162dB for the first 6 units.

8. CONCLUSION

The dynamic range calculations and measurements met the specification.
The noise calculations met the specification at 10 Hz.
The measurements were generally within 1dB of the specifications.

9. REFERENCES

(1) T060067-00-C AdL Quad Suspension UK Coil Driver Design requirements