LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

Drive Card ID……Q_TOP47P………
Monitor Card ID…Mon82…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

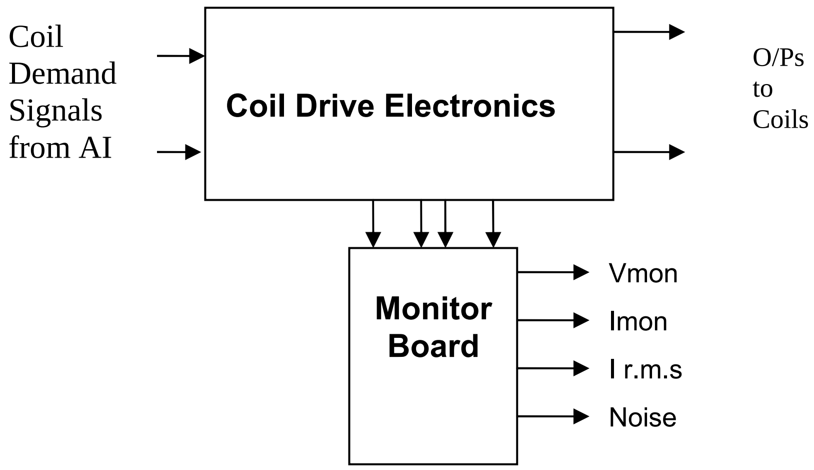


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P47…………………….Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..16/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

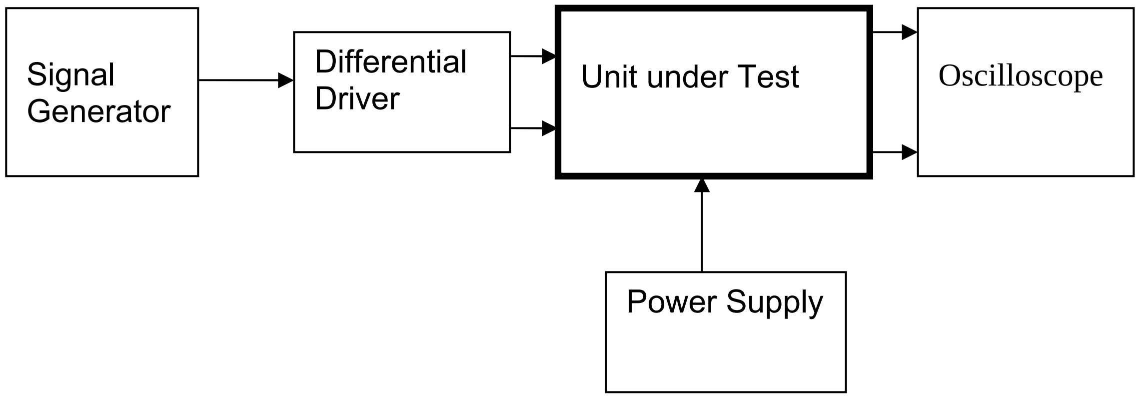
Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.018	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.012	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.014	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.022	√

Unit……………..Q_TOP_P47…………………..Serial No …………………………….
Test Engineer…..Xen…………………
Date……………..25/5/10……………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		2.4	2.9μV√Hz	√
2		1.33	2.9μV√Hz	√
3		1.36	2.9μV√Hz	√
4		1.50	2.9μV√Hz	√

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..16/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..16/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

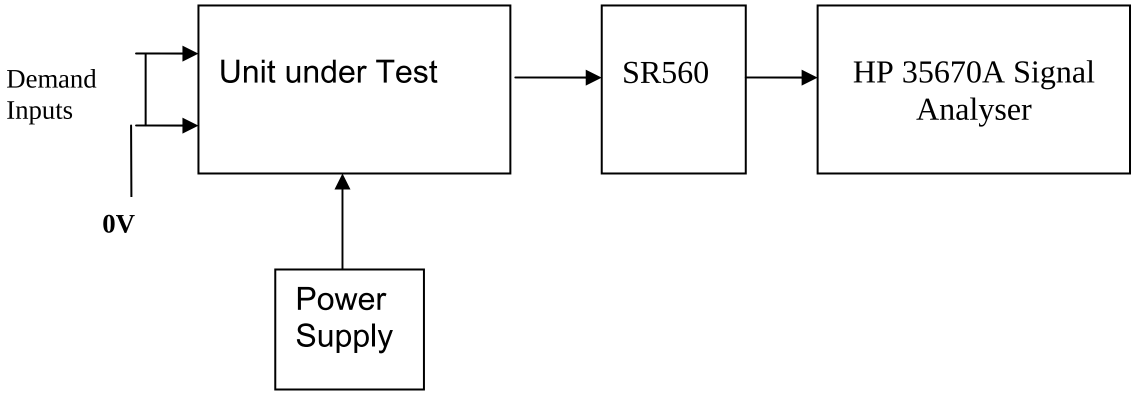
The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.36	√	**CH1 IC1**	44.3	√
CH1 Negative			**CH1 IC5**	41.1	√
CH2 Positive	24.37	√	**CH2 IC1**	42.8	√
CH2 Negative			**CH2 IC5**	42.8	√
CH3 Positive	24.37	√	**CH3 IC1**	44.8	√
CH3 Negative			**CH3 IC5**	41.6	√
CH4 Positive	24.37	√	**CH4 IC1**	42.1	√
CH4 Negative			**CH4 IC5**	43.6	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100	-160
Ch2	-161.15dB	-101	-161
Ch3	-161.15dB	-101.4	-161.4
Ch4	-161.15dB	-100	-160

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P47……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.58	141.6mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………QTOP47P……………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP47P
Driver board ID	QTOP47P
Driver board Drawing No/Issue No	D0902747-V3
Driver board Serial Number	QTOP47P
Monitor board ID	MON82
Monitor board Drawing No/Issue No	D070480-04-K
Monitor board Serial Number	MON82

10. Check the security of any modification wires.   None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

Technical
T e c h n i c a l ┌€< T h e U n i v e r s i t y o f
B i r m i n g h a m n

◘ ┬

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R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..5/7/10……..…………

Drive Card ID……Q_TOP1P………
Monitor Card ID…Mon149…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

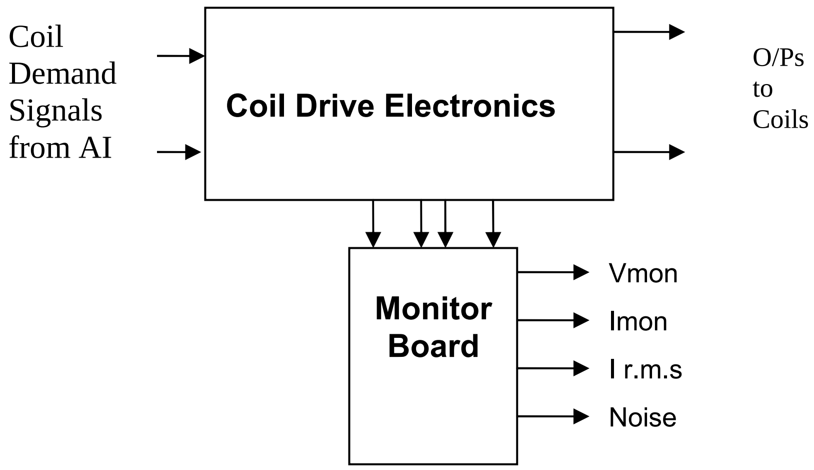


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen…….…………..
Date……………..5/7/10……..…………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	**Agilent**	**33120A**	**MY40016550**
Oscilloscope	**Tenma**	**72-6800**	**0900889**
Power supply	**Digimess**	**BP3002**	**211259**
DVM	**Fluke**	**115**	
Signal Analyser	**HP**	**35670A**	
Pre-amplifier	**Stanford Systems**	**SR560**	
DVM	**TENMA**	**72-7730**	
V/I calibrator	**Time Electronics**	**1044**	

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on all channels.

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V			
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V			
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

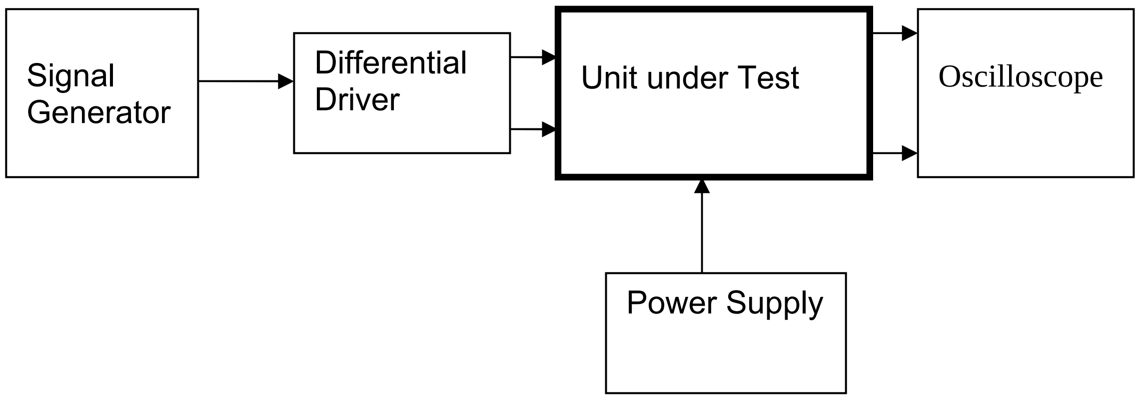
Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
540mA	490mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.01V	√
	Pin 1	RMS Current	1v dc	1.01V	√
2	Pin 5	Current Monitor	1v r.m.s	1.01V	√
	Pin 4	RMS Current	1v dc	1.01V	√
3	Pin 8	Current Monitor	1v r.m.s	1.01V	√
	Pin 7	RMS Current	1v dc	1.01V	√
4	Pin 11	Current Monitor	1v r.m.s	1.01V	√
	Pin 10	RMS Current	1v dc	1.01V	√

Unit……………..Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..5/7/10……..…………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32V	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.33V	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32V	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32V	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9µV√Hz out.

Ch.	**Output (µV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.66	2.9µV√Hz	√
2		1.48	2.9µV√Hz	√
3		1.36	2.9µV√Hz	√
4		1.49	2.9µV√Hz	√

Unit……………..Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..29/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.7		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.7		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.7		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.7		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…….……………
Date……………..29/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

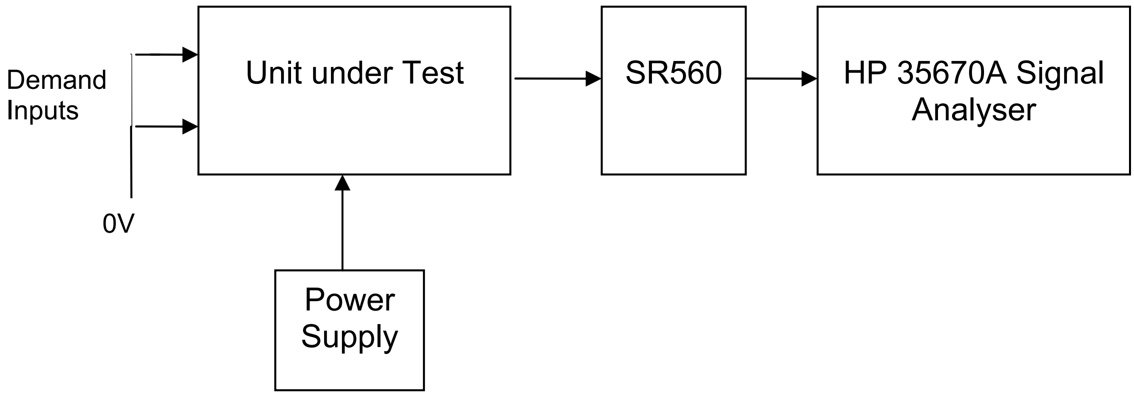
The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.60V	√	**CH1 IC1**	45.0	√
CH1 Negative			**CH1 IC5**	46.2	√
CH2 Positive	24.60V	√	**CH2 IC1**	47.0	√
CH2 Negative			**CH2 IC5**	46.7	√
CH3 Positive	24.60V	√	**CH3 IC1**	47.7	√
CH3 Negative			**CH3 IC5**	47.7	√
CH4 Positive	24.60V	√	**CH4 IC1**	44.5	√
CH4 Negative			**CH4 IC5**	53.5	√

Unit……………..Q_TOP_P48…………………..Serial No ……………………………
Test Engineer…..Xen…….…………..
Date……………..5/7/10……..………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-102.0	162.0
Ch2	-161.15dB	-99.8	-159.8
Ch3	-161.15dB	-101.7	-151.7
Ch4	-161.15dB	-101.6	-161.6

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P48……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.5	5.6	141.7	>200mA	>141.4mA	√
2	39.4	5.6	142.1	>200mA	>141.4mA	√
3	39.5	5.6	141.7	>200mA	>141.4mA	√
4	39.3	5.6	142.5	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit………QTOP1P……………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP1P
Driver board ID	QTOP1P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP1P
Monitor board ID	MON149
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON149

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 **Advanced LIGO UK** 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

Drive Card ID……Q_TOP2P………
Monitor Card ID…Mon174..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

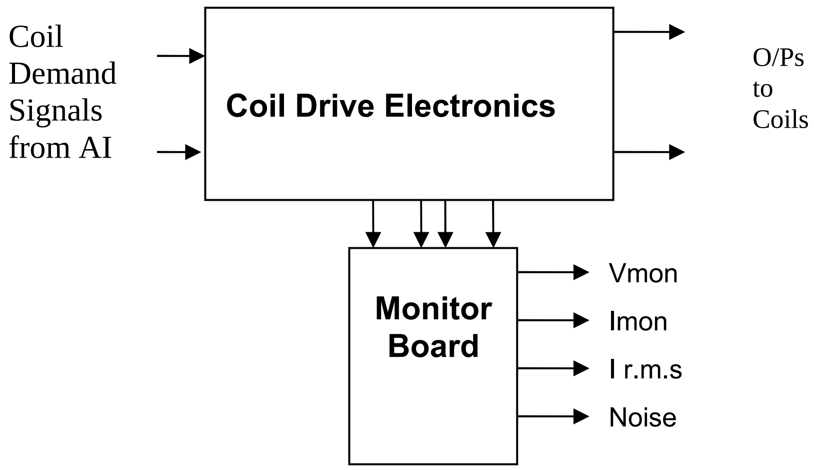


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..30/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced with the AD8671 op-amp on all channels.

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

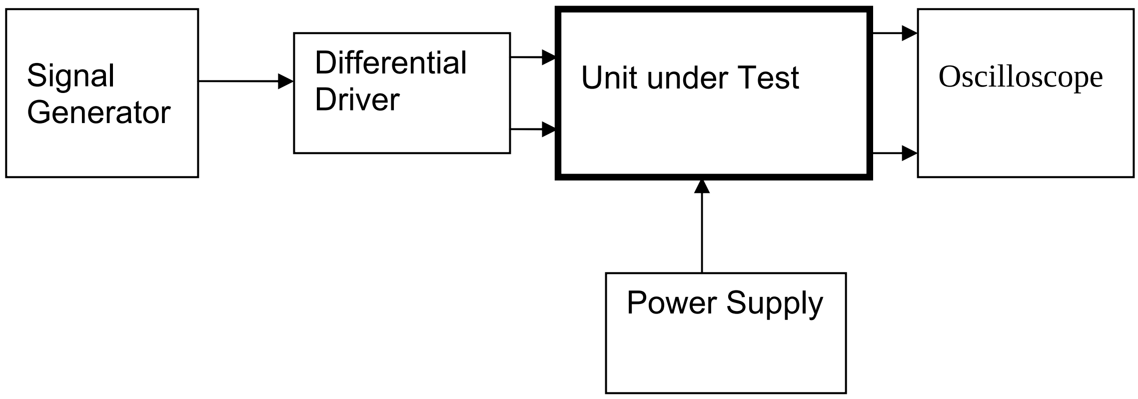
Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..30/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..30/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.019	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.022	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.013	√

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..30/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in µV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9µV√Hz out.

Ch.	**Output (µV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.21	2.9µV√Hz	√
2		1.62	2.9µV√Hz	√
3		2.37	2.9µV√Hz	√
4		2.62	2.9µV√Hz	√

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

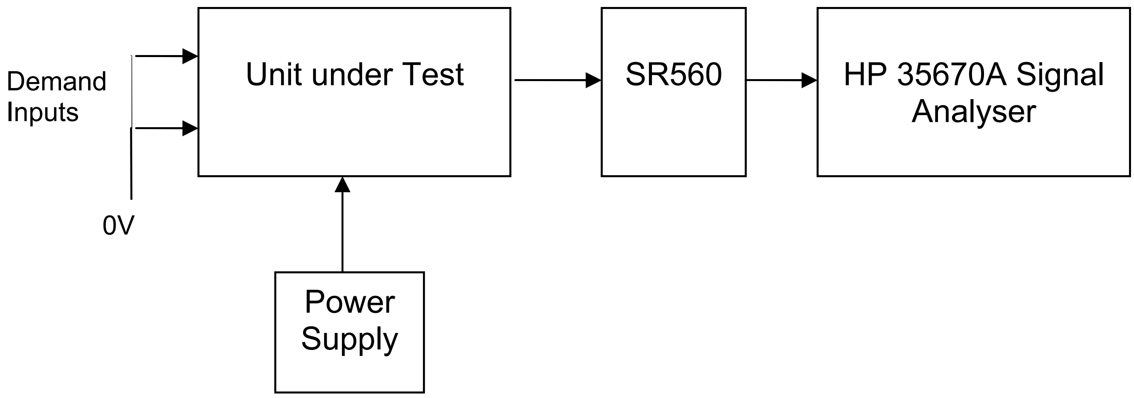
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.52	√	**CH1 IC1**	45.5	√
CH1 Negative			**CH1 IC5**	45.5	√
CH2 Positive	24.52	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	52.3	√
CH3 Positive	24.52	√	**CH3 IC1**	46.7	√
CH3 Negative			**CH3 IC5**	49.1	√
CH4 Positive	24.51	√	**CH4 IC1**	45.5	√
CH4 Negative			**CH4 IC5**	51.3	√

Unit……………..Q_TOP_P2…………………..Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-103.1	-161.3
Ch2	-161.15dB	-101.7	-161.7
Ch3	-161.15dB	-101.5	-161.5
Ch4	-161.15dB	-99.4	-159.4

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit………………Q_TOP_P2……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..30/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP2P..........................Serial No ....
Test Engineer ....RMC
Date 27/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP2P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP2P
Driver board Serial Number	QTOP2P
Monitor board ID	MON174
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON174

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

Drive Card ID……Q_TOP3P………
Monitor Card ID…Mon141..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

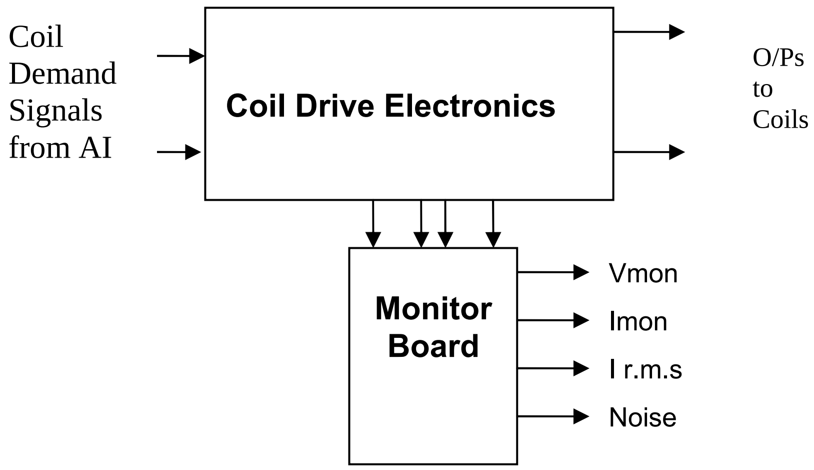


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH 1.

Unit……………….Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

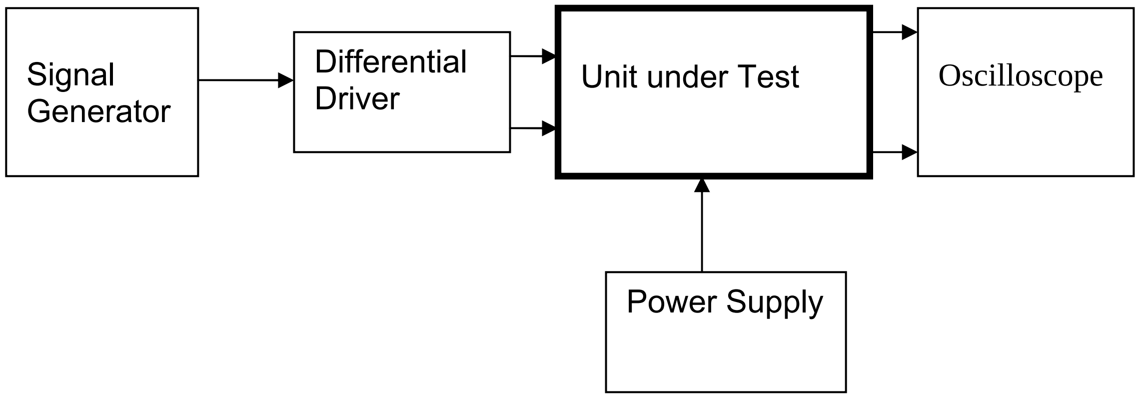
Unit………………Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit..................Q_TOP_P3........................Serial No ....
Test Engineer.....Xen.....................
Date.................2/7/10..................

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.012	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.016	√
3	Pin 8	Current Monitor	1v r.m.s	1.012	√
	Pin 7	RMS Current	1v dc	1.018	√
4	Pin 11	Current Monitor	1v r.m.s	1.011	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit……………..Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.98	2.9μV√Hz	√
2		1.28	2.9μV√Hz	√
3		1.07	2.9μV√Hz	√
4		1.69	2.9μV√Hz	√

Unit……………….Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..Q_TOP_P3……………………Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

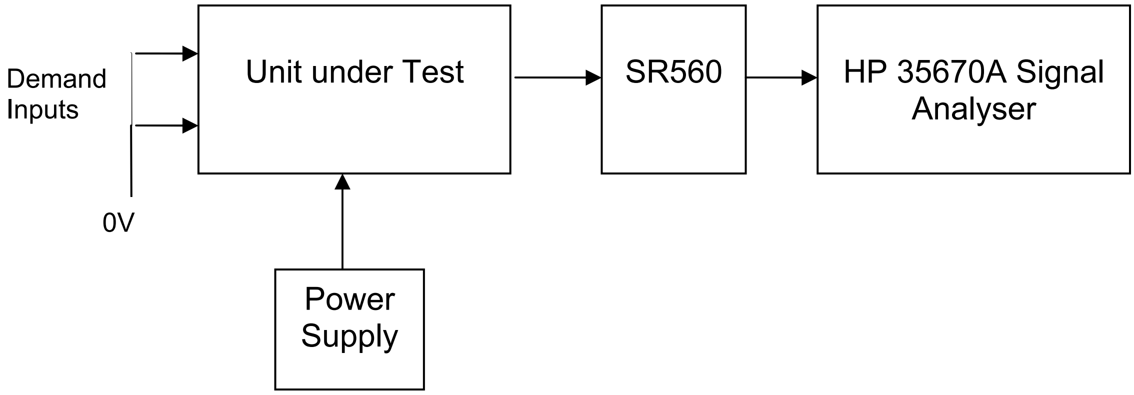
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.40	√	**CH1 IC1**	40.1	√
CH1 Negative			**CH1 IC5**	42.8	√
CH2 Positive	24.40	√	**CH2 IC1**	43.6	√
CH2 Negative			**CH2 IC5**	45.3	√
CH3 Positive	24.40	√	**CH3 IC1**	42.3	√
CH3 Negative			**CH3 IC5**	43.3	√
CH4 Positive	24.40	√	**CH4 IC1**	39.4	√
CH4 Negative			**CH4 IC5**	42.8	√

Unit……………….Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.2	-161.2
Ch2	-161.15dB	-100.8	-160.8
Ch3	-161.15dB	-102.5	-162.5
Ch4	-161.15dB	-101.0	-161.0

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P3……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.59	141.2mA	>200mA	>141.4mA	√
2	39.4	5.60	142.1mA	>200mA	>141.4mA	√
3	39.3	5.58	142.0mA	>200mA	>141.4mA	√
4	39.4	5.59	141.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..................QTOP3P..................Serial No ....
Test Engineer ....RMC
Date 28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP3P
Driver board ID	QTOP3P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP3P
Monitor board ID	MON141
Monitor board Drawing No/Issue No	D070_4_K
Monitor board Serial Number	MON141

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2	Advanced LIGO UK	30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..6/7/10..………………

Drive Card ID……Q_TOP4P…….……
Monitor Card ID…Mon174…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

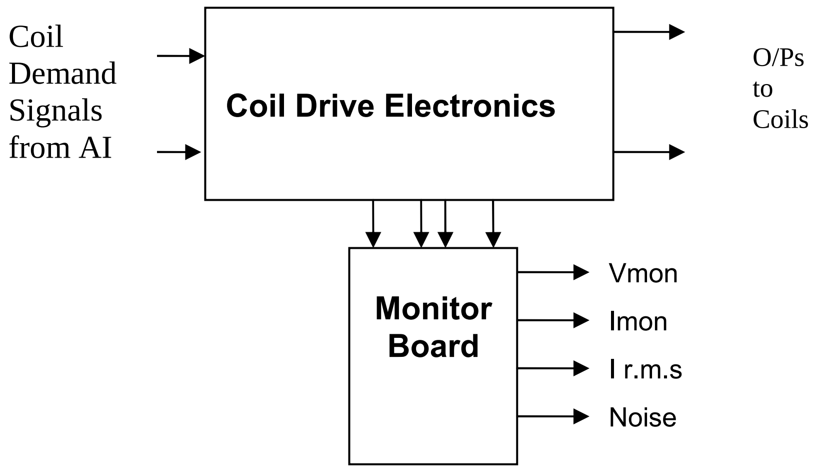


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..6/7/10..………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P49…………………….Serial No ………………………………
Test Engineer…..Simon Pyatt…….…………..
Date……………..1/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V			
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V			
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

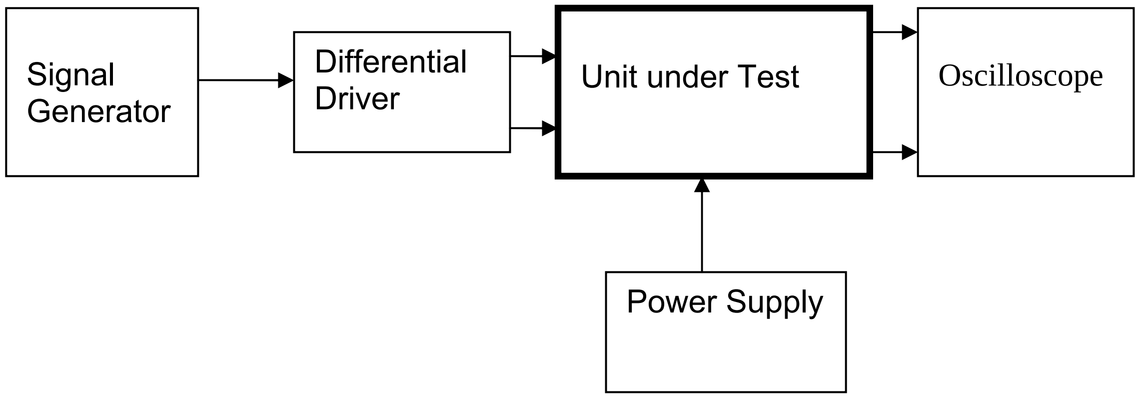
Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
540mA	490mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..5/7/10..………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.018	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.010	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit………………Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..5/7/10..………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.24	2.9μV√Hz	√
2		1.63	2.9μV√Hz	√
3		0.92	2.9μV√Hz	√
4		0.91	2.9μV√Hz	√

Unit……………….Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..5/7/10..………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit……………..Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..6/7/10..………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.44	√	**CH1 IC1**	39.7	√
CH1 Negative			**CH1 IC5**	43.8	√
CH2 Positive	24.43	√	**CH2 IC1**	42.6	√
CH2 Negative			**CH2 IC5**	43.1	√
CH3 Positive	24.43	√	**CH3 IC1**	45.3	√
CH3 Negative			**CH3 IC5**	45.5	√
CH4 Positive	24.44	√	**CH4 IC1**	41.8	√
CH4 Negative			**CH4 IC5**	42.6	√

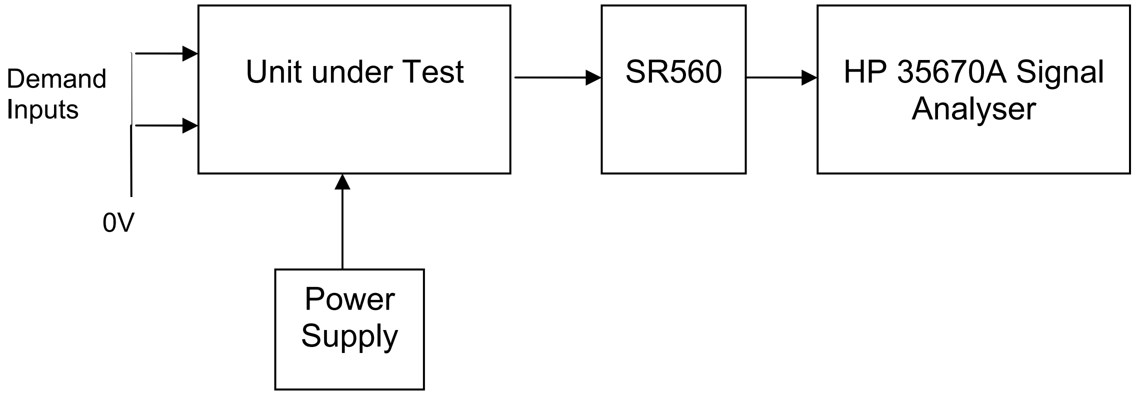
Unit..................Q_TOP_P4........................Serial No ....
Test Engineer.....Xen.......................
Date.................5/7/10....................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.0	-160.0
Ch2	-161.15dB	-101.4	-161.4
Ch3	-161.15dB	-101.5	-161.5
Ch4	-161.15dB	-102.2	-162.2

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………….Q_TOP_P4……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..6/7/10..……………….

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………QTOP4P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP4P
Driver board ID	QTOP4P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP4P
Monitor board ID	MON142
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON142

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..30/6/10……………..

Drive Card ID……Q_TOP5P………
Monitor Card ID…Mon217..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

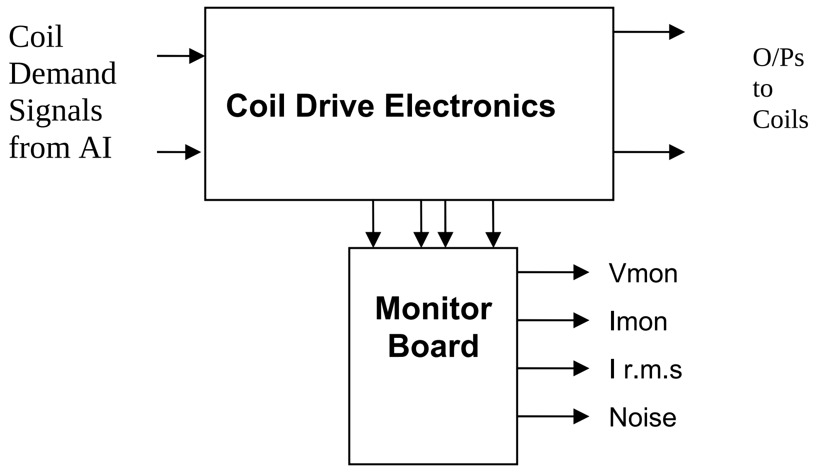


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..30/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

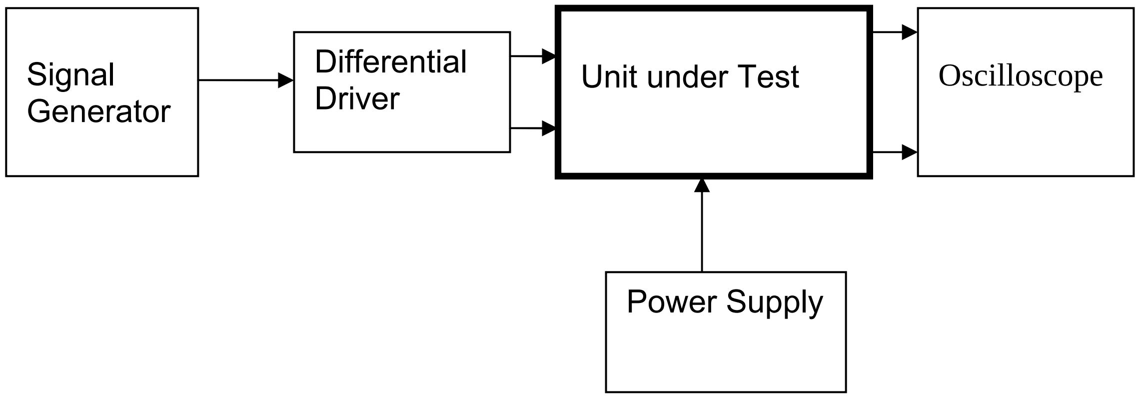
Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..29/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..29/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.025	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.014	√
3	Pin 8	Current Monitor	1v r.m.s	1.016	√
	Pin 7	RMS Current	1v dc	1.020	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.018	√

Unit………………Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.05	2.9μV√Hz	√
2		0.96	2.9μV√Hz	√
3		0.94	2.9μV√Hz	√
4		1.35	2.9μV√Hz	√

Unit……………..Q_TOP_P5…………………..Serial No …………………………….
Test Engineer…..Xen……………………
Date……………..30/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P5…………………..Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..30/6/10……………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.45	√	CH1 IC1	44.8	√
CH1 Negative			CH1 IC5	50.4	√
CH2 Positive	24.45	√	CH2 IC1	47.2	√
CH2 Negative			CH2 IC5	50.1	√
CH3 Positive	24.46	√	CH3 IC1	44.3	√
CH3 Negative			CH3 IC5	50.1	√
CH4 Positive	24.45	√	CH4 IC1	44.3	√
CH4 Negative			CH4 IC5	49.1	√

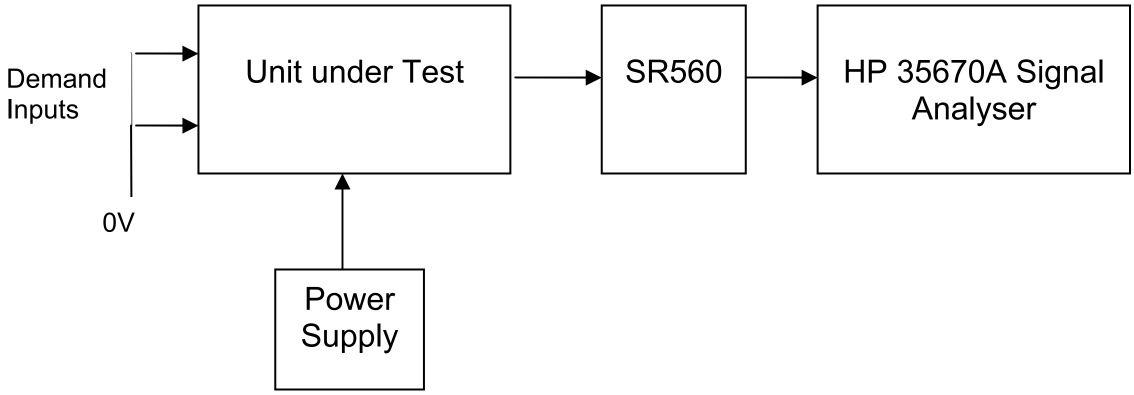
Unit……………..Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..29/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.2	-159.2
Ch2	-161.15dB	-98.3	-158.3
Ch3	-161.15dB	-100.8	-160.8
Ch4	-161.15dB	-101.2	-161.2

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P5……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..30/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTPOP5P....................Serial No ....
Test Engineer ....RMC
Date 28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP5P
Driver board ID	QTOP5P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP5P
Monitor board ID	MON217
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON217

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

Drive Card ID……Q_TOP6P………
Monitor Card ID…Mon176..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

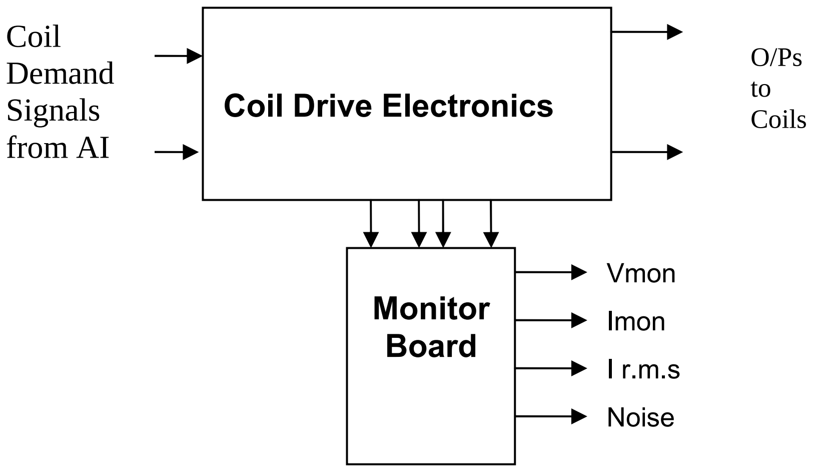


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Unit………………Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

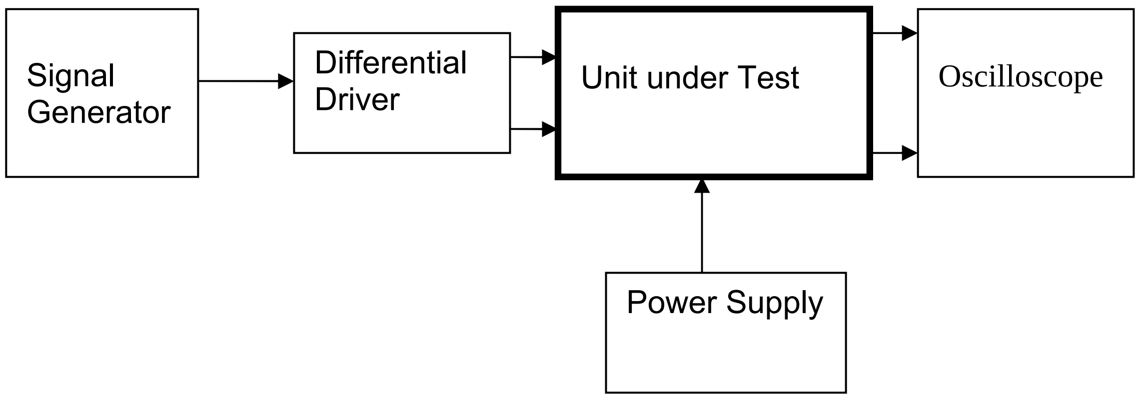
Unit……………..Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.017	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.012	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.019	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.013	√

Unit………………Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.96	2.9μV√Hz	√
2		1.06	2.9μV√Hz	√
3		1.32	2.9μV√Hz	√
4		1.19	2.9μV√Hz	√

Unit……………..Q_TOP_P6…………………..Serial No ……………………………..
Test Engineer…..Xen…………………
Date……………..5/7/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..Q_TOP_P6……………………Serial No ………………………………
Test Engineer…..Xen………………..
Date……………..5/7/10……………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.42	√	CH1 IC1	44.3	√
CH1 Negative			CH1 IC5	44.0	√
CH2 Positive	24.42	√	CH2 IC1	45.5	√
CH2 Negative			CH2 IC5	43.1	√
CH3 Positive	24.42	√	CH3 IC1	45.5	√
CH3 Negative			CH3 IC5	46.0	√
CH4 Positive	24.42	√	CH4 IC1	43.1	√
CH4 Negative			CH4 IC5	47.0	√

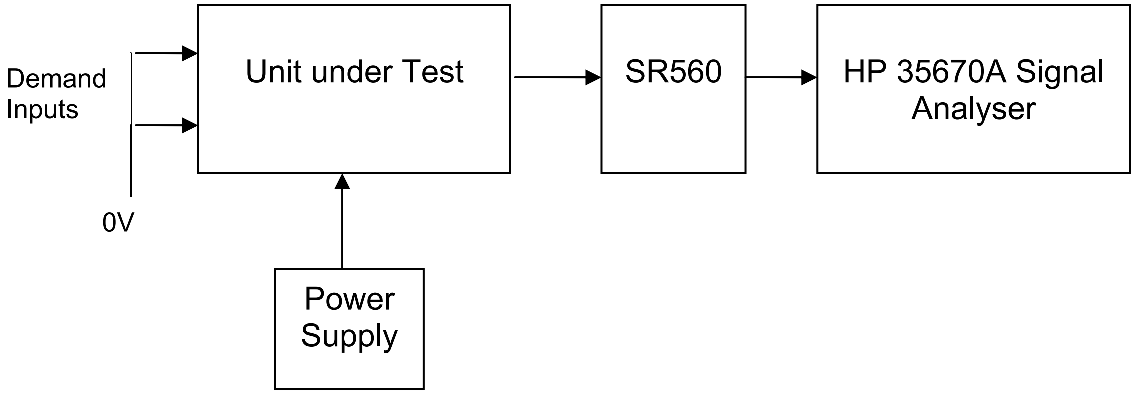
Unit……………..Q_TOP_P6……………………Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..5/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-102.1	-162.1
Ch2	-161.15dB	-99.7	-159.7
Ch3	-161.15dB	-98.4	-158.4
Ch4	-161.15dB	-101.4	-161.4

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P6…………………..Serial No ……………………………..
Test Engineer…..Xen………………..
Date……………..5/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.8	5.54	139.2mA	>200mA	>141.4mA	√
2	40.2	5.55	138.1mA	>200mA	>141.4mA	√
3	40.1	5.54	138.2mA	>200mA	>141.4mA	√
4	40.1	5.56	138.7mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………… QTOP6P ………Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP6P
Driver board ID	QTOP6P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP6P
Monitor board ID	MON176
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON176

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 **Advanced LIGO UK** 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

Drive Card ID……Q_TOP7P………
Monitor Card ID…Mon213..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

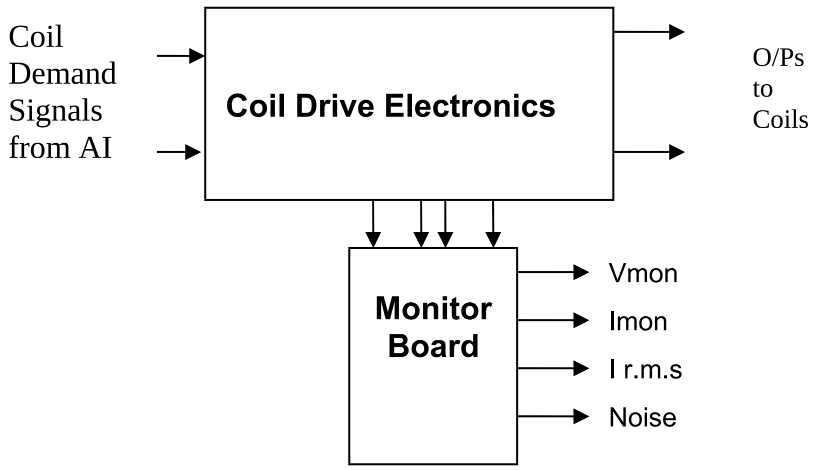


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..2/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Unit……………..Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

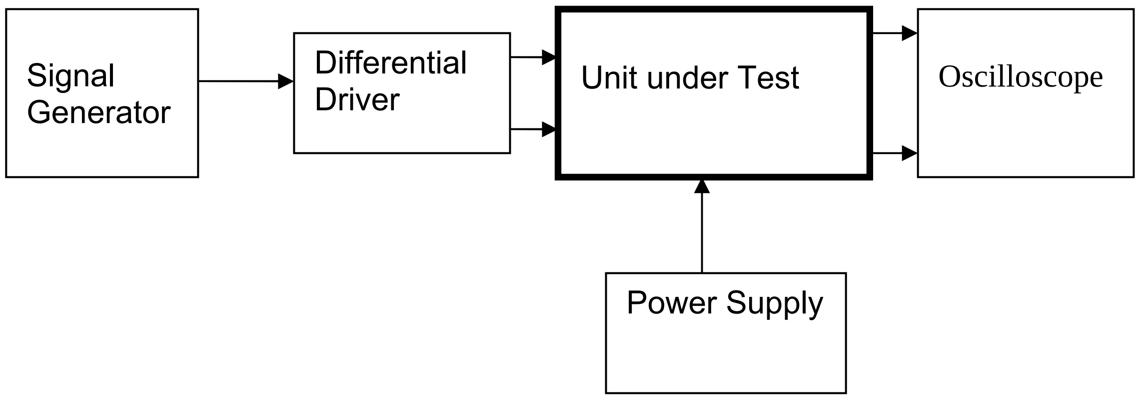
Unit..................Q_TOP_P7........................Serial No ....
Test Engineer.....Xen.....................
Date.................1/7/10..................

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1
Ch2+ = Coil out to Sat pin 3
Ch3+ = Coil out to Sat pin 5
Ch4+ = Coil out to Sat pin 7

Ch1- = Coil out to Sat pin 9
Ch2- = Coil out to Sat pin 11
Ch3- = Coil out to Sat pin 13
Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.015	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.013	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.017	√

Unit………………Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.01	2.9μV√Hz	√
2		1.09	2.9μV√Hz	√
3		1.48	2.9μV√Hz	√
4		1.00	2.9μV√Hz	√

Unit……………..Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.9		
1kHz	-44.9		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit………………Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	**CH1 IC1**	41.8	√
CH1 Negative			**CH1 IC5**	44.3	√
CH2 Positive	24.38	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	41.4	√
CH3 Positive	24.39	√	**CH3 IC1**	45.5	√
CH3 Negative			**CH3 IC5**	42.8	√
CH4 Positive	24.38	√	**CH4 IC1**	42.3	√
CH4 Negative			**CH4 IC5**	44.3	√

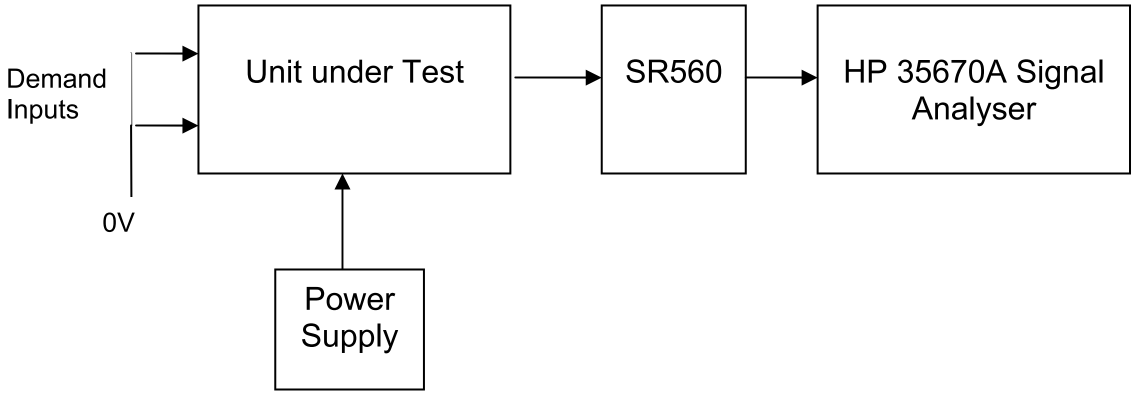
Unit……………….Q_TOP_P7…………………….Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100.2	-160.2
Ch2	-161.15dB	-100.3	-160.3
Ch3	-161.15dB	-99.8	-159.8
Ch4	-161.15dB	-100.3	-160.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P7……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..1/7/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.54	141.0mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.54	140.6mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………..QTOP7P……………..Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP7P
Driver board ID	QTOP7P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP7P
Monitor board ID	MON213
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON213

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen……..…………….
Date……………..1/7/10…..…………….

Drive Card ID……Q_TOP8P………
Monitor Card ID…Mon214..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

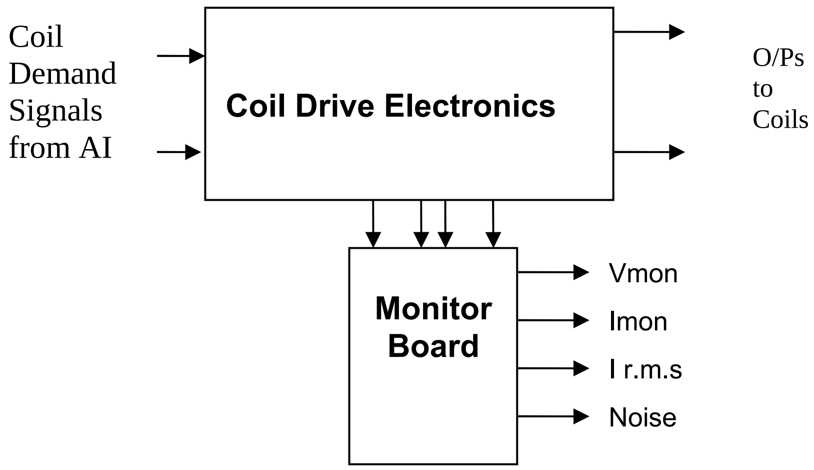


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..1/7/10..………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 2 & 3.

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..30/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

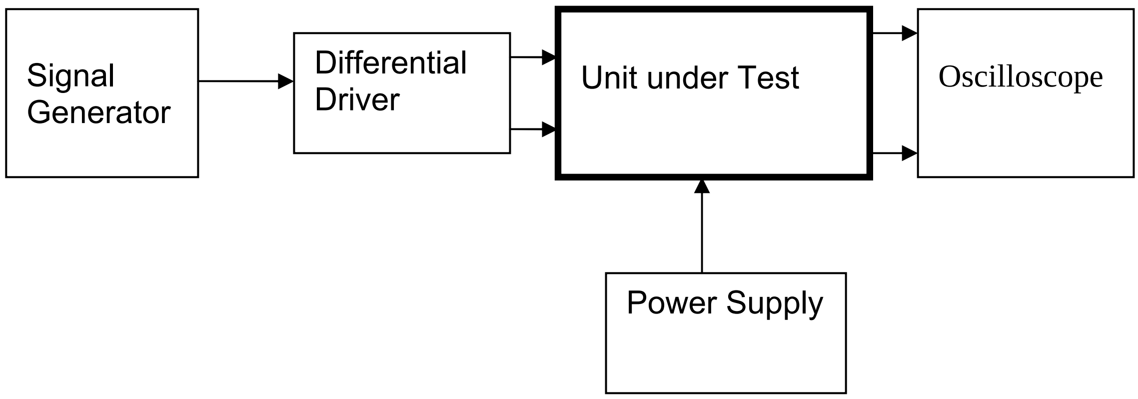
Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..30/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..30/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.012	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.013	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.009	√

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..30/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.19	2.9μV√Hz	√
2		0.95	2.9μV√Hz	√
3		1.84	2.9μV√Hz	√
4		0.97	2.9μV√Hz	√

Unit……………..Q_TOP_P8…………………..Serial No ……………………………
Test Engineer…..Xen…….…………..
Date……………..1/7/10..………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.8		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.83		
Ch2	4.83		
Ch3	4.83		
Ch4	4.83		

Unit………………Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..1/7/10..………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

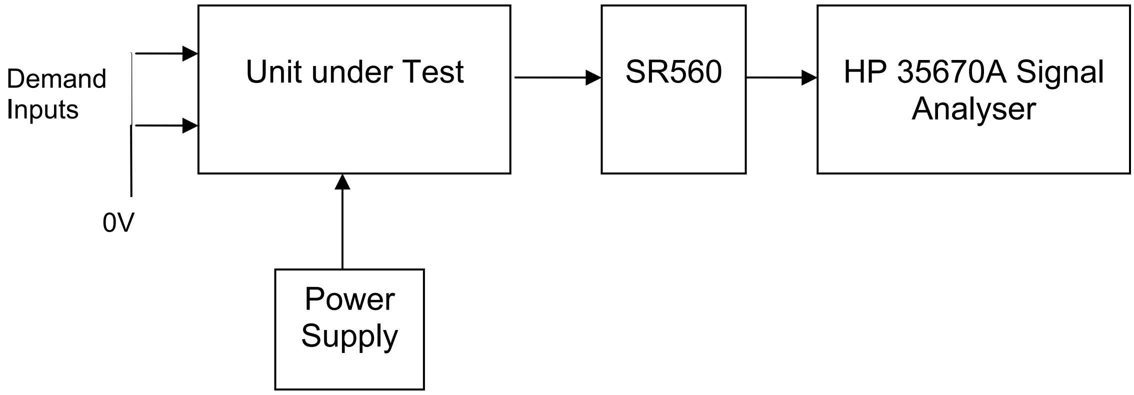
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.55	√	CH1 IC1	44.3	√
CH1 Negative			CH1 IC5	45.7	√
CH2 Positive	24.55	√	CH2 IC1	46.0	√
CH2 Negative			CH2 IC5	44.5	√
CH3 Positive	24.55	√	CH3 IC1	46.5	√
CH3 Negative			CH3 IC5	44.8	√
CH4 Positive	24.55	√	CH4 IC1	44.8	√
CH4 Negative			CH4 IC5	47.4	√

Unit.................Q_TOP_P8.......................Serial No ....
Test Engineer.....Xen.......................
Date................1/7/10...................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100.1	-160.1
Ch2	-161.15dB	-101.3	-161.3
Ch3	-161.15dB	-100.3	-160.3
Ch4	-161.15dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P8……………………Serial No ………………………………
Test Engineer…..Xen…….………………
Date……………..1/7/10..………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………..QTOP8P………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP8P
Driver board ID	QTOP8P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP8P
Monitor board ID	MON214
Monitor board Drawing No/Issue No	D070480_4_k
Monitor board Serial Number	MON214

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….…………..
Date……………..28/6/10……………..

Drive Card ID……Q_TOP9P………
Monitor Card ID…Mon210…………

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

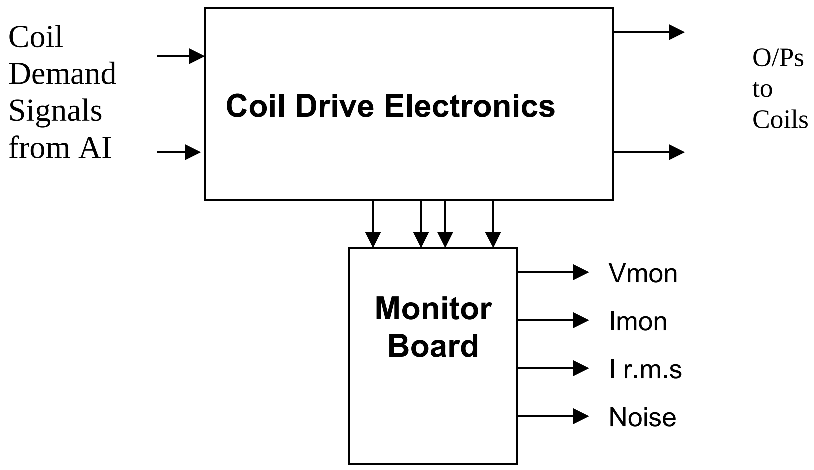


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P9…………………….Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low-pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH4.

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

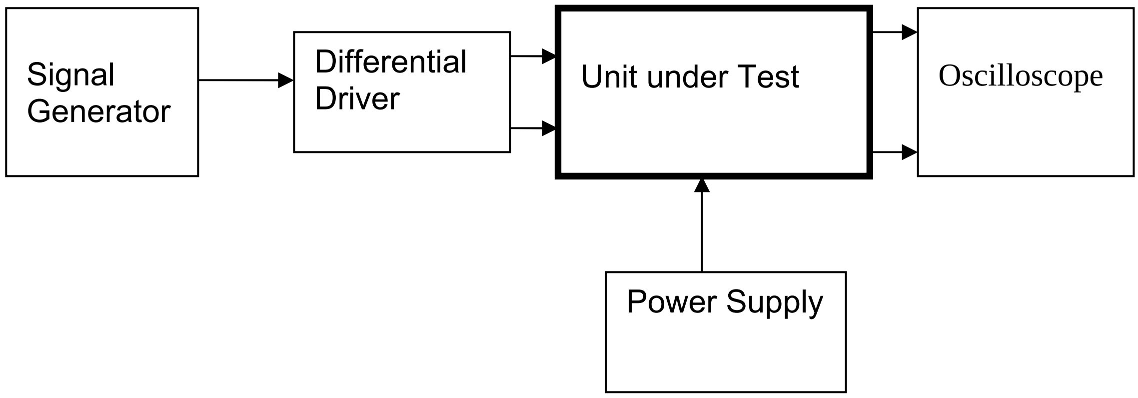
Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.025	√
2	Pin 5	Current Monitor	1v r.m.s	1.016	√
	Pin 4	RMS Current	1v dc	1.013	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.011	√

Unit……………..Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..25/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.02	2.9μV√Hz	√
2		1.10	2.9μV√Hz	√
3		1.20	2.9μV√Hz	√
4		1.39	2.9μV√Hz	√

Unit……………..Q_TOP_P9………………….Serial No …………………………….
Test Engineer…..Xen…….……………
Date……………..28/6/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..28/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.41	√	**CH1 IC1**	44.3	√
CH1 Negative			**CH1 IC5**	45.5	√
CH2 Positive	24.40	√	**CH2 IC1**	47.0	√
CH2 Negative			**CH2 IC5**	47.4	√
CH3 Positive	24.40	√	**CH3 IC1**	47.7	√
CH3 Negative			**CH3 IC5**	47.0	√
CH4 Positive	24.40	√	**CH4 IC1**	46.0	√
CH4 Negative			**CH4 IC5**	47.2	√

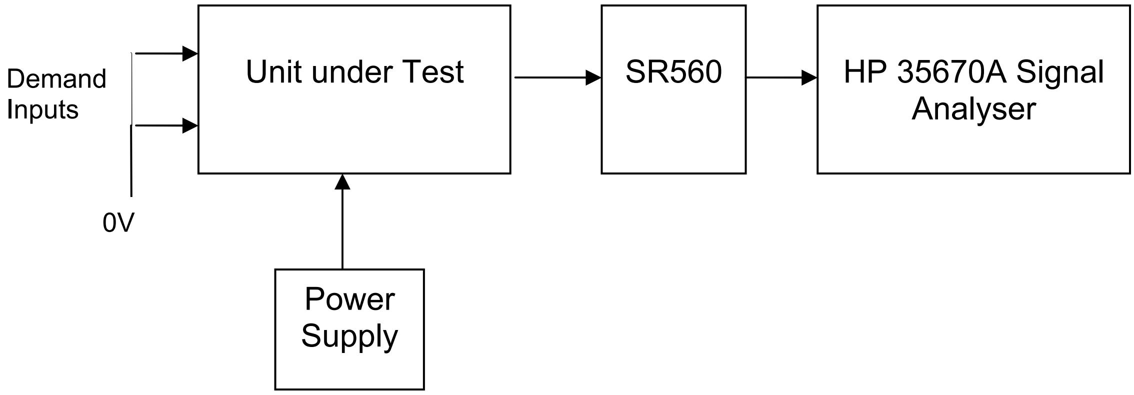
Unit………………Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.6	-159.6
Ch2	-161.15dB	-100.8	-160.8
Ch3	-161.15dB	-99.0	-159.0
Ch4	-161.15dB	-100.3	-160.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………….Q_TOP_P9……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.54	141.0mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.54	140.6mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit………………..QTOP9P………………..Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	**QTOP9P**
Driver board ID	**QTOP9P**
Driver board Drawing No/Issue No	**D0902747_V9**
Driver board Serial Number	**QTOP9P**
Monitor board ID	**MON210**
Monitor board Drawing No/Issue No	**D070480_4_K**
Monitor board Serial Number	**MON210**

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

Drive Card ID……Q_TOP10P………
Monitor Card ID…Mon212…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

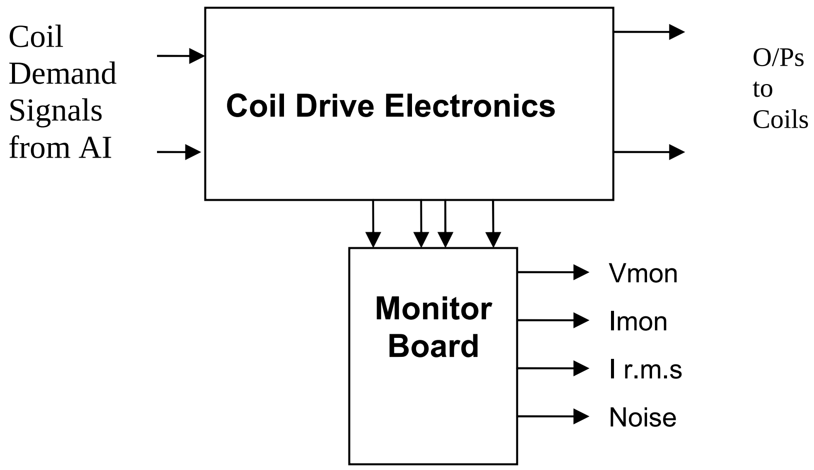


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CH2.

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

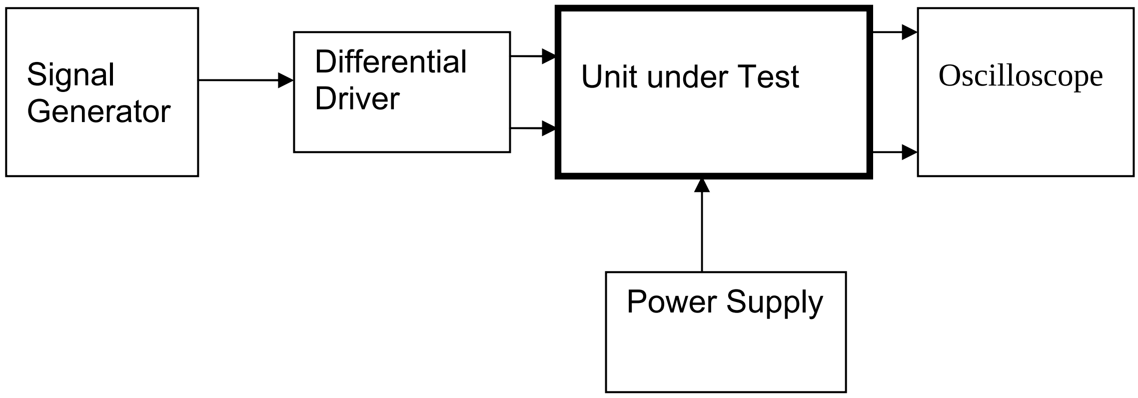
Unit……………….Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..25/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..25/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.019	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.020	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.020	√

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.92	2.9μV√Hz	√
2		2.19	2.9μV√Hz	√
3		1.35	2.9μV√Hz	√
4		1.82	2.9μV√Hz	√

Unit………………Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………….Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..25/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

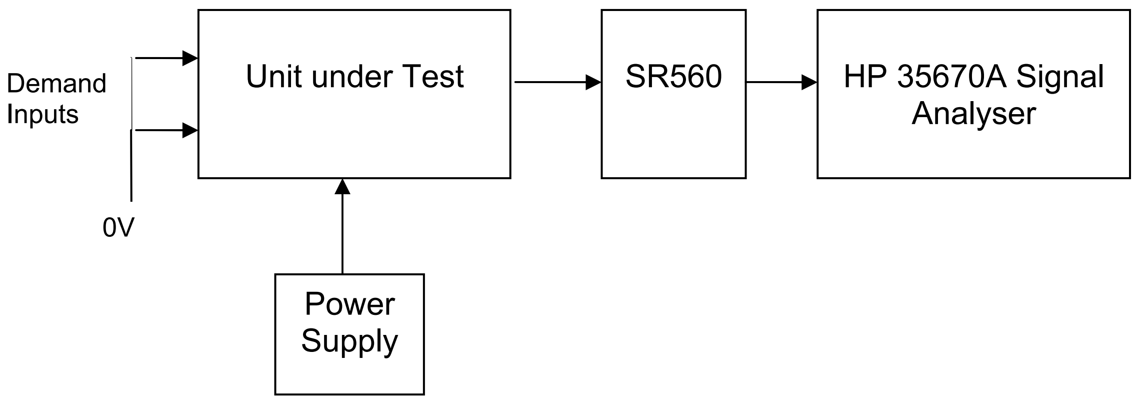
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.51	√	**CH1 IC1**	43.3	√
CH1 Negative			**CH1 IC5**	44.3	√
CH2 Positive	24.51	√	**CH2 IC1**	46.2	√
CH2 Negative			**CH2 IC5**	47.9	√
CH3 Positive	24.52	√	**CH3 IC1**	44.8	√
CH3 Negative			**CH3 IC5**	48.4	√
CH4 Positive	24.51	√	**CH4 IC1**	44.3	√
CH4 Negative			**CH4 IC5**	48.2	√

Unit……………..Q_TOP_P10……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..25/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100.5	-160.5
Ch2	-161.15dB	-98.7	-158.7
Ch3	-161.15dB	-99.9	-159.9
Ch4	-161.15dB	-99.9	-159.9

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P10…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..25/6/10……………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.58	141.6mA	>200mA	>141.4mA	√
3	39.3	5.57	141.7mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP10P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………28/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.

4. Check that all internal connectors are firmly mated.

5. Tighten the screw-locks holding all the external connectors.

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.

8. Check that links W4 and W5 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	**QTOP10P**
Driver board ID	**QTOP10P**
Driver board Drawing No/Issue No	**D0902747_V9**
Driver board Serial Number	**QTOP10P**
Monitor board ID	**MON212**
Monitor board Drawing No/Issue No	**D070480_4_K**
Monitor board Serial Number	**MON212**

10. Check the security of any modification wires.

11. Visually inspect.

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

Drive Card ID……Q_TOP11P………
Monitor Card ID…Mon209…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

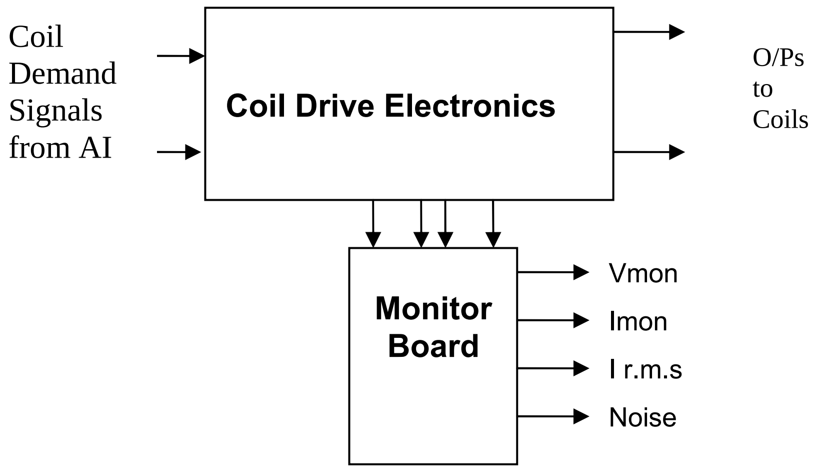


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..28/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1 & 3.

Unit……………….Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

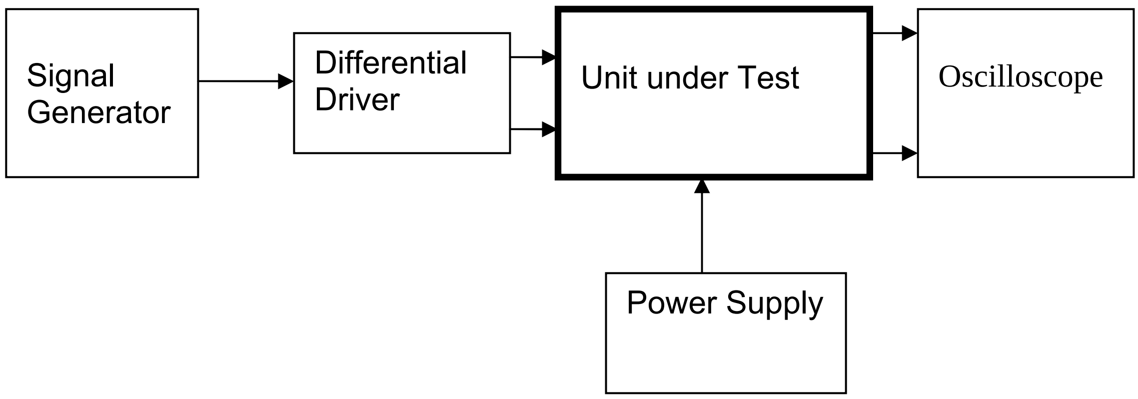
Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..28/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.013	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.012	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..28/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.28	2.9μV√Hz	√
2		1.00	2.9μV√Hz	√
3		1.06	2.9μV√Hz	√
4		1.46	2.9μV√Hz	√

Unit…………….…Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.8		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.9		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..29/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

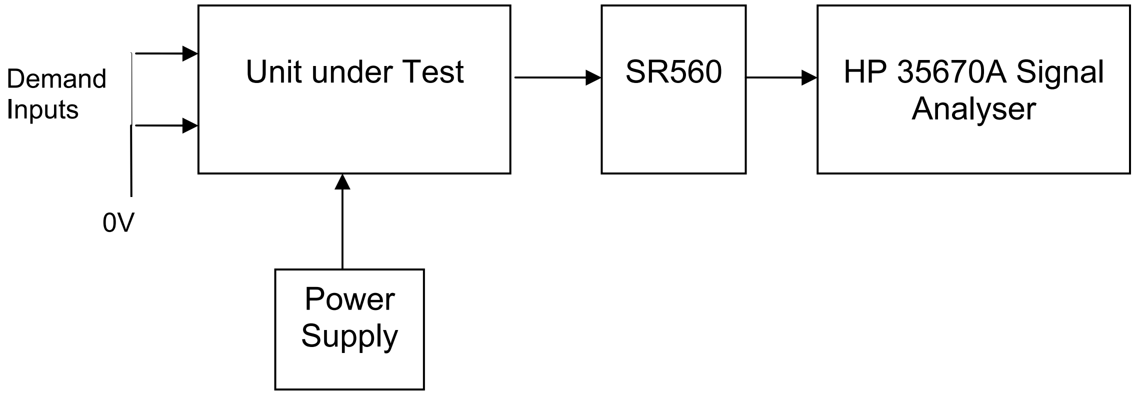
The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.43	√	**CH1 IC1**	43.8	√
CH1 Negative			**CH1 IC5**	44.8	√
CH2 Positive	24.43	√	**CH2 IC1**	44.8	√
CH2 Negative			**CH2 IC5**	48.7	√
CH3 Positive	24.44	√	**CH3 IC1**	46.7	√
CH3 Negative			**CH3 IC5**	48.9	√
CH4 Positive	24.44	√	**CH4 IC1**	44.0	√
CH4 Negative			**CH4 IC5**	45.7	√

Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.0	-161.0
Ch2	-161.15dB	-99.7	-159.7
Ch3	-161.15dB	-102.1	-162.1
Ch4	-161.15dB	-101.3	-161.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit………………Q_TOP_P11……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..29/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box.

2. Unplug all external connections.

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.

4. Check that all internal connectors are firmly mated.

5. Tighten the screw-locks holding all the external connectors.

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.

8. Check that links W4 and W5 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	
Driver board ID	
Driver board Drawing No/Issue No	
Driver board Serial Number	
Monitor board ID	
Monitor board Drawing No/Issue No	
Monitor board Serial Number	

10. Check the security of any modification wires.

11. Visually inspect.

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

Drive Card ID……Q_TOP12P………
Monitor Card ID…Mon88…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

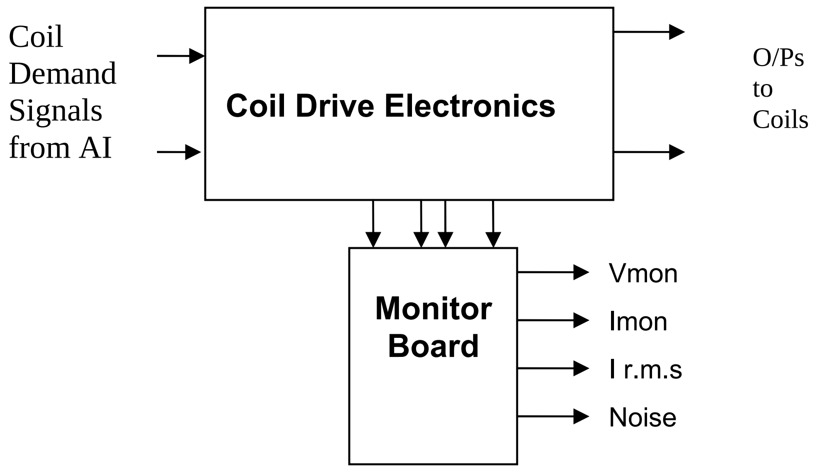


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

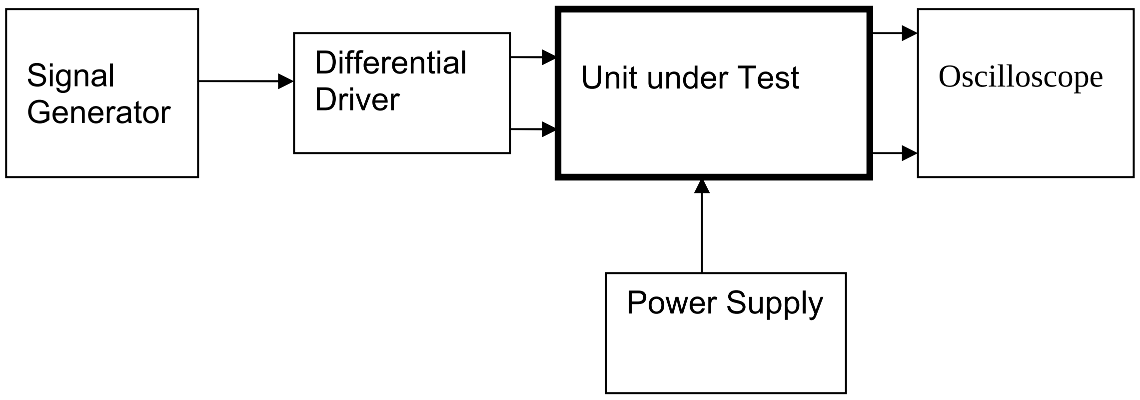
Unit………………Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.017	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.015	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.020	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.022	√

Unit………………Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.27	2.9μV√Hz	√
2		1.60	2.9μV√Hz	√
3		1.77	2.9μV√Hz	√
4		1.30	2.9μV√Hz	√

Unit……………..Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.9		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P12……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.40	√	**CH1 IC1**	42.3	√
CH1 Negative			**CH1 IC5**	45.3	√
CH2 Positive	24.41	√	**CH2 IC1**	46.2	√
CH2 Negative			**CH2 IC5**	46.7	√
CH3 Positive	24.40	√	**CH3 IC1**	45.5	√
CH3 Negative			**CH3 IC5**	47.0	√
CH4 Positive	24.40	√	**CH4 IC1**	45.7	√
CH4 Negative			**CH4 IC5**	44.8	√

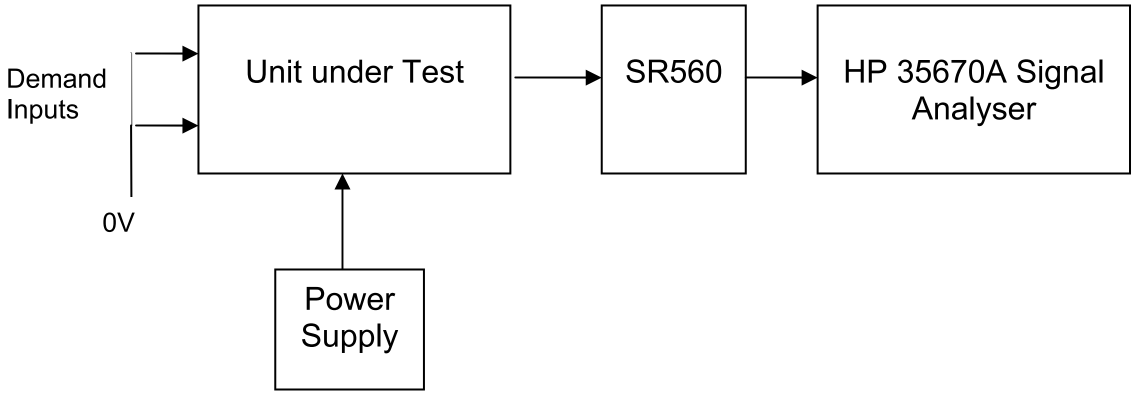
Unit……………..Q_TOP_P12…………………..Serial No ………………………………
Test Engineer…..Xen………………..
Date……………..8/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100.9	-160.9
Ch2	-161.15dB	-101.6	-161.6
Ch3	-161.15dB	-101.2	-161.2
Ch4	-161.15dB	-100.0	-160.0

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3			>200mA	>141.4mA	
2	39.4			>200mA	>141.4mA	
3	39.3			>200mA	>141.4mA	
4	39.4			>200mA	>141.4mA	

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP12P…………Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP12P
Driver board ID	DO902747_V9
Driver board Drawing No/Issue No	QTOP12P
Driver board Serial Number	QTOP12P
Monitor board ID	MON88
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON88

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…..………………
Date……………..10/5/10……………..

Drive Card ID……Q_TOP13P………
Monitor Card ID…Mon121…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

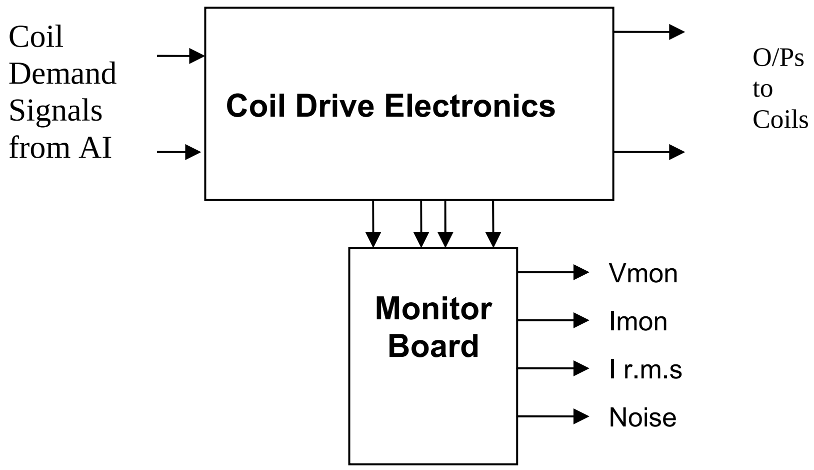


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P13…………………….Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH2.

Unit……………..Q_TOP_P13…………………..Serial No ……………………………
Test Engineer…..Xen……………….
Date……………..6/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

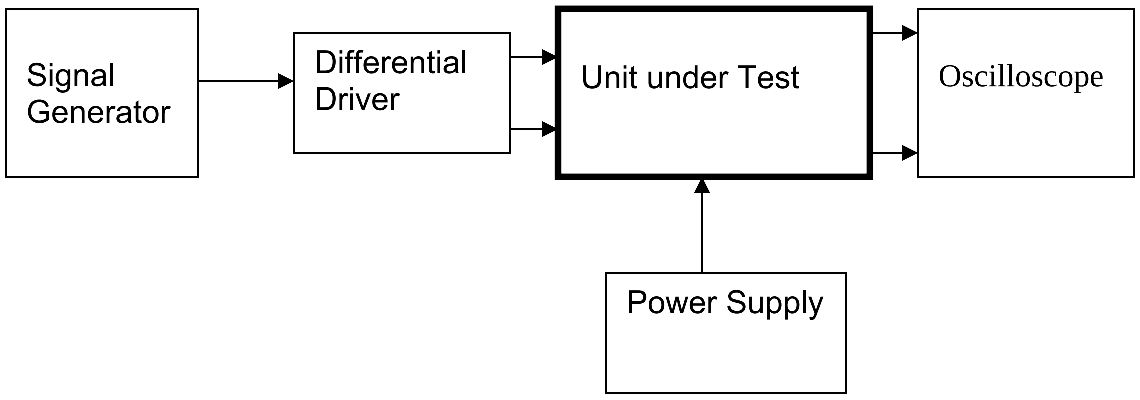
Unit………………Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P13……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.021	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.014	√

Unit……………..Q_TOP_P13…………………..Serial No …………………………….
Test Engineer…..Xen……………….
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.43	2.9μV√Hz	√
2		1.40	2.9μV√Hz	√
3		1.05	2.9μV√Hz	√
4		1.09	2.9μV√Hz	√

Unit……………..Q_TOP_P13…………………..Serial No ……………………………
Test Engineer…..Xen…..……………..
Date……………..10/5/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.9		
Ch2	4.9		
Ch3	4.9		
Ch4	4.9		

Unit…………………Q_TOP_P13………………………Serial No ……………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	CH1 IC1	42.6	√
CH1 Negative			CH1 IC5	42.6	√
CH2 Positive	24.36	√	CH2 IC1	44.3	√
CH2 Negative			CH2 IC5	45.5	√
CH3 Positive	24.36	√	CH3 IC1	44.8	√
CH3 Negative			CH3 IC5	45.3	√
CH4 Positive	24.36	√	CH4 IC1	43.3	√
CH4 Negative			CH4 IC5	44.5	√

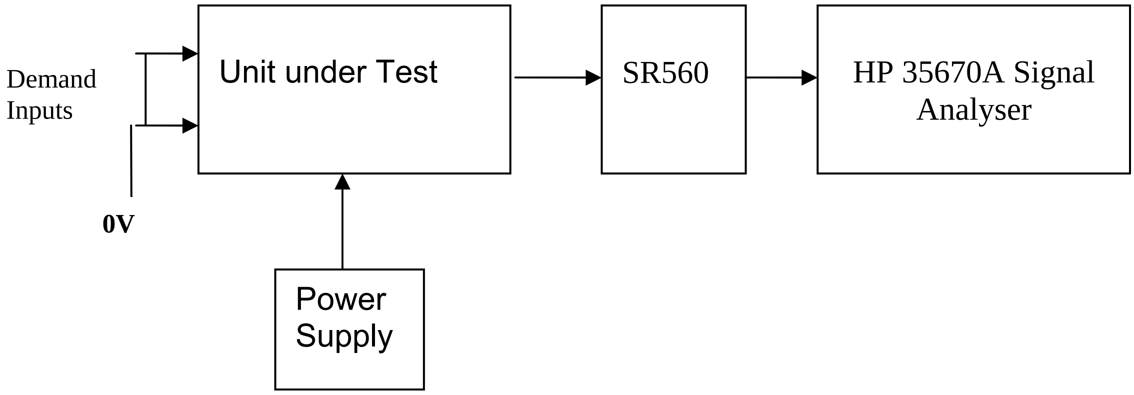
Unit……………..Q_TOP_P13…………………..Serial No ……………………………..
Test Engineer…..Xen…….…………….
Date……………..11/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.0	-159.0
Ch2	-161.15dB	-99.2	-159.2
Ch3	-161.15dB	-100.8	-160.8
Ch4	-161.15dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………….Q_TOP_P13…………………….Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP13P………..Serial No ………………………………
Test Engineer ………RMC
Date ………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP13P
Driver board ID	QTOP13P
Driver board Drawing No/Issue No	D0902747_v9
Driver board Serial Number	QTOP13P
Monitor board ID	MON121
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON121

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

Drive Card ID……Q_TOP14P………
Monitor Card ID…Mon120…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

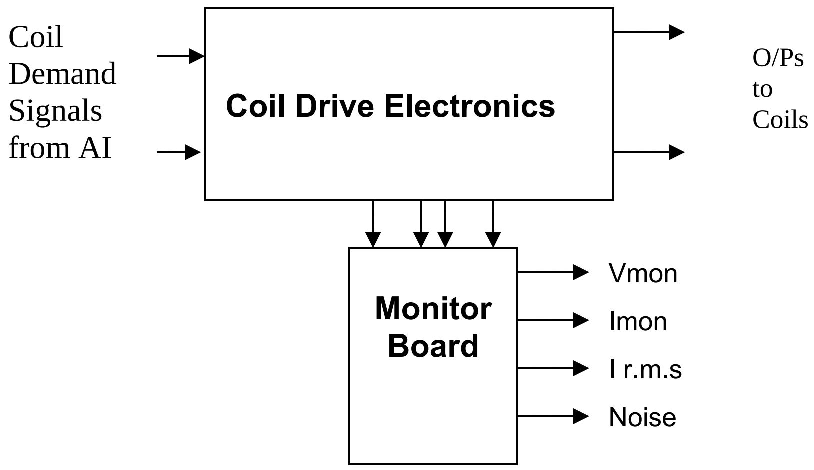


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………...Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH3.

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

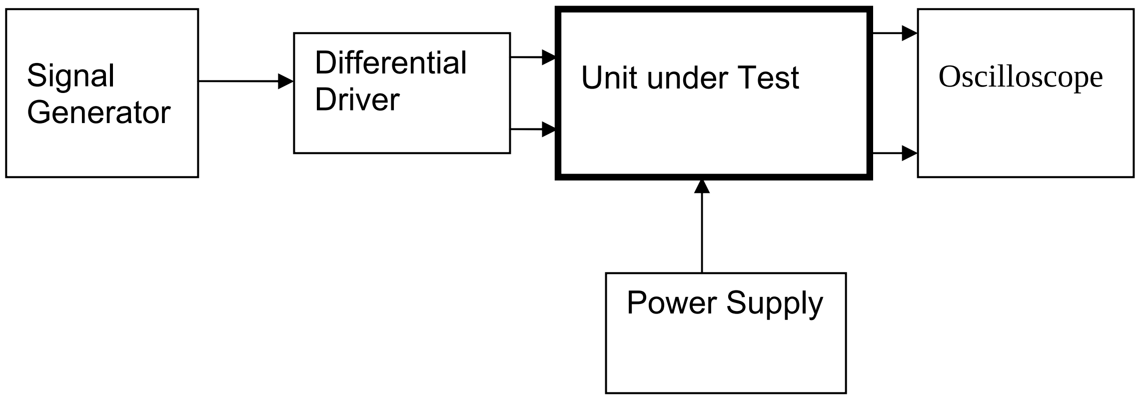
Unit……………….Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.020	√
3	Pin 8	Current Monitor	1v r.m.s	1.016	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.19	2.9μV√Hz	√
2		1.43	2.9μV√Hz	√
3		1.41	2.9μV√Hz	√
4		1.06	2.9μV√Hz	√

Unit……………...Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.9		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

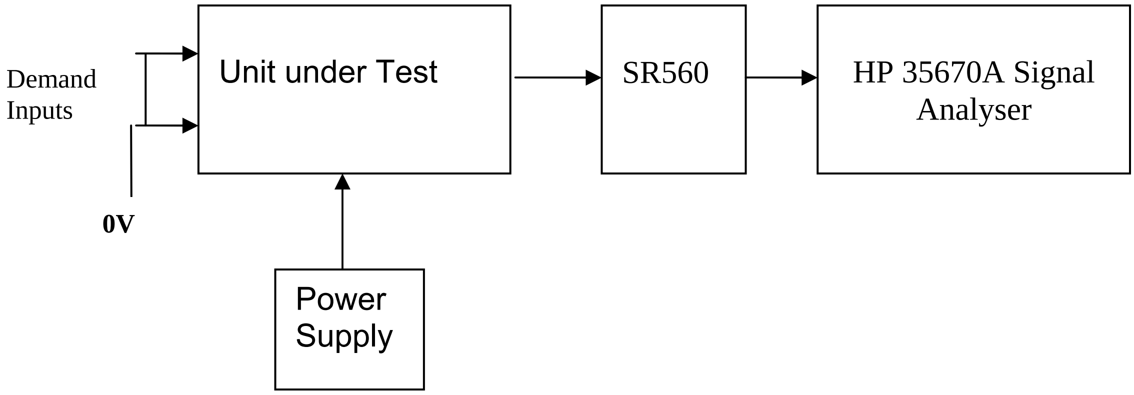
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	42.6	√
CH1 Negative			CH1 IC5	44.5	√
CH2 Positive	24.39	√	CH2 IC1	42.8	√
CH2 Negative			CH2 IC5	43.6	√
CH3 Positive	24.39	√	CH3 IC1	45.0	√
CH3 Negative			CH3 IC5	43.1	√
CH4 Positive	24.39	√	CH4 IC1	42.6	√
CH4 Negative			CH4 IC5	47.0	√

Unit……………..Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..9/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-102.8	-162.8
Ch2	-161.15dB	-102.0	-162.0
Ch3	-161.15dB	-100.5	-160.5
Ch4	-161.15dB	-101.0	-161.0

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P14……………………Serial No ………………………………
Test Engineer…..Xen…..…………….
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP14P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP14P
Driver board ID	QTOP14P
Driver board Drawing No/Issue No	D090747_V9
Driver board Serial Number	QTOP14P
Monitor board ID	MON120
Monitor board Drawing No/Issue No	D070480_k
Monitor board Serial Number	MON120

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

Drive Card ID……Q_TOP15P………
Monitor Card ID…Mon125…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

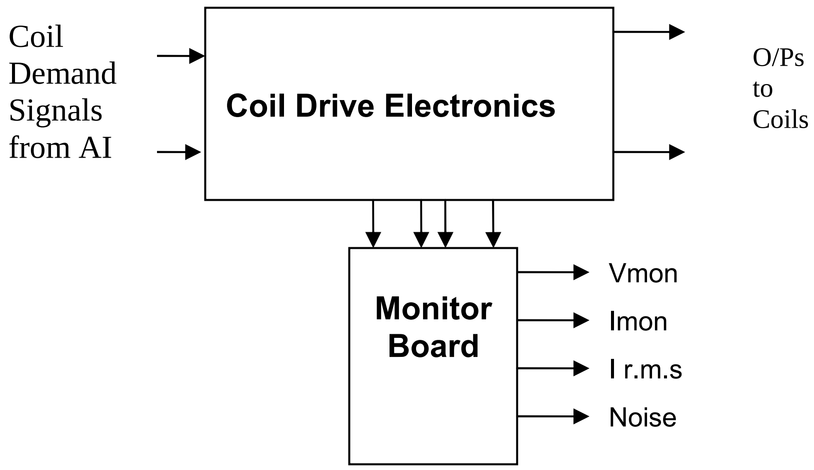


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P15…………………….Serial No ……………………………….
Test Engineer…..Xen…..…………….
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CHs 2 & 3.

Unit……………….Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..…………….
Date……………..6/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

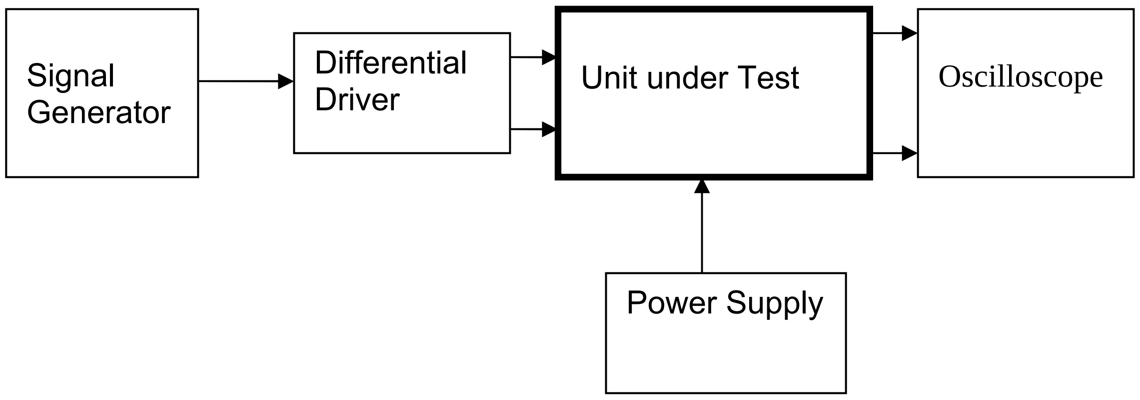
Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit…………………Q_TOP_P15……………………….Serial No …………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.025	√
2	Pin 5	Current Monitor	1v r.m.s	1.017	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.017	√
	Pin 7	RMS Current	1v dc	1.025	√
4	Pin 11	Current Monitor	1v r.m.s	1.015	√
	Pin 10	RMS Current	1v dc	1.020	√

Unit……………….Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.25	2.9μV√Hz	√
2		1.55	2.9μV√Hz	√
3		1.75	2.9μV√Hz	√
4		1.02	2.9μV√Hz	√

Unit.................Q_TOP_P15......................Serial No ....
Test Engineer.....Xen........................
Date.................10/5/10.................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.8		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	CH1 IC1	44.0	√
CH1 Negative			CH1 IC5	47.0	√
CH2 Positive	24.40	√	CH2 IC1	46.2	√
CH2 Negative			CH2 IC5	46.7	√
CH3 Positive	24.40	√	CH3 IC1	46.2	√
CH3 Negative			CH3 IC5	45.0	√
CH4 Positive	24.40	√	CH4 IC1	43.3	√
CH4 Negative			CH4 IC5	44.8	√

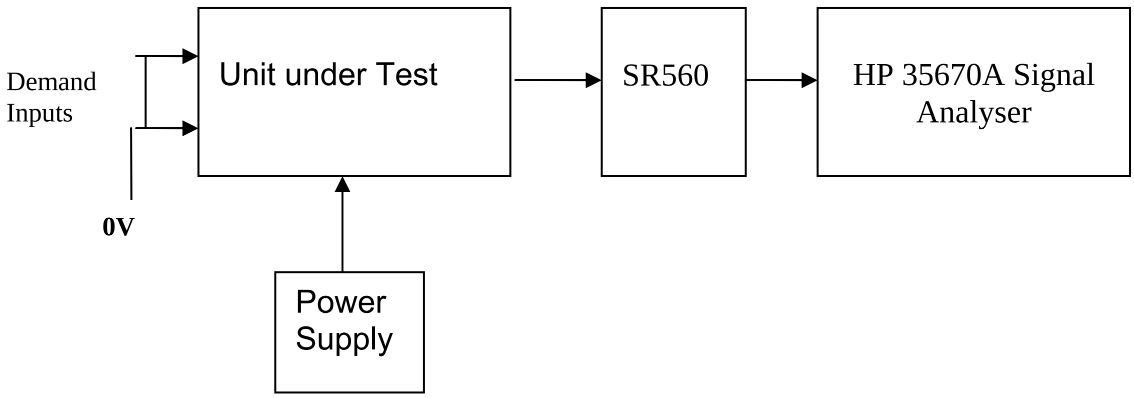
Unit……………..Q_TOP_P15………………….Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..14/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.8	-159.8
Ch2	-161.15dB	-99.9	-159.9
Ch3	-161.15dB	-101.5	-161.5
Ch4	-161.15dB	-101.2	-161.2

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P15……………………Serial No ………………………………
Test Engineer…..Xen…..…………….
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP15P………..Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP15P
Driver board ID	QTOP15P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP15P
Monitor board ID	MON125
Monitor board Drawing No/Issue No	D070480K_4_K
Monitor board Serial Number	MON125

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws,

Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..10/5/10……………..

Drive Card ID……Q_TOP16P………
Monitor Card ID…Mon124…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

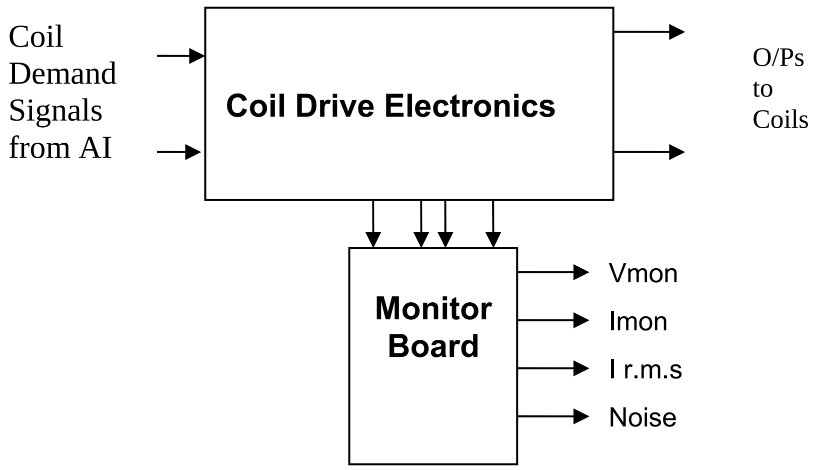


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………..
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P16…………………….Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH2.

Unit……………..Q_TOP_P16…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

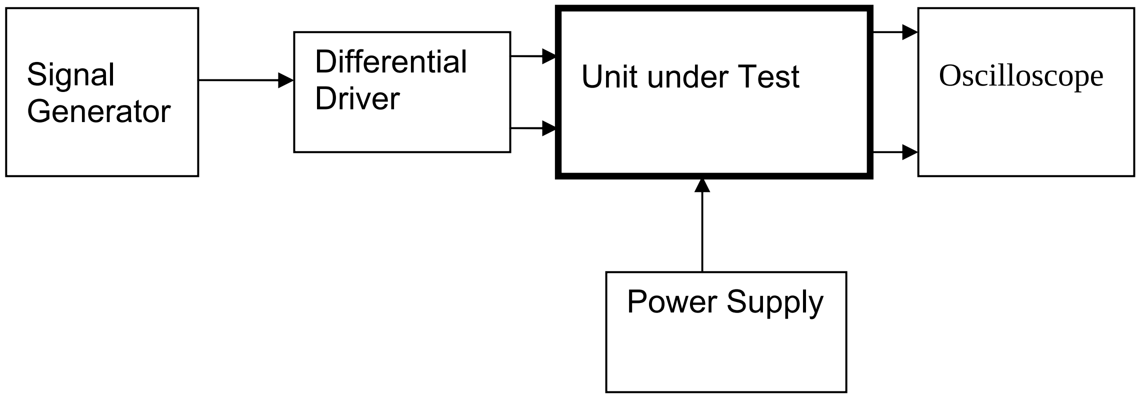
Unit……………..Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.023	√
2	Pin 5	Current Monitor	1v r.m.s	1.016	√
	Pin 4	RMS Current	1v dc	1.014	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.019	√
4	Pin 11	Current Monitor	1v r.m.s	1.015	√
	Pin 10	RMS Current	1v dc	1.018	√

Unit………………Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.30	2.9μV√Hz	√
2		0.99	2.9μV√Hz	√
3		1.17	2.9μV√Hz	√
4		1.18	2.9μV√Hz	√

Unit……………..Q_TOP_P16……………………Serial No ……………………………..
Test Engineer…..Xen…………………
Date……………..10/5/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

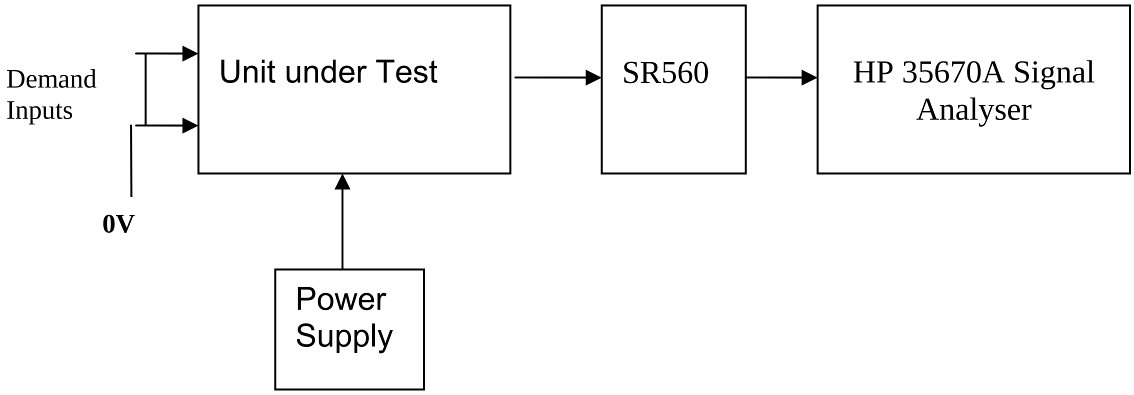
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	**CH1 IC1**	43.1	√
CH1 Negative			**CH1 IC5**	44.8	√
CH2 Positive	24.37	√	**CH2 IC1**	44.5	√
CH2 Negative			**CH2 IC5**	44.3	√
CH3 Positive	24.38	√	**CH3 IC1**	42.8	√
CH3 Negative			**CH3 IC5**	45.3	√
CH4 Positive	24.37	√	**CH4 IC1**	42.3	√
CH4 Negative			**CH4 IC5**	42.1	√

Unit……………..Q_TOP_P16…………………..Serial No ……………………………
Test Engineer…..Xen………………….
Date……………..11/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.0	-159.0
Ch2	-161.15dB	-100.1	-160.1
Ch3	-161.15dB	-99.2	-159.2
Ch4	-161.15dB	-101.1	-161.1

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P16……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit............QTOP16P.....................Serial No ....
Test Engineer ....RMC
Date 7/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP16P
Driver board ID	QTOP16P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP16P
Monitor board ID	MON24
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON24

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..10/5/10………………

Drive Card ID……Q_TOP17P………
Monitor Card ID…Mon122…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

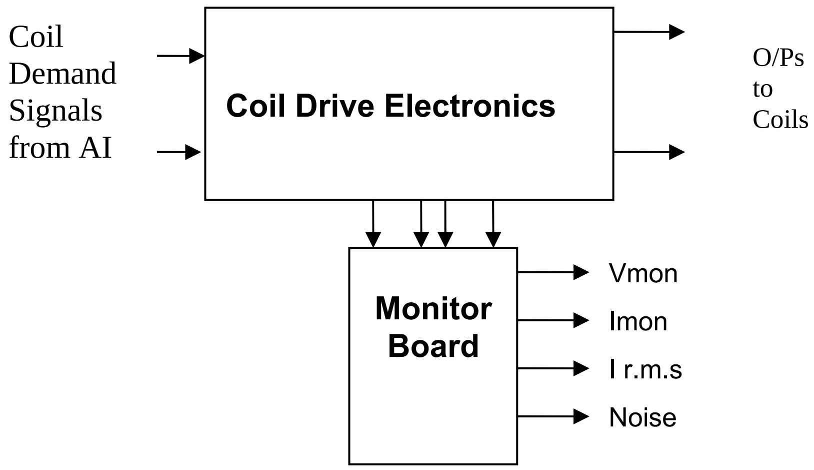


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P17…………………….Serial No ……………………………….
Test Engineer…..Xen………………….
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH2.

Unit..................Q_TOP_P17........................Serial No ....
Test Engineer.....Xen.....................
Date.................6/5/10..................

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

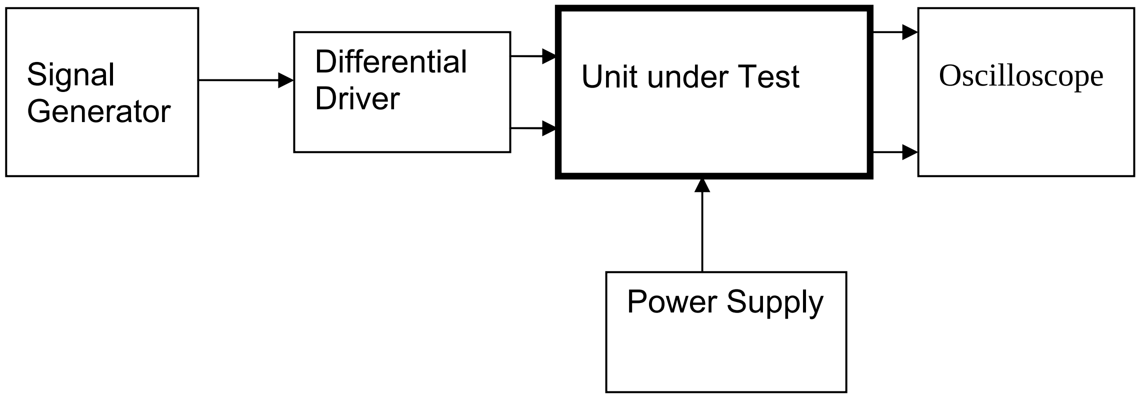
Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit…………………Q_TOP_P17………………………Serial No ……………………………………
Test Engineer…..Xen…………………….
Date……………..6/5/10…………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….Q_TOP_P17…………………….Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.017	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.019	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.020	√

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.06	2.9μV√Hz	√
2		0.88	2.9μV√Hz	√
3		1.51	2.9μV√Hz	√
4		1.32	2.9μV√Hz	√

Unit……………..Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..10/5/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

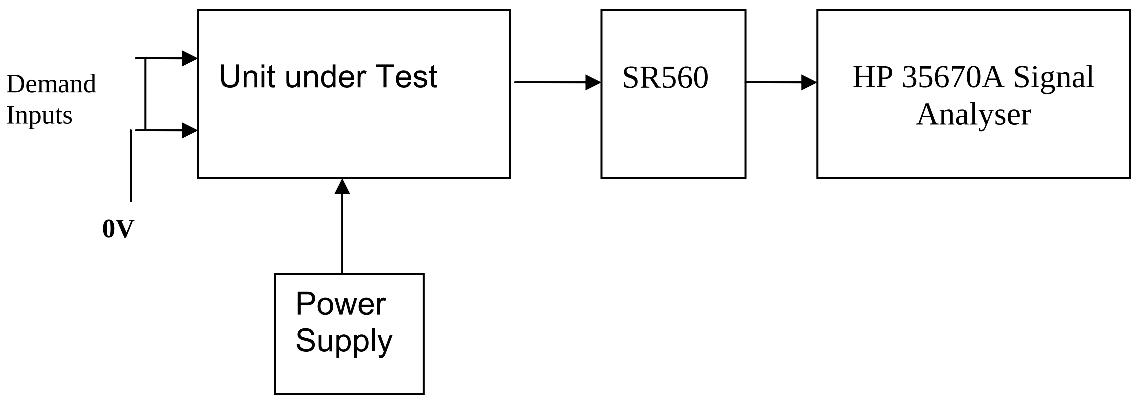
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.37	√	**CH1 IC1**	42.1	√
CH1 Negative			**CH1 IC5**	45.0	√
CH2 Positive	24.37	√	**CH2 IC1**	45.3	√
CH2 Negative			**CH2 IC5**	45.0	√
CH3 Positive	24.37	√	**CH3 IC1**	43.8	√
CH3 Negative			**CH3 IC5**	42.8	√
CH4 Positive	24.37	√	**CH4 IC1**	44.5	√
CH4 Negative			**CH4 IC5**	45.5	√

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..11/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.8	-159.8
Ch2	-161.15dB	-103.1	-163.1
Ch3	-161.15dB	-101.1	-161.1
Ch4	-161.15dB	-100.6	-160.6

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P17……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.57	141.7mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP17P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP17P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP17P
Driver board Serial Number	QTOP17P
Monitor board ID	MON122
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON122

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

Drive Card ID……Q_TOP18P………
Monitor Card ID…Mon123…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

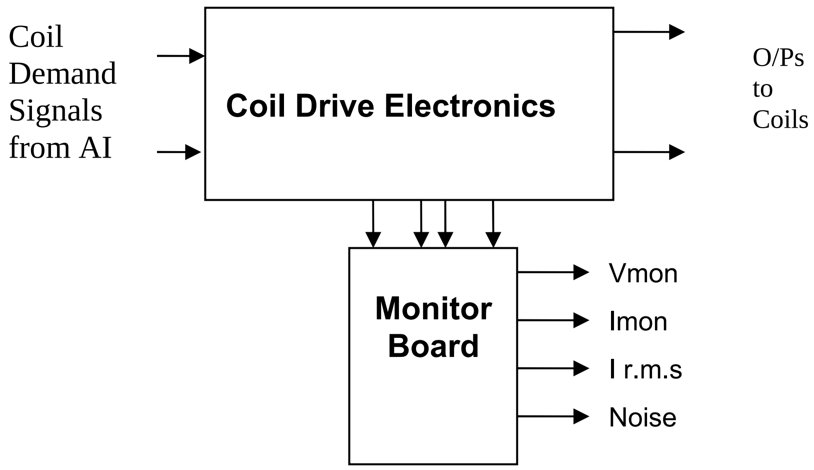


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..10/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CH1.

Unit……………….Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

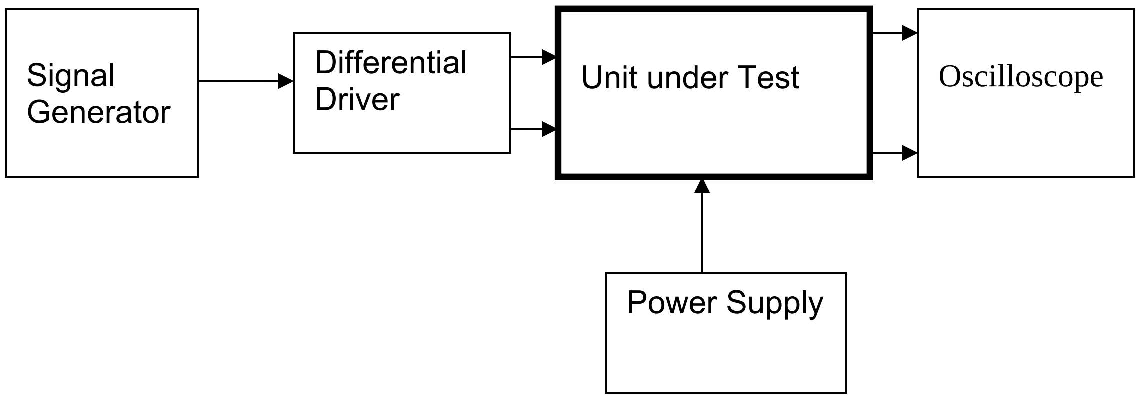
Unit……………….Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..…………….
Date……………..6/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.018	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.016	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.013	√

Unit………………Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..……………
Date……………..6/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.09	2.9μV√Hz	√
2		1.46	2.9μV√Hz	√
3		1.60	2.9μV√Hz	√
4		1.82	2.9μV√Hz	√

Unit………………Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..10/5/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.6		
10Hz	-29.7		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.6		
10Hz	-29.8		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P18……………………Serial No ………………………………
Test Engineer…..Xen…..…………..
Date……………..6/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	**CH1 IC1**	40.6	√
CH1 Negative			**CH1 IC5**	40.9	√
CH2 Positive	24.38	√	**CH2 IC1**	44.5	√
CH2 Negative			**CH2 IC5**	42.3	√
CH3 Positive	24.38	√	**CH3 IC1**	44.8	√
CH3 Negative			**CH3 IC5**	44.0	√
CH4 Positive	24.38	√	**CH4 IC1**	43.8	√
CH4 Negative			**CH4 IC5**	45.0	√

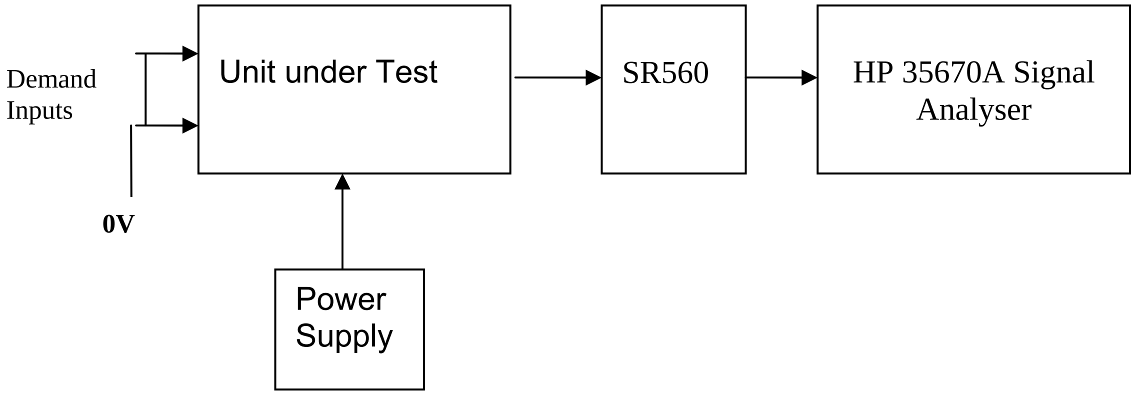
Unit……………..Q_TOP_P18…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..11/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.8	-161.8
Ch2	-161.15dB	-99.6	-159.6
Ch3	-161.15dB	-100.5	-160.5
Ch4	-161.15dB	-100.6	-160.6

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P18…………………..Serial No ……………………………
Test Engineer…..Xen…..…………..
Date……………..6/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP18P………..Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP18P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP18P
Driver board Serial Number	QTOP18P
Monitor board ID	MON123
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON123

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

Drive Card ID……Q_TOP19P………
Monitor Card ID…Mon97…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

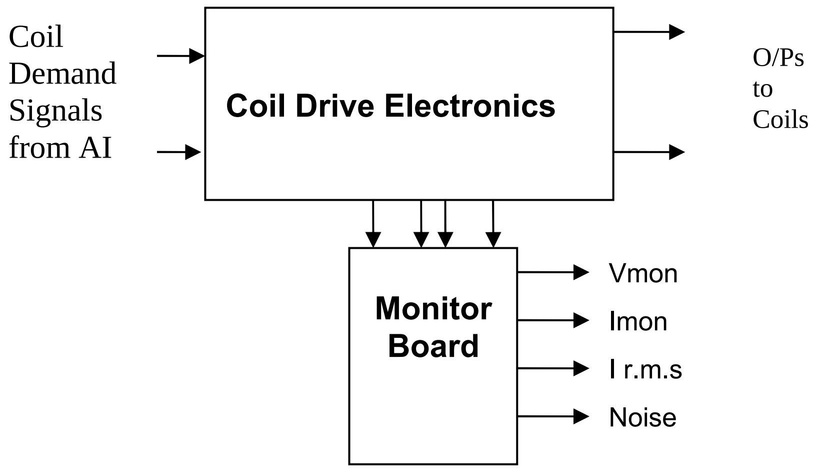


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P19……………………Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..4/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………….Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

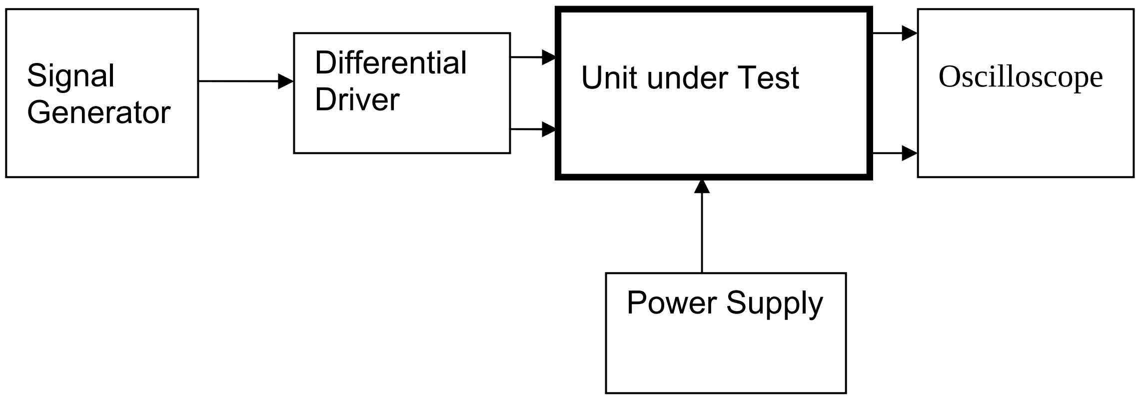
Unit……………….Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.011	√
	Pin 1	RMS Current	1v dc	1.010	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.007	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit………………Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9μV√Hz	√
2		1.27	2.9μV√Hz	√
3		1.0	2.9μV√Hz	√
4		1.31	2.9μV√Hz	√

Unit……………..Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	**CH1 IC1**	43.3	√
CH1 Negative			**CH1 IC5**	46.5	√
CH2 Positive	24.39	√	**CH2 IC1**	45.7	√
CH2 Negative			**CH2 IC5**	47.9	√
CH3 Positive	24.40	√	**CH3 IC1**	44.5	√
CH3 Negative			**CH3 IC5**	47.4	√
CH4 Positive	24.40	√	**CH4 IC1**	44.5	√
CH4 Negative			**CH4 IC5**	45.7	√

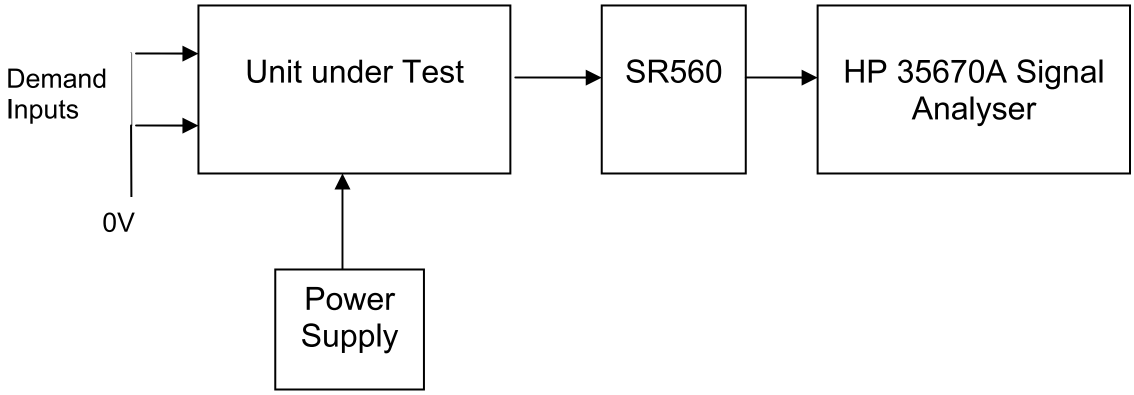
Unit……………..Q_TOP_P19…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..8/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-98.6	-158.6
Ch2	-161.15dB	-101.6	-161.6
Ch3	-161.15dB	-100.7	-160.7
Ch4	-161.15dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P19……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.58	141.6mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP19P……………Serial No ………………………………
Test Engineer ………RMC
Date …………………7/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP19P
Driver board ID	QTOP19P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP19P
Monitor board ID	MON97
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON97

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

Drive Card ID……Q_TOP20P………
Monitor Card ID…Mon87…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

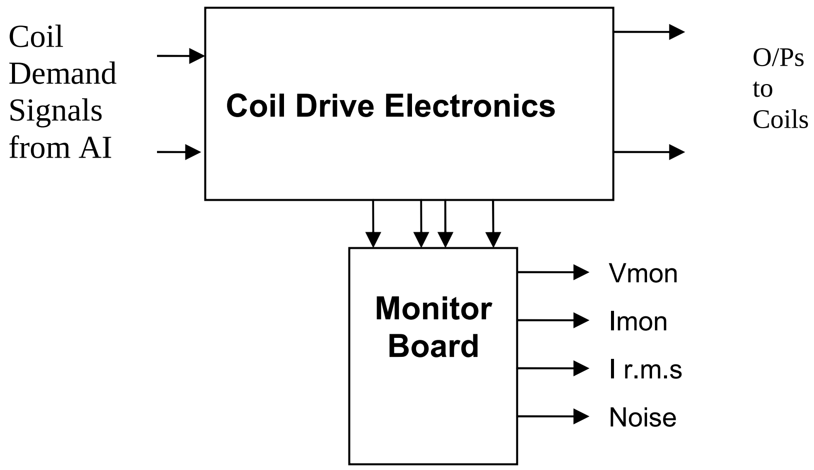


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P20…………………….Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..4/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

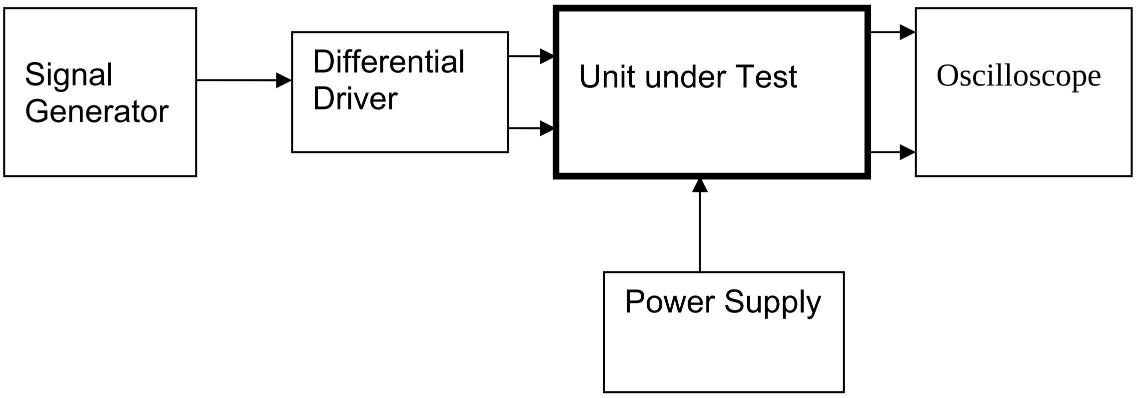
Unit……………….Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.015	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.014	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.011	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit……………..Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.15	2.9μV√Hz	√
2		1.15	2.9μV√Hz	√
3		1.49	2.9μV√Hz	√
4		0.99	2.9μV√Hz	√

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..4/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	42.8	√
CH1 Negative			CH1 IC5	46.0	√
CH2 Positive	24.39	√	CH2 IC1	45.5	√
CH2 Negative			CH2 IC5	44.8	√
CH3 Positive	24.39	√	CH3 IC1	45.3	√
CH3 Negative			CH3 IC5	48.7	√
CH4 Positive	24.39	√	CH4 IC1	46.0	√
CH4 Negative			CH4 IC5	48.9	√

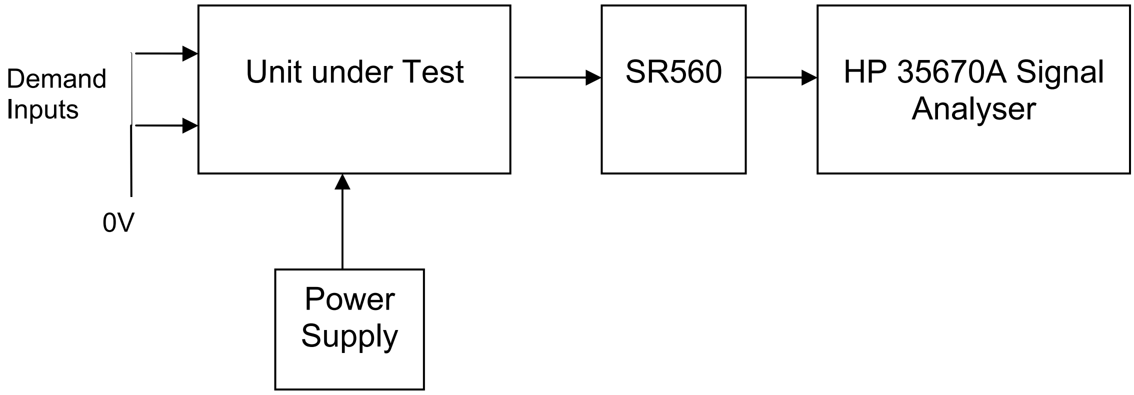
Unit…………………Q_TOP_P20……………………….Serial No …………………………………
Test Engineer…..Xen…………………
Date……………..8/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-98.9	-158.9
Ch2	-161.15dB	-100.9	-160.9
Ch3	-161.15dB	-101.5	-161.5
Ch4	-161.15dB	-100.6	-160.6

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P20……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.58	141.6mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………… QTOP20P …………Serial No ………………………………
Test Engineer ………RMC
Date …………………6/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP20P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP20P
Driver board Serial Number	QTOP20P
Monitor board ID	MON87
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON87

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..21/5/10………………

Drive Card ID……Q_TOP21P………
Monitor Card ID…Mon96…...………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

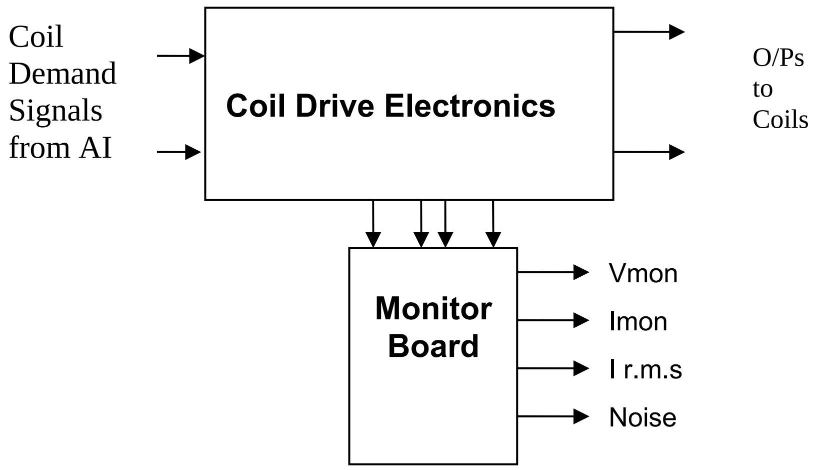


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..21/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

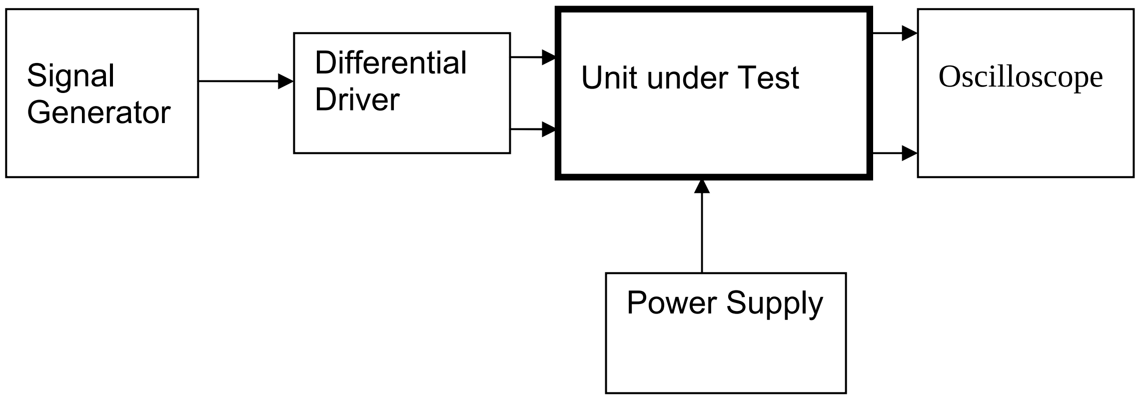
Unit……………….Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..21/5/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..21/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………...Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.011	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.016	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.014	√
4	Pin 11	Current Monitor	1v r.m.s	1.011	√
	Pin 10	RMS Current	1v dc	1.014	√

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..9/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.19	2.9μV√Hz	√
2		1.01	2.9μV√Hz	√
3		1.90	2.9μV√Hz	√
4		1.33	2.9μV√Hz	√

Unit..................Q_TOP_P21........................Serial No ....
Test Engineer.....Xen......................
Date.................21/5/10..................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..21/5/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

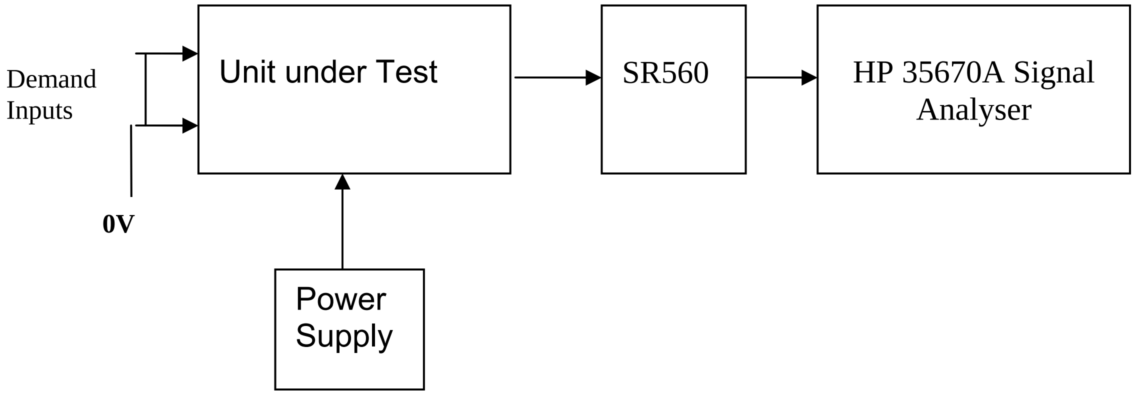
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.37	√	**CH1 IC1**	42.1	√
CH1 Negative			**CH1 IC5**	39.2	√
CH2 Positive	24.37	√	**CH2 IC1**	46.7	√
CH2 Negative			**CH2 IC5**	46.0	√
CH3 Positive	24.37	√	**CH3 IC1**	46.0	√
CH3 Negative			**CH3 IC5**	45.5	√
CH4 Positive	24.37	√	**CH4 IC1**	46.5	√
CH4 Negative			**CH4 IC5**	46.5	√

Unit……………..Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..9/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100.1	-160.1
Ch2	-161.15dB	-99.8	-159.8
Ch3	-161.15dB	-99.9	-159.9
Ch4	-161.15dB	-101.2	-161.2

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P21……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..21/5/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………… QTOP21P …………Serial No ………………………………
Test Engineer ………RMC
Date …………………6/7/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP21P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP21P
Driver board Serial Number	QTOP21P
Monitor board ID	MON96
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON96

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..26/5/10……………..

Drive Card ID……Q_TOP22P………
Monitor Card ID…Mon95…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

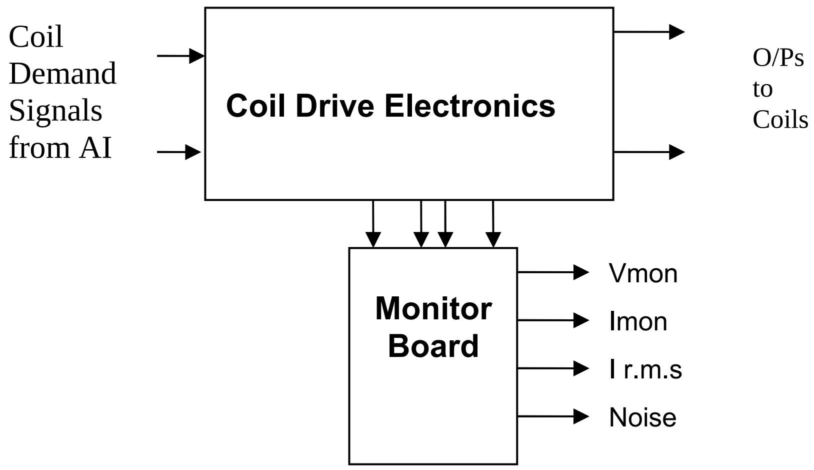


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..26/5/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P22…………………….Serial No ……………………………….
Test Engineer…..Xen…….…………….
Date……………..26/5/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on channels 1, 2 and 3.

Unit………………Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/5/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

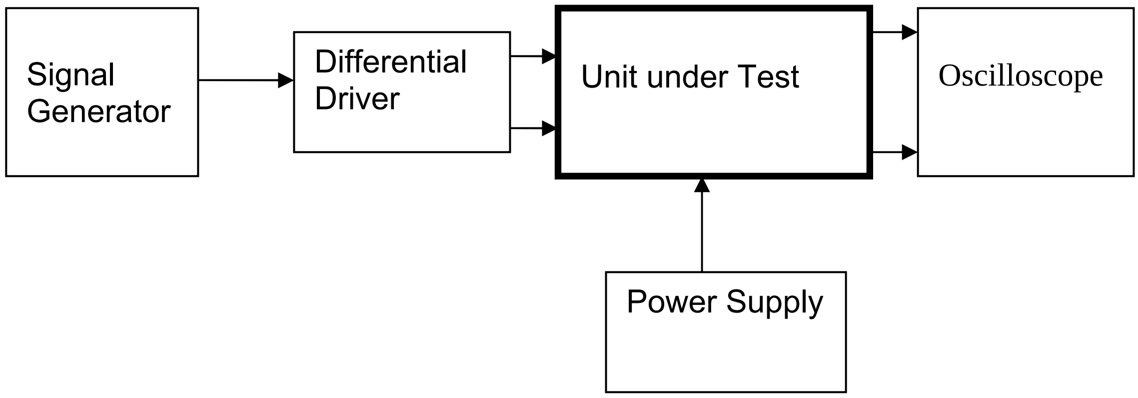
Unit..................Q_TOP_P22........................Serial No ....
Test Engineer.....Xen.......................
Date.................26/5/10..................

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..26/5/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	600mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..26/5/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..26/5/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.017	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.008	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.012	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.013	√

Unit……………..Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.23	2.9μV√Hz	√
2		1.12	2.9μV√Hz	√
3		0.99	2.9μV√Hz	√
4		1.52	2.9μV√Hz	√

Unit……………..Q_TOP_P22……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..4/6/10………………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit.................Q_TOP_P22.......................Serial No ....
Test Engineer.....Xen.......................
Date................4/6/10...................

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

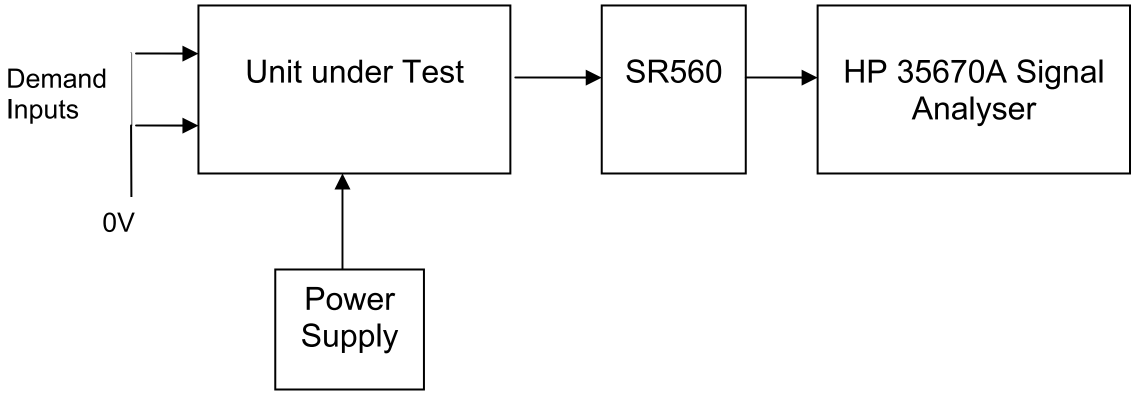
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	44.5	√
CH1 Negative			CH1 IC5	45.5	√
CH2 Positive	24.38	√	CH2 IC1	45.7	√
CH2 Negative			CH2 IC5	44.0	√
CH3 Positive	24.39	√	CH3 IC1	45.0	√
CH3 Negative			CH3 IC5	45.3	√
CH4 Positive	24.38	√	CH4 IC1	44.3	√
CH4 Negative			CH4 IC5	42.8	√

Unit……………..Q_TOP_P22…………………..Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..8/6/10..………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-101.6	-161.6
Ch2	-161.15dB	-101.9	-161.9
Ch3	-161.15dB	-101.2	-161.2
Ch4	-161.15dB	-100.5	-160.5

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit.................Q_TOP_P22.......................Serial No ....
Test Engineer.....Xen.......................
Date................4/6/10...................

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.40	137.1mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit………… QTOP22P …………………Serial No ………………………………
Test Engineer ………RMC
Date …………………6.7/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP22P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP22P
Driver board Serial Number	QTOP22P
Monitor board ID	MON95
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON95

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

Drive Card ID……Q_TOP23P………
Monitor Card ID…Mon86…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

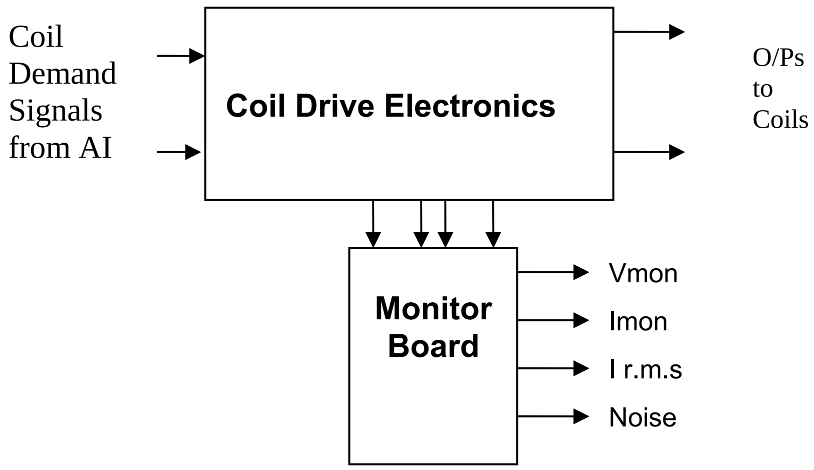


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..Q_TOP_P23……………………Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

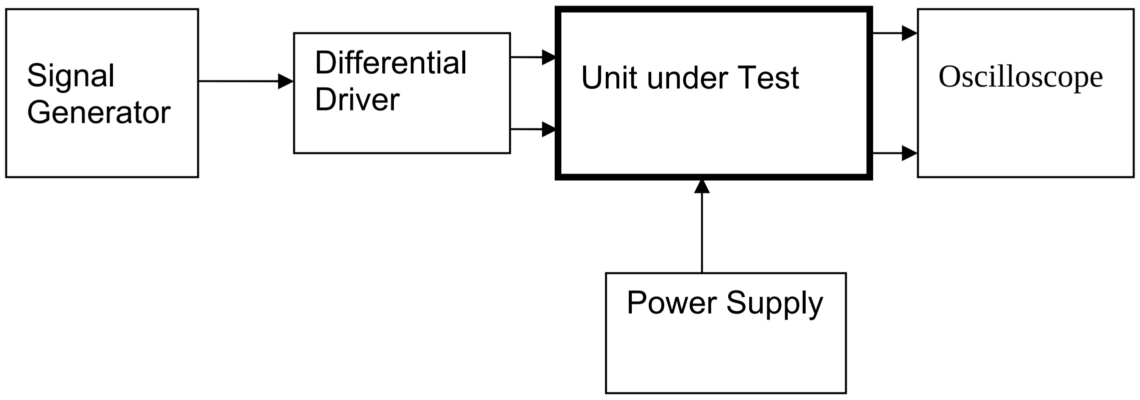
Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1
Ch2+ = Coil out to Sat pin 3
Ch3+ = Coil out to Sat pin 5
Ch4+ = Coil out to Sat pin 7
Ch1- = Coil out to Sat pin 9
Ch2- = Coil out to Sat pin 11
Ch3- = Coil out to Sat pin 13
Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.015	√
2	Pin 5	Current Monitor	1v r.m.s	1.016	√
	Pin 4	RMS Current	1v dc	1.015	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.017	√

Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.07	2.9μV√Hz	√
2		1.20	2.9μV√Hz	√
3		0.91	2.9μV√Hz	√
4		1.66	2.9μV√Hz	√

Unit……………..Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

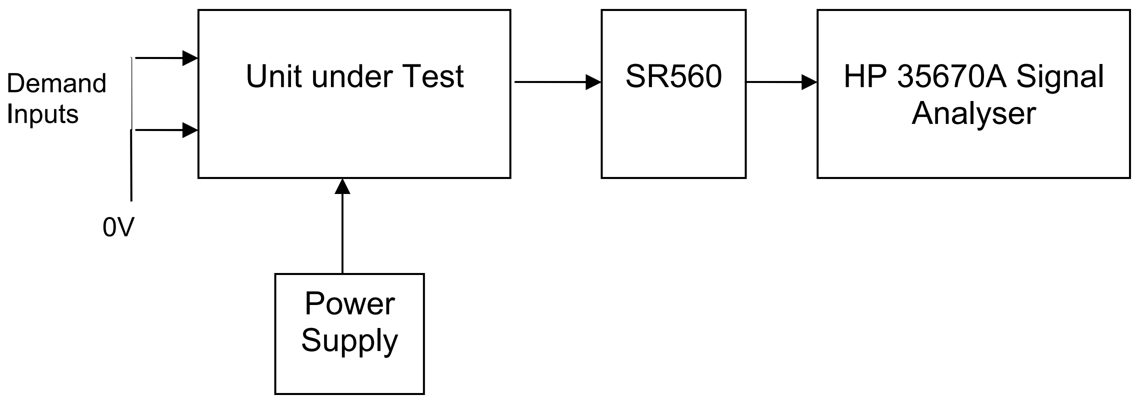
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.40	√	**CH1 IC1**	42.6	√
CH1 Negative			**CH1 IC5**	42.3	√
CH2 Positive	24.40	√	**CH2 IC1**	45.0	√
CH2 Negative			**CH2 IC5**	46.0	√
CH3 Positive	24.38	√	**CH3 IC1**	44.8	√
CH3 Negative			**CH3 IC5**	45.0	√
CH4 Positive	24.39	√	**CH4 IC1**	42.8	√
CH4 Negative			**CH4 IC5**	46.2	√

Unit……………..Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..8/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100.9	-160.9
Ch2	-161.15dB	-100.2	-160.2
Ch3	-161.15dB	-101.2	-161.2
Ch4	-161.15dB	-98.6	-158.6

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit………………Q_TOP_P23……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..7/6/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP23P..........................Serial No ....
Test Engineer ....RMC
Date 6/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP23P
Driver board ID	D0902747_V9
Driver board Drawing No/Issue No	QTOP23P
Driver board Serial Number	QTOP23P
Monitor board ID	MON86
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON86

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..28/4/10……………..

Drive Card ID……Q_TOP24P………
Monitor Card ID…Mon94…...………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

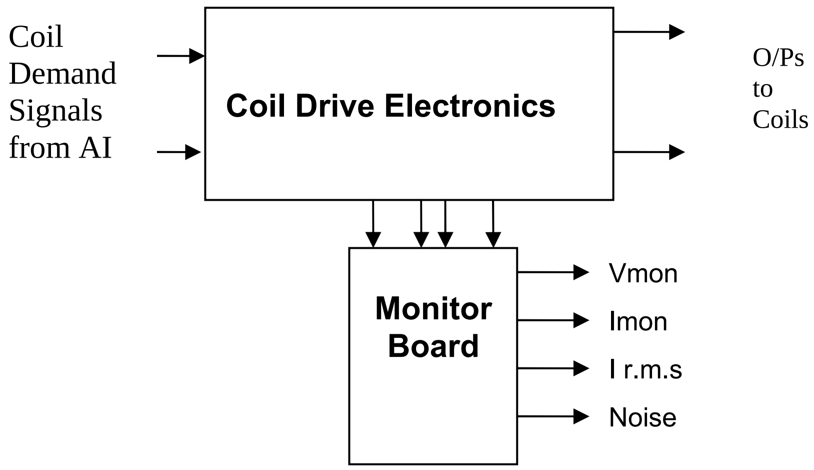


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P24…………………….Serial No ……………………………….
Test Engineer…..Xen…….…………….
Date……………..28/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P24……………………Serial No ……………………………….
Test Engineer…..Xen…….…………….
Date……………..28/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1, 2 and 3.

Unit……………….Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..28/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

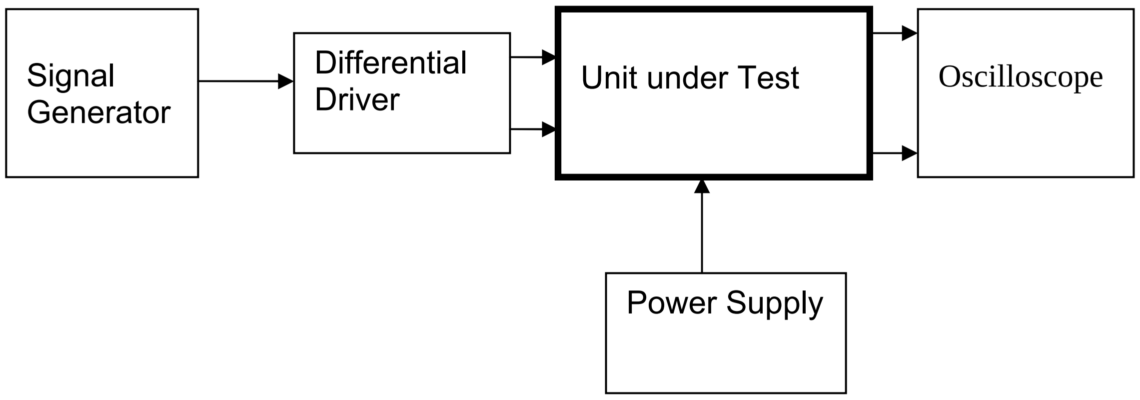
Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..28/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.009	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.018	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.014	√

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.91	2.9μV√Hz	√
2		0.94	2.9μV√Hz	√
3		1.17	2.9μV√Hz	√
4		1.29	2.9μV√Hz	√

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.89		
Ch2	4.89		
Ch3	4.89		
Ch4	4.89		

Unit……………..Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

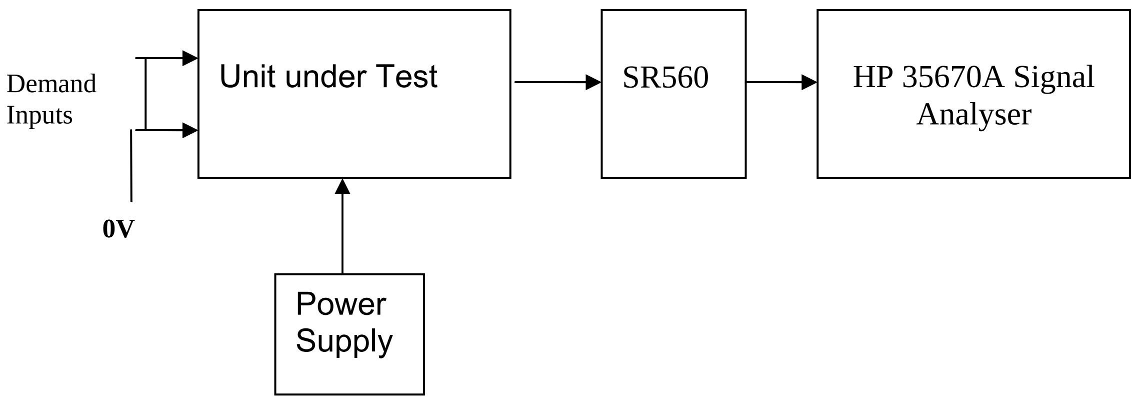
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	**CH1 IC1**	42.1	√
CH1 Negative			**CH1 IC5**	44.8	√
CH2 Positive	24.38	√	**CH2 IC1**	43.8	√
CH2 Negative			**CH2 IC5**	43.3	√
CH3 Positive	24.38	√	**CH3 IC1**	44.8	√
CH3 Negative			**CH3 IC5**	49.1	√
CH4 Positive	24.38	√	**CH4 IC1**	46.0	√
CH4 Negative			**CH4 IC5**	47.7	√

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…...………………
Date……………..18/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston’s noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.6	-161.6
Ch2	-161.15dB	-99.6	-159.6
Ch3	-161.15dB	-102.6	-162.6
Ch4	-161.15dB	-100.5	-160.5

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P24……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP24P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………1/7/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP24P
Driver board ID	QTOP24P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP24P
Monitor board ID	MON94
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON94

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

Drive Card ID……Q_TOP25P………
Monitor Card ID…Mon93…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

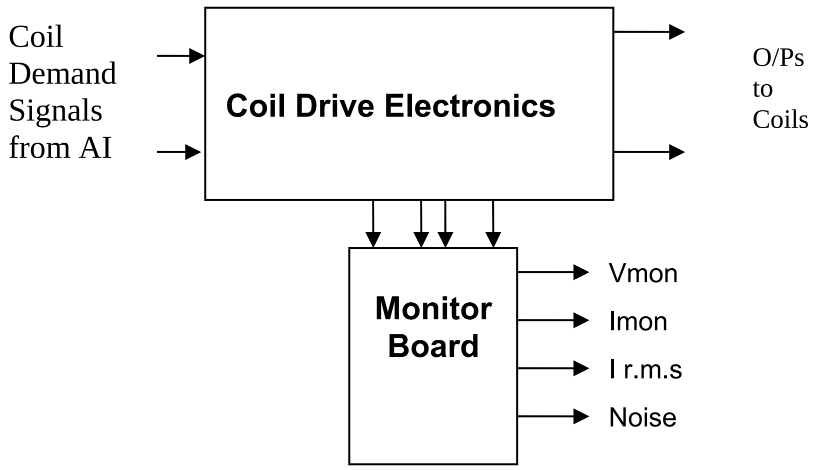


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………...Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..28/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P25…………………….Serial No ……………………………….
Test Engineer…..Xen……..…………..
Date……………..27/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH3.

Unit……………….Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

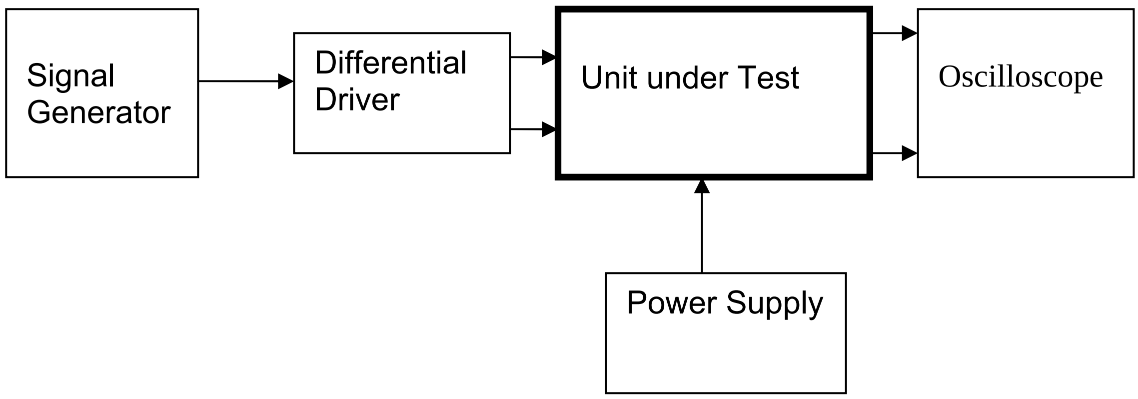
Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..27/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..27/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen……………………
Date……………..27/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.015	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.018	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.012	√

Unit..................Q_TOP_P25........................Serial No ....
Test Engineer.....Xen.......................
Date.................27/4/10..................

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.45	2.9μV√Hz	√
2		1.03	2.9μV√Hz	√
3		1.09	2.9μV√Hz	√
4		1.61	2.9μV√Hz	√

Unit……………..Q_TOP_P25…………………..Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.89		
Ch2	4.89		
Ch3	4.89		
Ch4	4.89		

Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

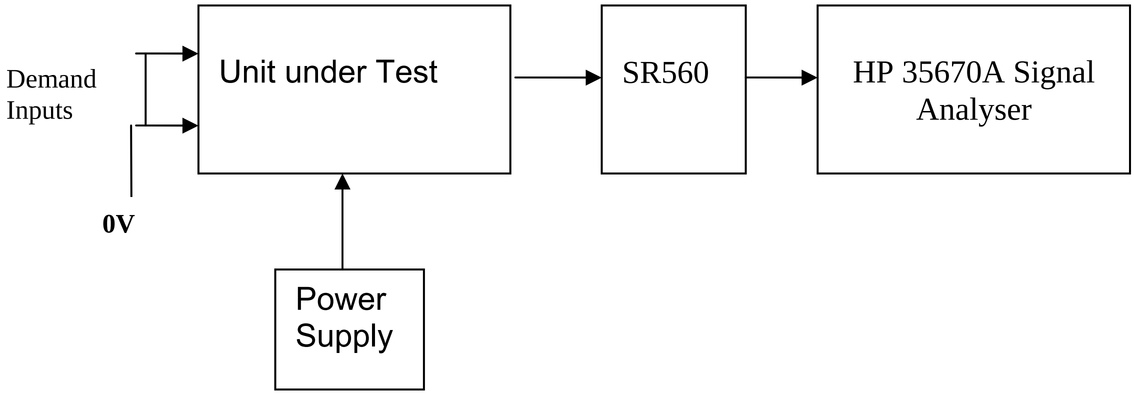
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	**CH1 IC1**	41.4	√
CH1 Negative			**CH1 IC5**	46.5	√
CH2 Positive	24.36	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	43.1	√
CH3 Positive	24.36	√	**CH3 IC1**	43.8	√
CH3 Negative			**CH3 IC5**	45.7	√
CH4 Positive	24.37	√	**CH4 IC1**	43.3	√
CH4 Negative			**CH4 IC5**	45.7	√

Unit……………..Q_TOP_P25…………………..Serial No ……………………………
Test Engineer…..Xen…….…………….
Date……………..16/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100.6	-160.6
Ch2	-161.15dB	-100.8	-160.8
Ch3	-161.15dB	-102.2	-162.2
Ch4	-161.15dB	-101.3	-161.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P25……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..28/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP25P....................Serial No ....
Test Engineer ....RMC
Date 1/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP25P
Driver board ID	QTOP25P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP25P
Monitor board ID	MON93
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON93

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P26……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..27/4/10………………

Drive Card ID……Q_TOP26P………
Monitor Card ID…Mon92…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

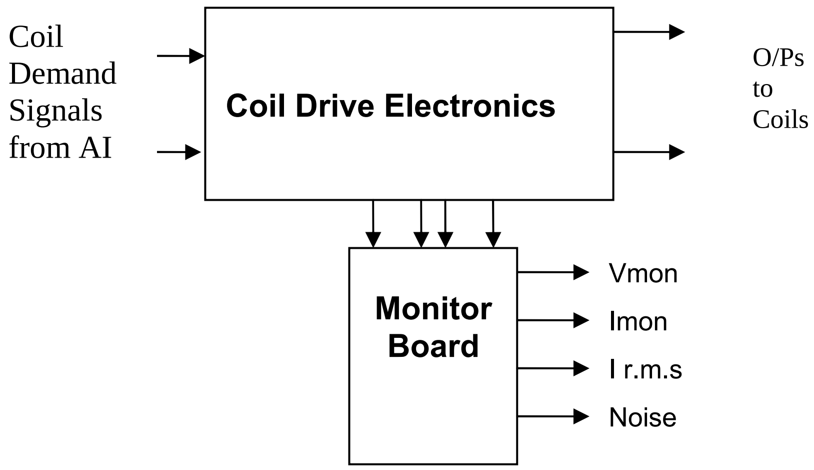

FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P26……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

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3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

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4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

Unit………………Q_TOP_P26……………………Serial No ………………………………
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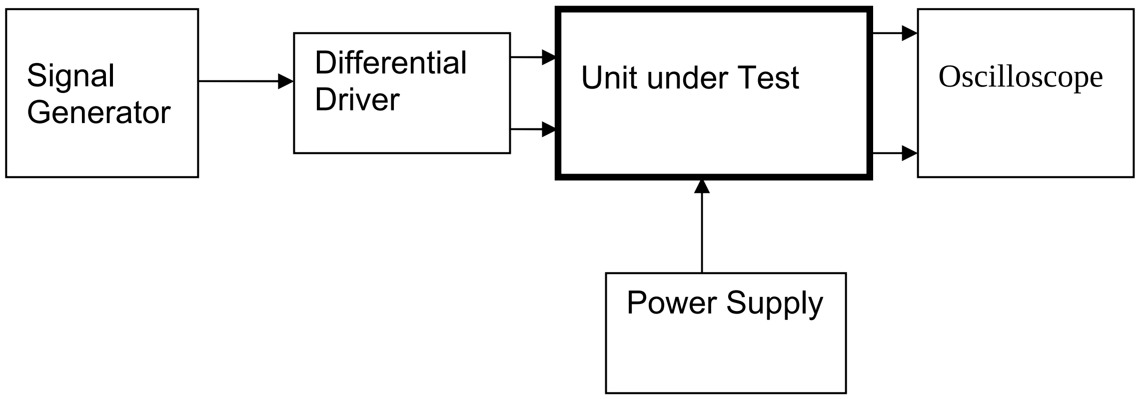
Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P26……………………Serial No ………………………………
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6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P26……………………Serial No ………………………………
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

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8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.011	√

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9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.11	2.9μV√Hz	√
2		1.15	2.9μV√Hz	√
3		1.31	2.9μV√Hz	√
4		1.05	2.9μV√Hz	√

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10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.9		
Ch2	4.9		
Ch3	4.9		
Ch4	4.9		

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11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	42.3	√
CH1 Negative			CH1 IC5	45.7	√
CH2 Positive	24.38	√	CH2 IC1	44.0	√
CH2 Negative			CH2 IC5	47.7	√
CH3 Positive	24.37	√	CH3 IC1	48.7	√
CH3 Negative			CH3 IC5	47.2	√
CH4 Positive	24.38	√	CH4 IC1	44.3	√
CH4 Negative			CH4 IC5	48.9	√

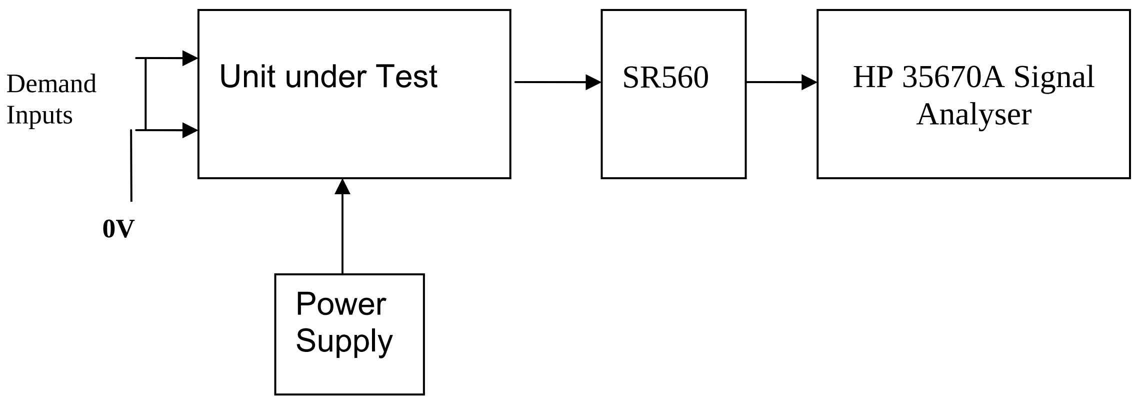
Unit……………..Q_TOP_P26…………………..Serial No ……………………………
Test Engineer…..Xen……..……………
Date……………..15/6/10……………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.6	-161.6
Ch2	-161.15dB	-100.9	-160.9
Ch3	-161.15dB	-101.7	-161.7
Ch4	-161.15dB	-98.2	-158.2

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

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14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Test Engineer ………RMC
Date …………………1/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP26
Driver board ID	QTOP26
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP26
Monitor board ID	MON92
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON92

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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Drive Card ID……Q_TOP27P………
Monitor Card ID…Mon201…………..

Contents

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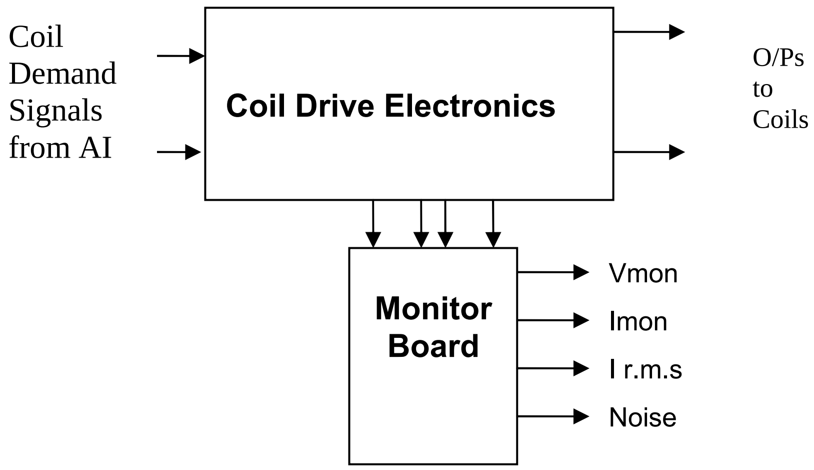

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DVM	Fluke	77III	
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3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 3 & 4.

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4. Continuity Checks

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2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

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Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
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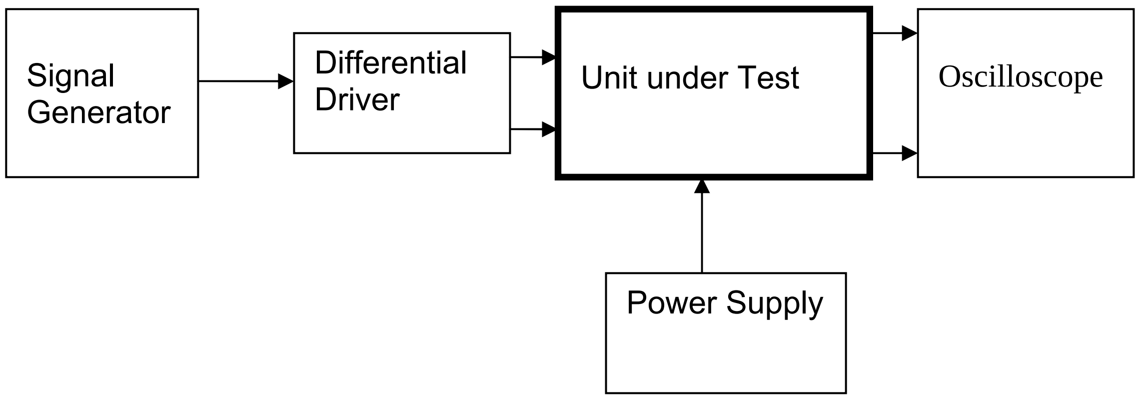
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.015	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.016	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.022	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit……………..Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.39	2.9μV√Hz	√
2		1.10	2.9μV√Hz	√
3		1.07	2.9μV√Hz	√
4		1.14	2.9μV√Hz	√

Unit……………..Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..27/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

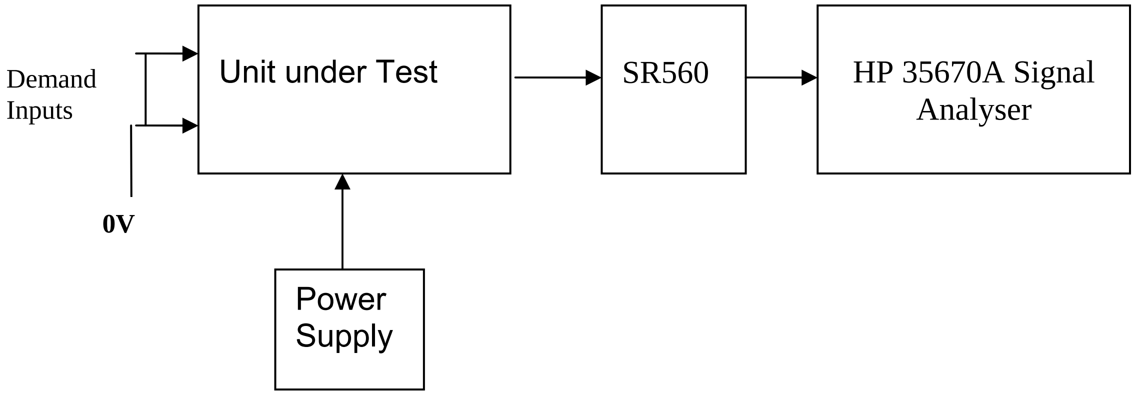
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.37	√	**CH1 IC1**	41.4	√
CH1 Negative			**CH1 IC5**	47.2	√
CH2 Positive	24.37	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	46.5	√
CH3 Positive	24.37	√	**CH3 IC1**	44.0	√
CH3 Negative			**CH3 IC5**	46.2	√
CH4 Positive	24.37	√	**CH4 IC1**	43.6	√
CH4 Negative			**CH4 IC5**	46.0	√

Unit……………..Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..15/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100.0	-160.0
Ch2	-161.15dB	-100.1	-160.1
Ch3	-161.15dB	-103.3	-163.3
Ch4	-161.15dB	-100.4	-160.4

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P27……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………QTOP27P………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………1/7/10

15. Final Assembly Checks

1. Remove the lid of the box.√

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP27P
Driver board ID	QTOP27P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP27P
Monitor board ID	MON201
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON201

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..27/4/10……………..

Drive Card ID……Q_TOP28P………
Monitor Card ID…Mon203…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

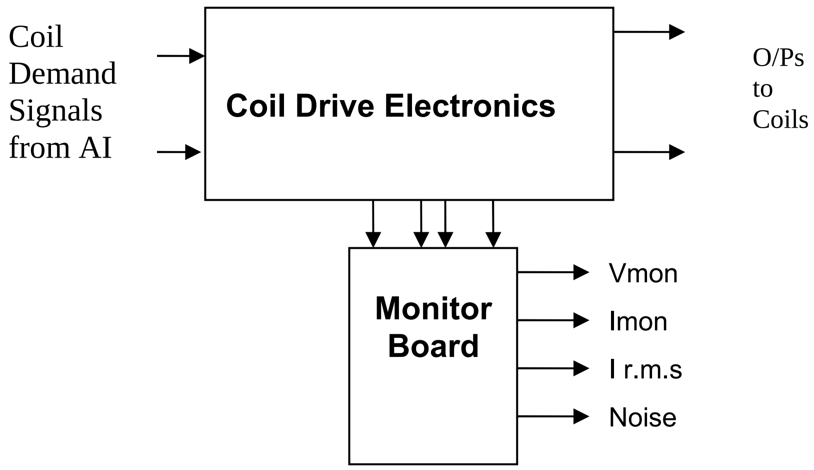


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..27/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CHs 2, 3 & 4.

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..27/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

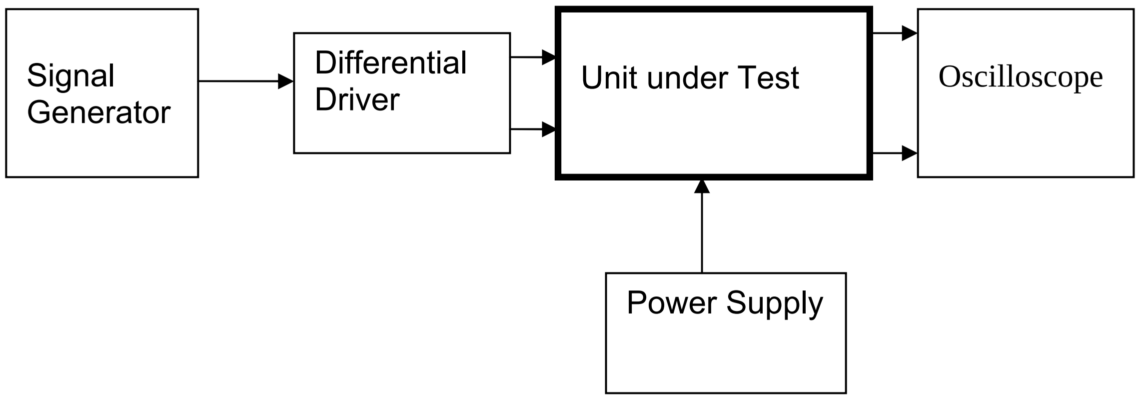
Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	**Monitor Connector**	**Parameter**	**Theoretical Value (+/- .1v)**	**Measured Value**	**Pass/ Fail**
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.013	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.012	√

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.31	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.06	2.9μV√Hz	√
2		1.28	2.9μV√Hz	√
3		0.82	2.9μV√Hz	√
4		1.86	2.9μV√Hz	√

Unit..................Q_TOP_P28........................Serial No ....
Test Engineer.....Xen.......................
Date.................27/4/10..................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

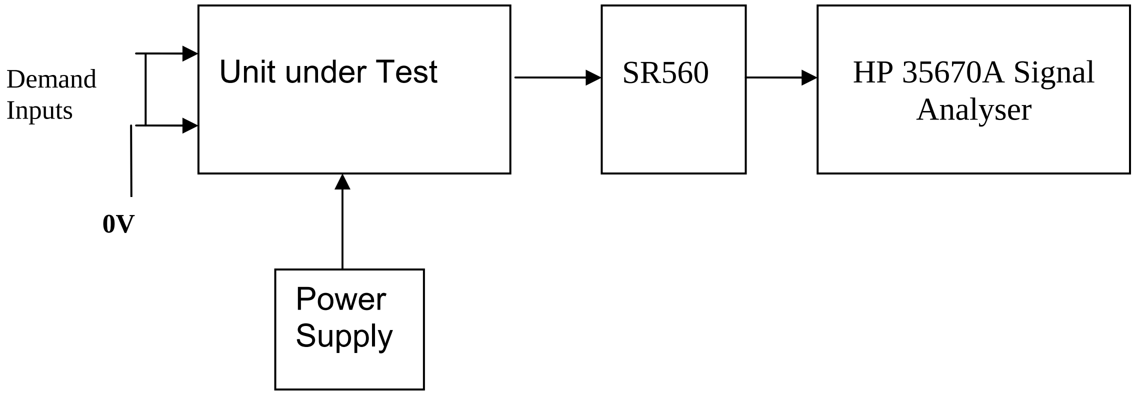
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.37	√	**CH1 IC1**	43.8	√
CH1 Negative			**CH1 IC5**	45.7	√
CH2 Positive	24.37	√	**CH2 IC1**	45.7	√
CH2 Negative			**CH2 IC5**	46.0	√
CH3 Positive	24.37	√	**CH3 IC1**	44.0	√
CH3 Negative			**CH3 IC5**	46.5	√
CH4 Positive	24.37	√	**CH4 IC1**	44.0	√
CH4 Negative			**CH4 IC5**	46.2	√

Unit……………..Q_TOP_P28…………………..Serial No ……………………………
Test Engineer…..Xen……..…………
Date……………..15/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.0	-161.0
Ch2	-161.15dB	-100.5	-160.5
Ch3	-161.15dB	-101.6	-161.6
Ch4	-161.15dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P28……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.55	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……QTOP28P…………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP28P
Driver board ID	QTOP28P
Driver board Drawing No/Issue No	D0902747_V_9
Driver board Serial Number	QTOP28P
Monitor board ID	MON203
Monitor board Drawing No/Issue No	DO70480_4_K
Monitor board Serial Number	MON203

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

Drive Card ID……Q_TOP29P………
Monitor Card ID…Mon202…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

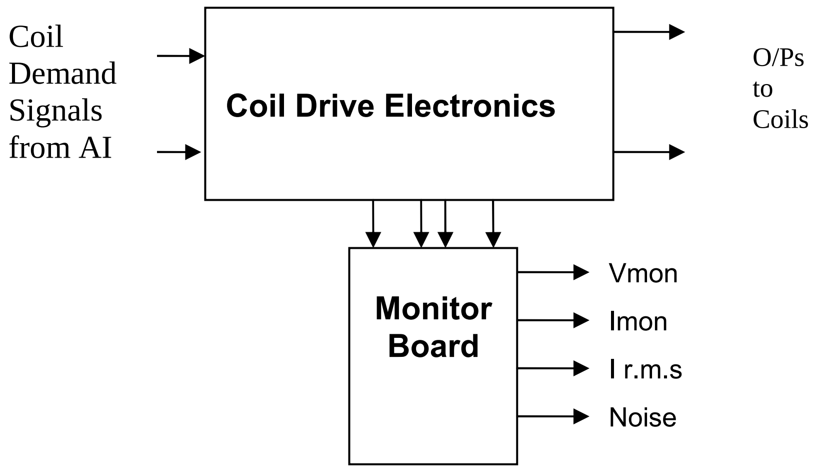


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..27/4/10……………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

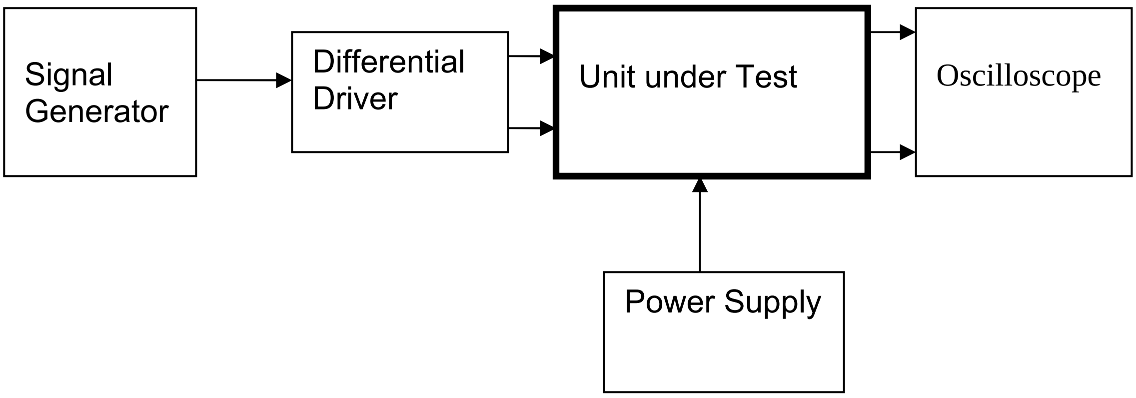
Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..27/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.014	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.020	√
3	Pin 8	Current Monitor	1v r.m.s	1.012	√
	Pin 7	RMS Current	1v dc	1.018	√
4	Pin 11	Current Monitor	1v r.m.s	1.011	√
	Pin 10	RMS Current	1v dc	1.010	√

Unit……………...Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.5	2.9μV√Hz	√
2		1.6	2.9μV√Hz	√
3		1.5	2.9μV√Hz	√
4		1.23	2.9μV√Hz	√

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P29……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

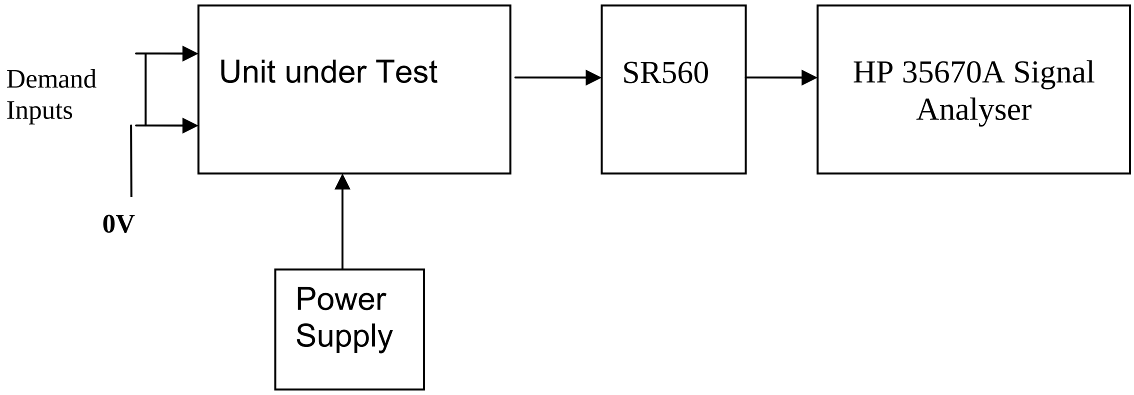
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	**CH1 IC1**	41.1	√
CH1 Negative			**CH1 IC5**	42.1	√
CH2 Positive	24.36	√	**CH2 IC1**	42.3	√
CH2 Negative			**CH2 IC5**	43.6	√
CH3 Positive	24.36	√	**CH3 IC1**	43.6	√
CH3 Negative			**CH3 IC5**	46.7	√
CH4 Positive	24.36	√	**CH4 IC1**	42.6	√
CH4 Negative			**CH4 IC5**	44.0	√

Unit.................Q_TOP_P29.......................Serial No ....
Test Engineer.....Xen......................
Date................25/5/10..................

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.7	-159.7
Ch2	-161.15dB	-100.2	-160.2
Ch3	-161.15dB	-98.1	-158.1
Ch4	-161.15dB	-98.3	-158.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P29…………………..Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..27/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………QTOP29P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP29P
Driver board ID	QTOP29P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP29P
Monitor board ID	MON202
Monitor board Drawing No/Issue No	D070_04_K
Monitor board Serial Number	MON202

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen………..…………
Date……………..26/4/10………………

Drive Card ID……Q_TOP30P………
Monitor Card ID…Mon200…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

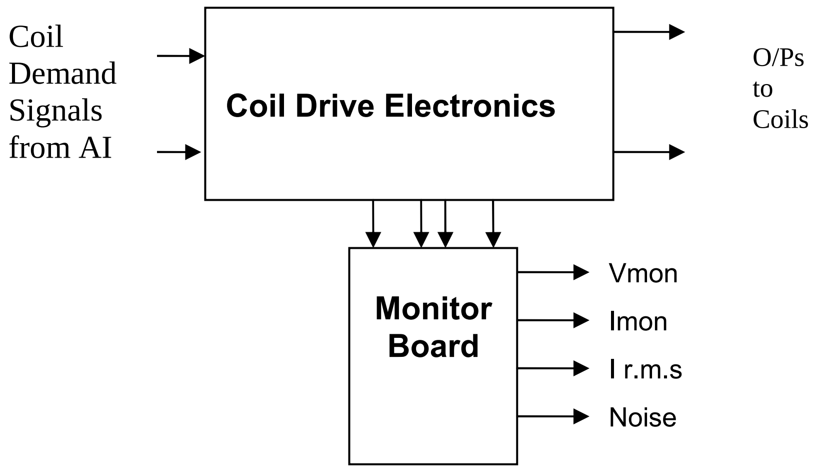


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P30…………………….Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CH3.

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

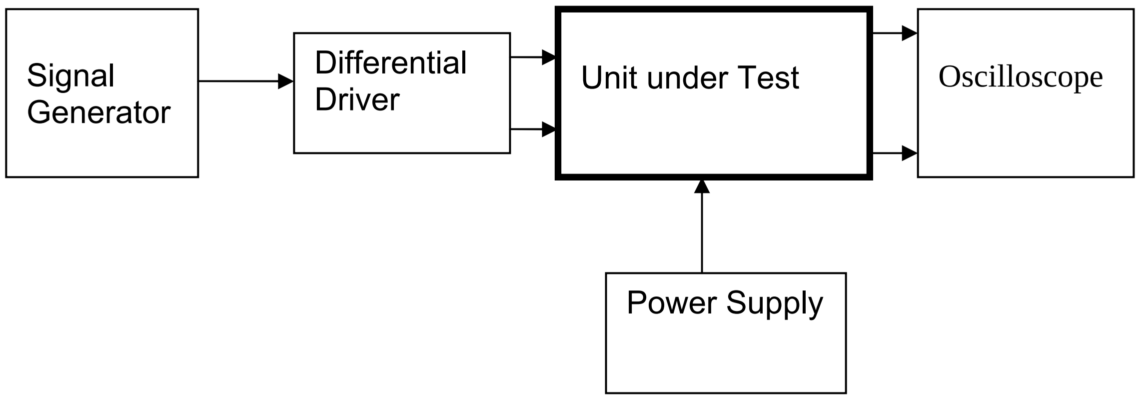
Unit……………….Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………….Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.013	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.019	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit……………..Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..26/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.87	2.9μV√Hz	√
2		1.61	2.9μV√Hz	√
3		1.49	2.9μV√Hz	√
4		1.25	2.9μV√Hz	√

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	**CH1 IC1**	40.6	√
CH1 Negative			**CH1 IC5**	47.7	√
CH2 Positive	24.37	√	**CH2 IC1**	46.5	√
CH2 Negative			**CH2 IC5**	44.3	√
CH3 Positive	24.38	√	**CH3 IC1**	46.2	√
CH3 Negative			**CH3 IC5**	46.5	√
CH4 Positive	24.38	√	**CH4 IC1**	44.0	√
CH4 Negative			**CH4 IC5**	46.5	√

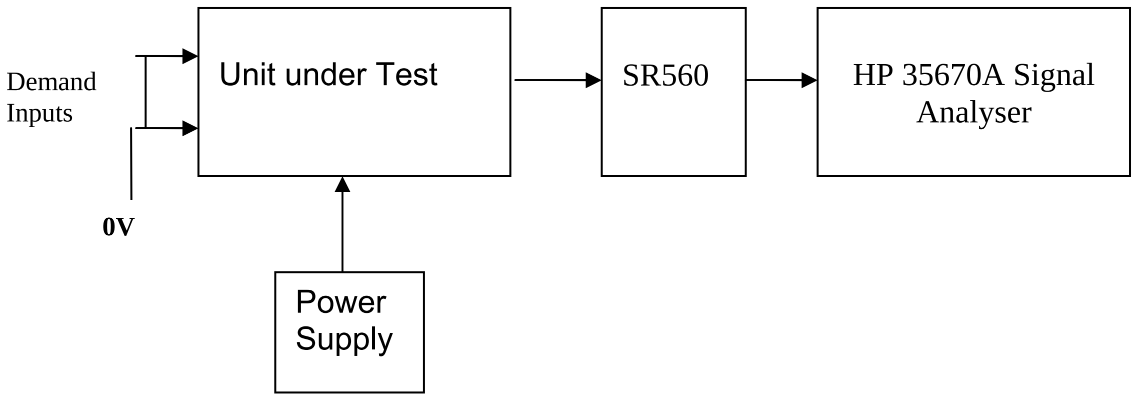
Unit……………….Q_TOP_P30…………………….Serial No ……………………………….
Test Engineer…..Xen…...……………….
Date……………..17/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.8	-159.8
Ch2	-161.15dB	-101.4	-161.4
Ch3	-161.15dB	-100.9	-160.9
Ch4	-161.15dB	-103.0	-163.0

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………….Q_TOP_P30……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit.........QTOP30P................................Serial No ....
Test Engineer ....RMC
Date 1/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP30P
Driver board ID	QTOP30P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP30P
Monitor board ID	MON200
Monitor board Drawing No/Issue No	DO70480_4_K
Monitor board Serial Number	MON200

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

Drive Card ID……Q_TOP31P………
Monitor Card ID…Mon99…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

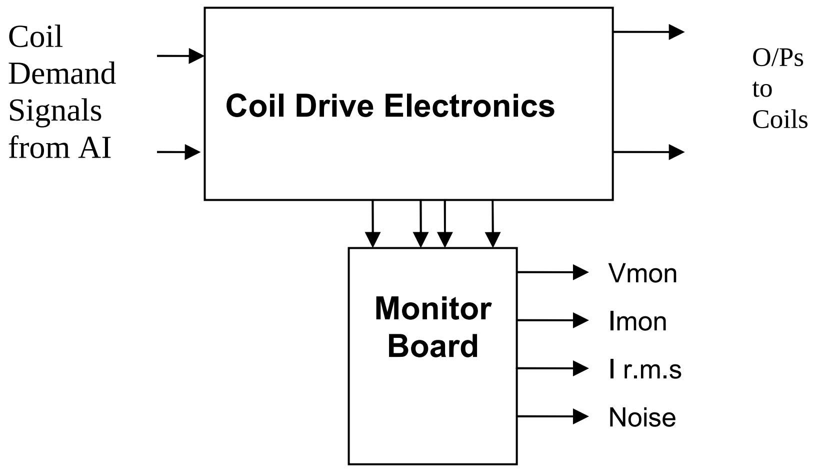


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 2 & 3.

Unit………………Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

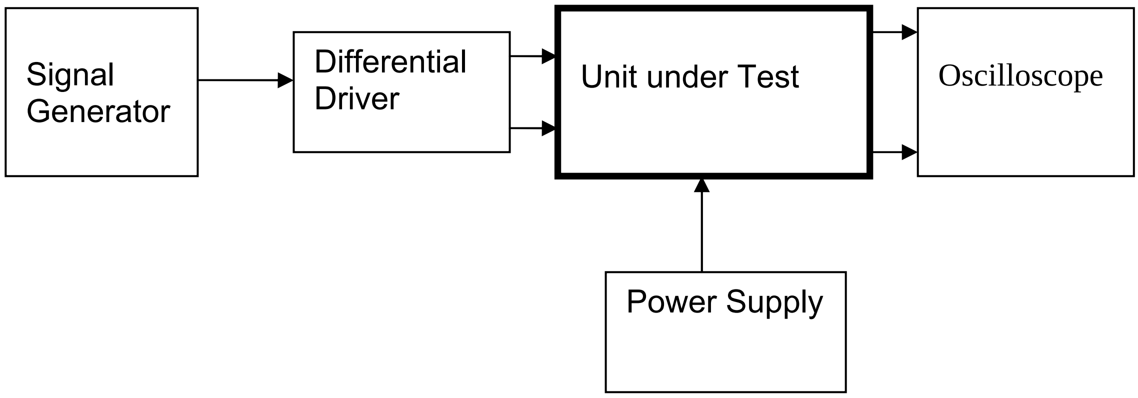
Unit……………….Q_TOP_P31…………………….Serial No ……………………………….
Test Engineer…..Xen………………….
Date……………..26/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.022	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.021	√
3	Pin 8	Current Monitor	1v r.m.s	1.016	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.017	√

Unit……………….Q_TOP_P31…………………….Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.32	2.9μV√Hz	√
2		0.93	2.9μV√Hz	√
3		0.89	2.9μV√Hz	√
4		1.42	2.9μV√Hz	√

Unit……………..Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…..................
Date……………..26/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.37	√	**CH1 IC1**	42.6	√
CH1 Negative			**CH1 IC5**	43.8	√
CH2 Positive	24.38	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	45.7	√
CH3 Positive	24.38	√	**CH3 IC1**	45.0	√
CH3 Negative			**CH3 IC5**	47.2	√
CH4 Positive	24.38	√	**CH4 IC1**	43.8	√
CH4 Negative			**CH4 IC5**	47.7	√

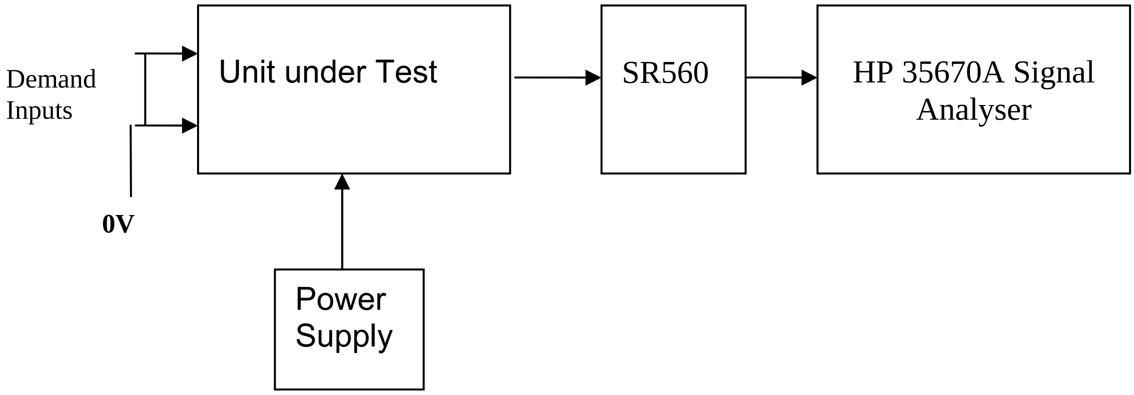
Unit……………..Q_TOP_P31…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..18/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.3	-161.3
Ch2	-161.15dB	-103.0	-163.0
Ch3	-161.15dB	-101.4	-161.4
Ch4	-161.15dB	-102.7	-162.7

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P31……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP31P.................Serial No ....
Test Engineer ....RMC
Date 1/7/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP31P
Driver board ID	QTOP31P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP31P
Monitor board ID	MON99
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON99

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..26/4/10………………

Drive Card ID……Q_TOP32P………
Monitor Card ID…Mon98…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

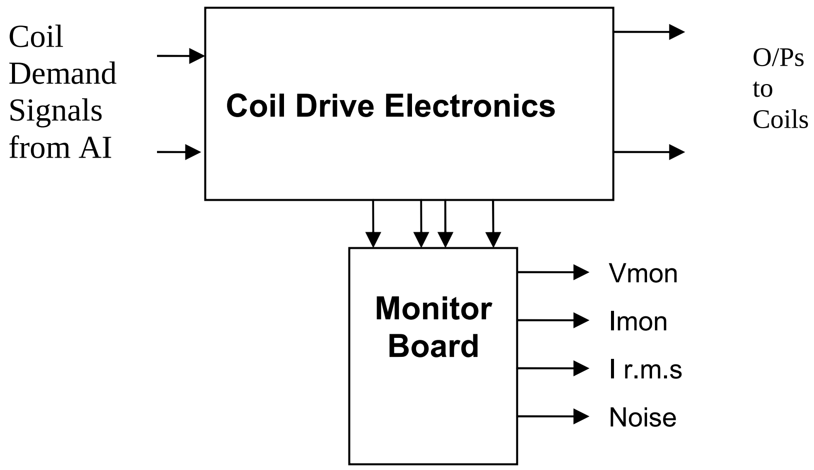


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen……..…………….
Date……………..26/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P32…………………….Serial No ……………………………….
Test Engineer…..Xen……..……………
Date……………..26/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 1, 2 & 3.

Unit……………..Q_TOP_P32…………………..Serial No ……………………………
Test Engineer…..Xen…….…………….
Date……………..26/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

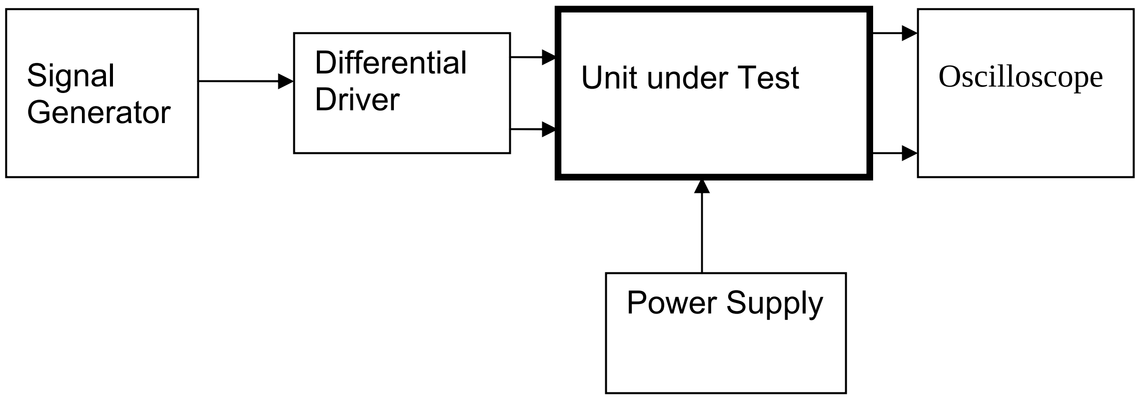
Unit………………Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..26/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..26/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..26/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.016	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit……………….Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.74	2.9μV√Hz	√
2		1.07	2.9μV√Hz	√
3		1.02	2.9μV√Hz	√
4		0.97	2.9μV√Hz	√

Unit.................Q_TOP_P32.......................Serial No ....
Test Engineer.....Xen.......................
Date................26/4/10.................

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

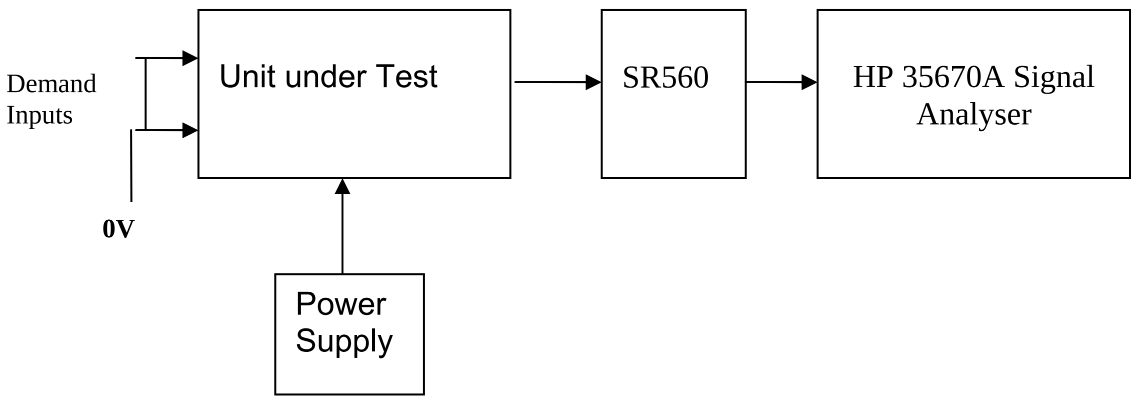
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	**CH1 IC1**	40.6	√
CH1 Negative			**CH1 IC5**	44.0	√
CH2 Positive	24.38	√	**CH2 IC1**	43.8	√
CH2 Negative			**CH2 IC5**	46.0	√
CH3 Positive	24.39	√	**CH3 IC1**	44.5	√
CH3 Negative			**CH3 IC5**	45.3	√
CH4 Positive	24.39	√	**CH4 IC1**	43.3	√
CH4 Negative			**CH4 IC5**	42.8	√

Unit……………..Q_TOP_P32…………………..Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..18/6/10……………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100.9	-160.9
Ch2	-161.15dB	-100.2	-160.2
Ch3	-161.15dB	-101.8	-161.8
Ch4	-161.15dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P32……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.54	141.0mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.54	141.0mA	>200mA	>141.4mA	√
4	39.4	5.54	140.6mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit.............. QTOP32P..........................Serial No ....
Test Engineer ....RMC
Date 30/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP32P
Driver board ID	QTOP32P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP32P
Monitor board ID	MON98
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON98

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

Drive Card ID……Q_TOP33P………
Monitor Card ID…Mon119…………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

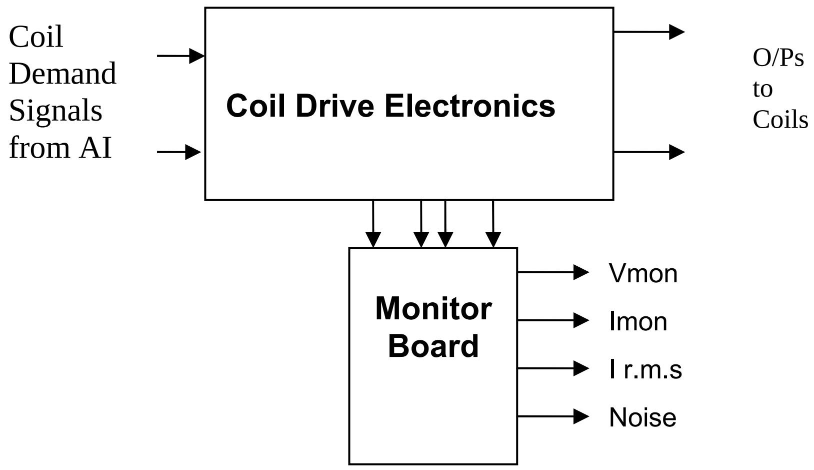


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..23/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..23/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

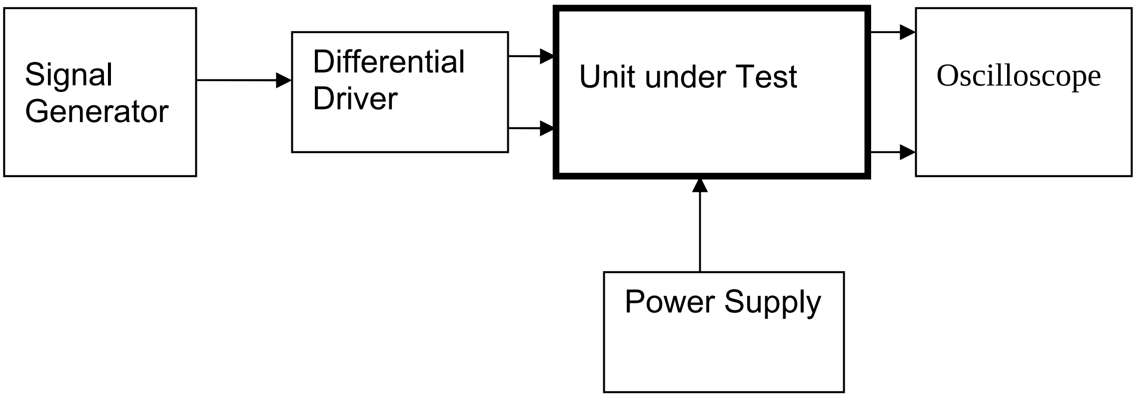
Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..23/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..23/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..23/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..23/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.015	√
2	Pin 5	Current Monitor	1v r.m.s	1.011	√
	Pin 4	RMS Current	1v dc	1.014	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.019	√

Unit……………..Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.59	2.9μV√Hz	√
2		1.07	2.9μV√Hz	√
3		1.32	2.9μV√Hz	√
4		0.90	2.9μV√Hz	√

Unit……………..Q_TOP_P33…………………..Serial No …………………………….
Test Engineer…..Xen…….…………….
Date……………..23/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..Q_TOP_P33……………………Serial No ……………………………
Test Engineer…..Xen………………….
Date……………..26/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	**CH1 IC1**	40.1	√
CH1 Negative			**CH1 IC5**	43.6	√
CH2 Positive	24.37	√	**CH2 IC1**	43.6	√
CH2 Negative			**CH2 IC5**	44.5	√
CH3 Positive	24.38	√	**CH3 IC1**	43.8	√
CH3 Negative			**CH3 IC5**	44.8	√
CH4 Positive	24.38	√	**CH4 IC1**	42.1	√
CH4 Negative			**CH4 IC5**	44.0	√

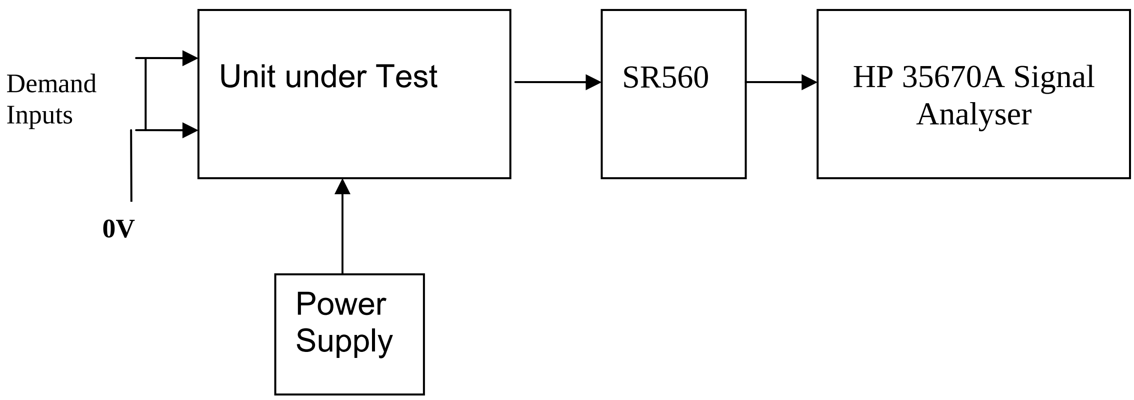
Unit………………Q_TOP_P33……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..17/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-102.5	-162.5
Ch2	-161.15dB	-99.7	-159.7
Ch3	-161.15dB	-101.0	-161.0
Ch4	-161.15dB	-100.9	-160.9

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P33…………………..Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..26/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.59	141.9mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………..QTOP33P……………..Serial No ……………………………
Test Engineer ……RMC
Date ……………..30/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP33P
Driver board ID	QTOP33P
Driver board Drawing No/Issue No	D0902747P_V9
Driver board Serial Number	QTOP33P
Monitor board ID	MON119
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON119

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10..……………

Drive Card ID……Q_TOP34P………
Monitor Card ID…Mon91…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

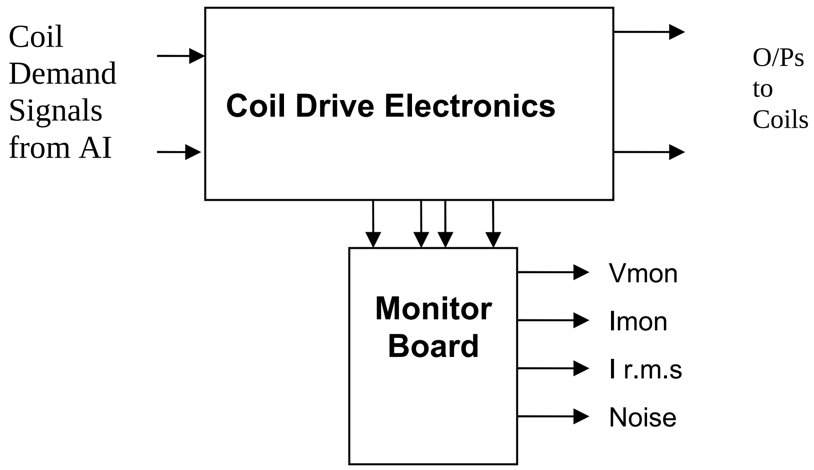


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10..……………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced with the AD8671 op-amp on CH4.

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

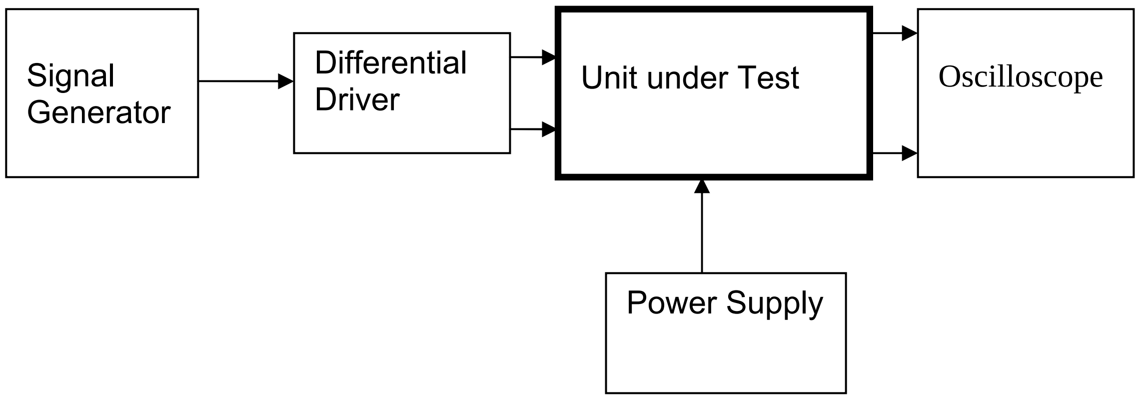
Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10..……………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)
Pd In from Sat pin 9, 10 = +16.5v or DC in A1
Pd In from Sat pin 11, 12 = -16.5 or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v or DC in A2

Coil Drive Outputs
Ch1+ = Coil out to Sat pin 1 Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3 Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5 Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7 Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10..……………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10……………..

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.010	√

Unit……………..Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.31	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.14	2.9μV√Hz	√
2		1.36	2.9μV√Hz	√
3		1.01	2.9μV√Hz	√
4		1.07	2.9μV√Hz	√

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10..……………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	-1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

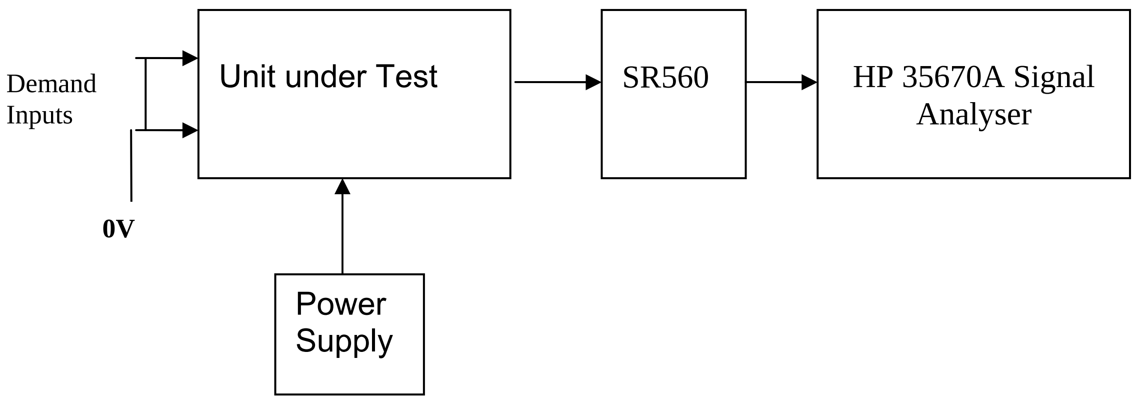
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	**CH1 IC1**	43.1	√
CH1 Negative			**CH1 IC5**	45.5	√
CH2 Positive	24.38	√	**CH2 IC1**	44.5	√
CH2 Negative			**CH2 IC5**	45.5	√
CH3 Positive	24.39	√	**CH3 IC1**	44.0	√
CH3 Negative			**CH3 IC5**	47.0	√
CH4 Positive	24.39	√	**CH4 IC1**	44.0	√
CH4 Negative			**CH4 IC5**	46.2	√

Unit……………..Q_TOP_P34…………………..Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..17/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.5	-161.5
Ch2	-161.15dB	-100.4	-160.4
Ch3	-161.15dB	-100.3	-160.3
Ch4	-161.15dB	-101.4	-161.4

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P34……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/4/10...……………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.54	140.6mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP34P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………30/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP34P
Driver board ID	QTOP34P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP34P
Monitor board ID	MON91
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON91

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

Drive Card ID……Q_TOP35P………
Monitor Card ID…Mon90…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

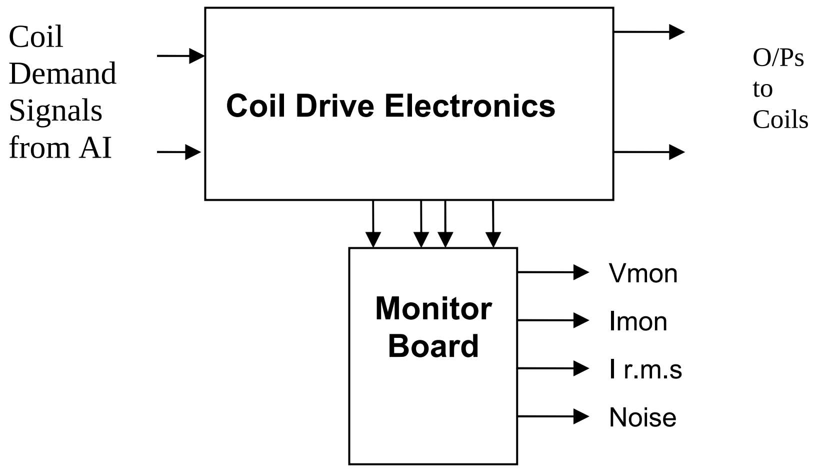


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P35…………………….Serial No ……………………………….
Test Engineer…..Xen…………………
Date……………..23/410………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..22/410……………..

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………….Q_TOP_P35…………………….Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..22/410………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

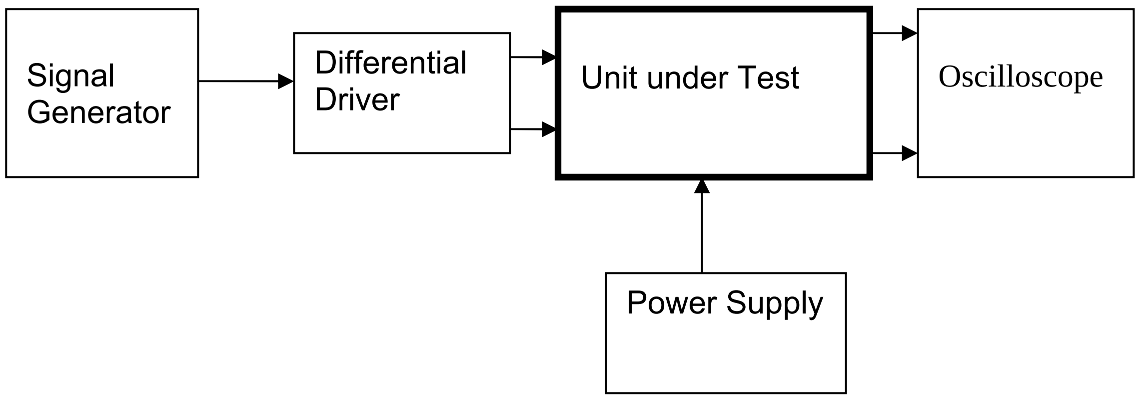
Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..22/410………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.012	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.012	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.007	√

Unit……………..Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		0.94	2.9μV√Hz	√
2		0.86	2.9μV√Hz	√
3		0.99	2.9μV√Hz	√
4		1.27	2.9μV√Hz	√

Unit……………..Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.8		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

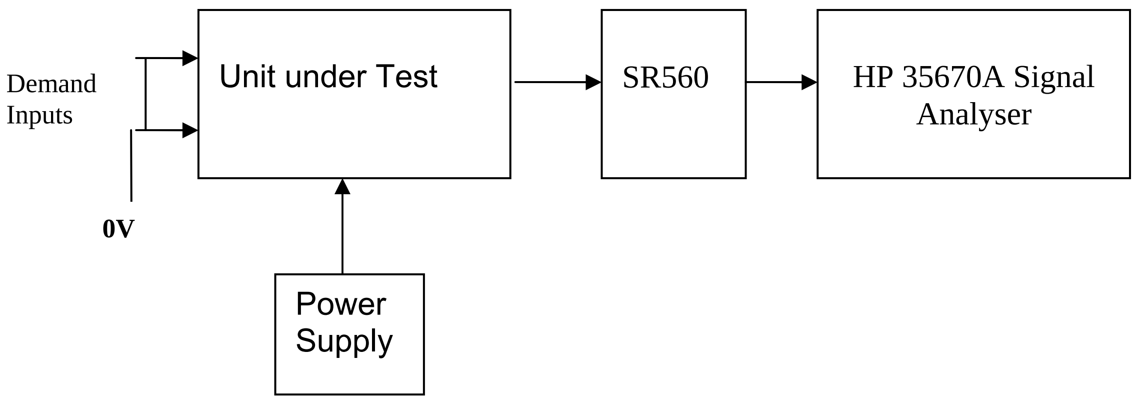
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	43.6	√
CH1 Negative			CH1 IC5	46.2	√
CH2 Positive	24.38	√	CH2 IC1	45.5	√
CH2 Negative			CH2 IC5	48.4	√
CH3 Positive	24.38	√	CH3 IC1	45.7	√
CH3 Negative			CH3 IC5	45.5	√
CH4 Positive	24.39	√	CH4 IC1	43.1	√
CH4 Negative			CH4 IC5	45.7	√

Unit……………..Q_TOP_P35…………………..Serial No ……………………………..
Test Engineer…..Xen…….…………….
Date……………..14/6/10……………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-101.5	-161.5
Ch2	-161.15dB	-100.2	-160.2
Ch3	-161.15dB	-100.0	-160.0
Ch4	-161.15dB	-100.7	-160.7

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………….Q_TOP_P35……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..23/410………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………..QTOP35P……………..Serial No ………………………………
Test Engineer ………RMC
Date …………………30/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP35P
Driver board ID	QTOP35P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP35P
Monitor board ID	MON90
Monitor board Drawing No/Issue No	D070480_4_k
Monitor board Serial Number	MON90

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit……………….Q_TOP_P36…………………….Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10……………..

Drive Card ID……Q_TOP36P………
Monitor Card ID…Mon71…….…….

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

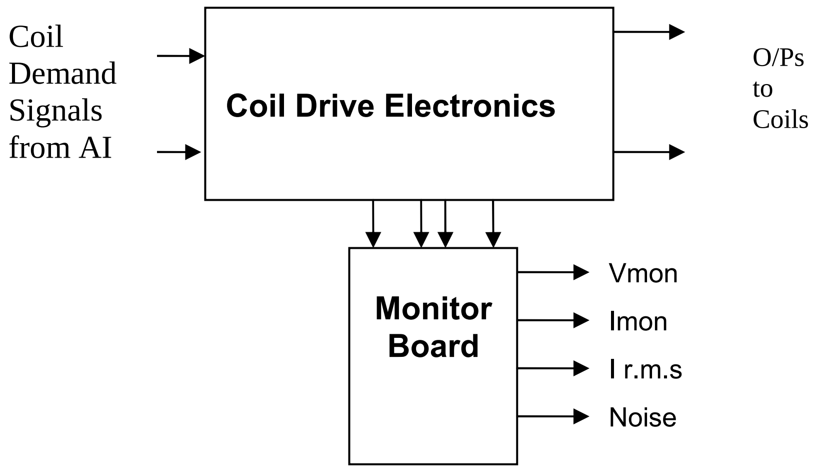


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..13/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

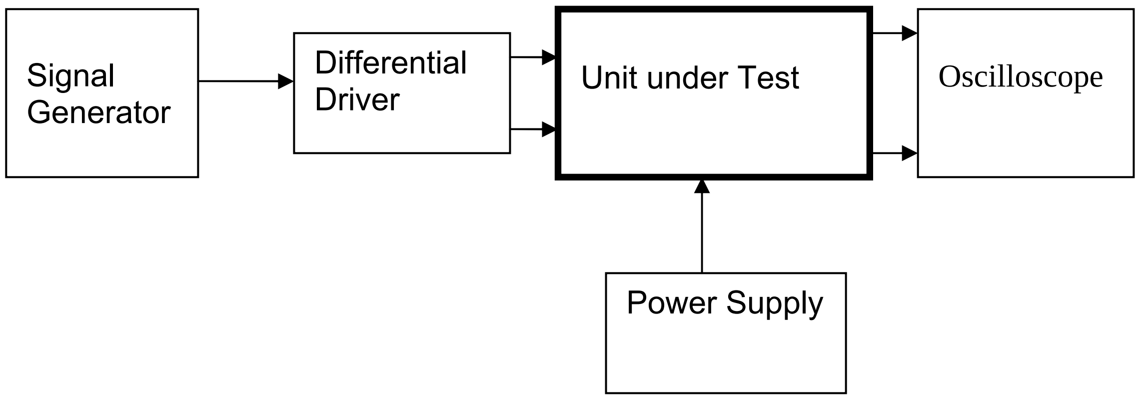
Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..13/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..13/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c..

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.011	√
2	Pin 5	Current Monitor	1v r.m.s	1.014	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.019	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.018	√

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.31	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.31	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.25	2.9μV√Hz	√
2		1.59	2.9μV√Hz	√
3		1.66	2.9μV√Hz	√
4		2.4	2.9μV√Hz	√

Unit……………..Q_TOP_P36…………………..Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.8		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..13/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	**CH1 IC1**	43.6	√
CH1 Negative			**CH1 IC5**	42.3	√
CH2 Positive	24.36	√	**CH2 IC1**	41.1	√
CH2 Negative			**CH2 IC5**	40.6	√
CH3 Positive	24.36	√	**CH3 IC1**	44.5	√
CH3 Negative			**CH3 IC5**	42.8	√
CH4 Positive	24.36	√	**CH4 IC1**	39.7	√
CH4 Negative			**CH4 IC5**	40.4	√

Unit……………..Q_TOP_P36…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.

Replace the lid of the box, and replace screws.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode

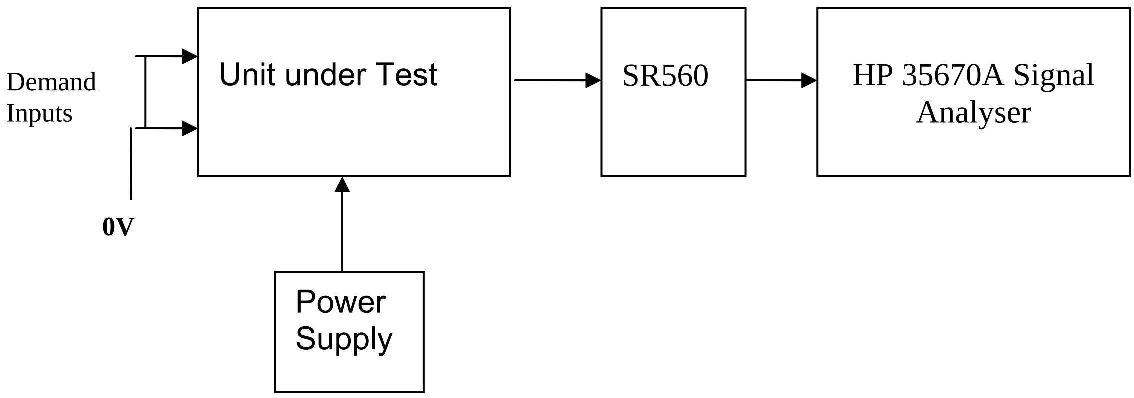
Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.

Switch the filters in.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.6	-159.6
Ch2	-161.15dB	-99.6	-159.6
Ch3	-161.15dB	-102.1	-162.1
Ch4	-161.15dB	-98.3	-158.3

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P36……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………………QTOP36P………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP46P
Driver board ID	QTOP46P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP46P
Monitor board ID	MON71
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON71

10. Check the security of any modification wires.

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..13/4/10……………..

Drive Card ID……Q_TOP37P………
Monitor Card ID…Mon72…….…….…..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

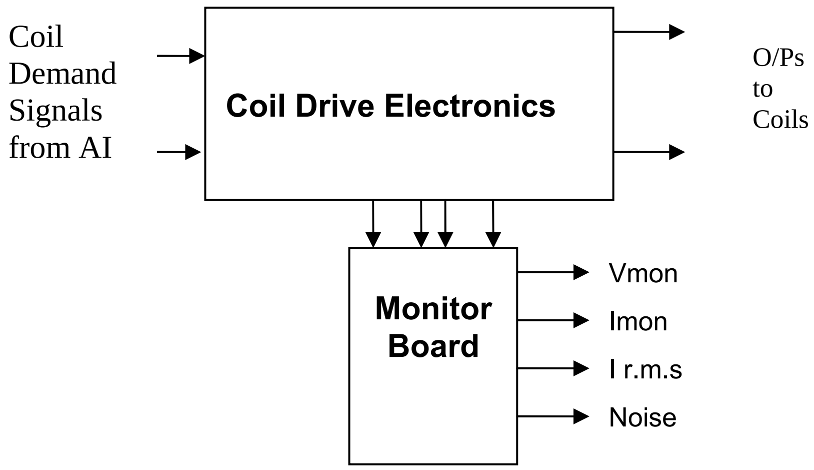


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..13/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..13/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………….Q_TOP_P37…………………….Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..13/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

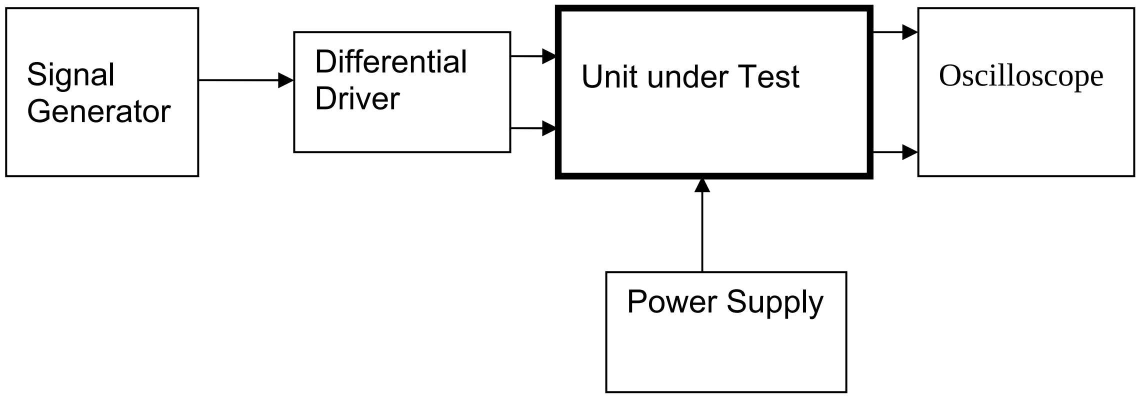
Unit………………Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..13/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen……..………….
Date……………..13/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..13/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.015	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.022	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.020	√

Unit……………….Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/5/10……………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.32	2.9μV√Hz	√
2		2.0	2.9μV√Hz	√
3		1.5	2.9μV√Hz	√
4		1.5	2.9μV√Hz	√

Unit……………..Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..13/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P37……………………Serial No ……………………………
Test Engineer…..Xen…….…………..
Date……………..13/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.40	√	**CH1 IC1**	40.4	√
CH1 Negative			**CH1 IC5**	40.4	√
CH2 Positive	24.40	√	**CH2 IC1**	41.6	√
CH2 Negative			**CH2 IC5**	41.6	√
CH3 Positive	24.40	√	**CH3 IC1**	41.4	√
CH3 Negative			**CH3 IC5**	42.3	√
CH4 Positive	24.40	√	**CH4 IC1**	40.6	√
CH4 Negative			**CH4 IC5**	40.4	√

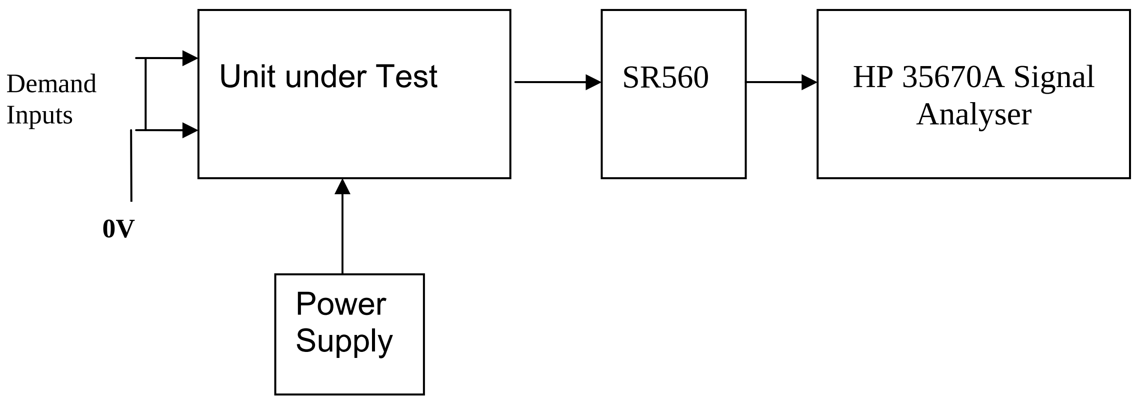
Unit……………..Q_TOP_P37…………………..Serial No ……………………………
Test Engineer…..Xen…….…………….
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-100	-160
Ch2	-161.15dB	-100	-160
Ch3	-161.15dB	-100	-160
Ch4	-161.15dB	-101	-161

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P37……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..13/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………..QTOP37P………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP37P
Driver board ID	QTOP37P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP37P
Monitor board ID	D070480-04-K
Monitor board Drawing No/Issue No	MON72P
Monitor board Serial Number	MON72P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

Drive Card ID…….Q_TOP38P………
Monitor Card ID …Mon74……..……..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

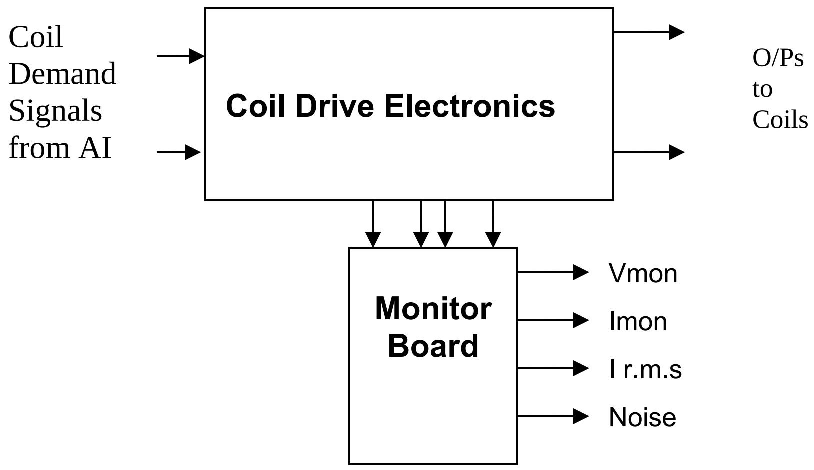


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P38…………………….Serial No ……………………………….
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit.................Q_TOP_P38......................Serial No ....
Test Engineer.....Xen.....................
Date................14/4/10.................

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	**SIGNAL**	**DESCRIPTION**	**Pd in from Sat**	**OK?**
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	**SIGNAL**	**Monitors:**	**In from Sat**	**OK?**
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	**SIGNAL**	**DESCRIPTION**	**DC in Connector**	**OK?**
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

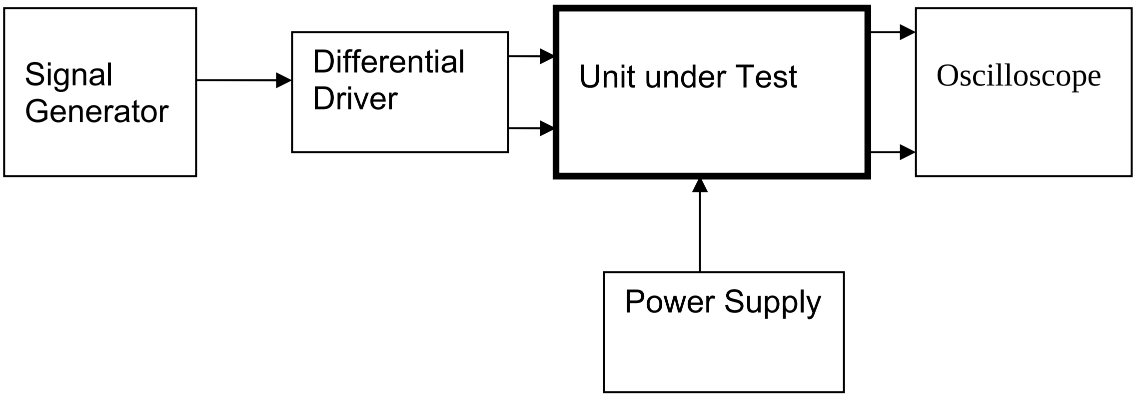
Unit……………….Q_TOP_P38…………………….Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit.................Q_TOP_P38.......................Serial No ....
Test Engineer.....Xen.......................
Date.................14/4/10.................

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..14/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.015	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.016	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.017	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.017	√

Unit……………..Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/5/10……………….

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.5	2.9μV√Hz	√
2		1.3	2.9μV√Hz	√
3		1.0	2.9μV√Hz	√
4		1.75	2.9μV√Hz	√

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

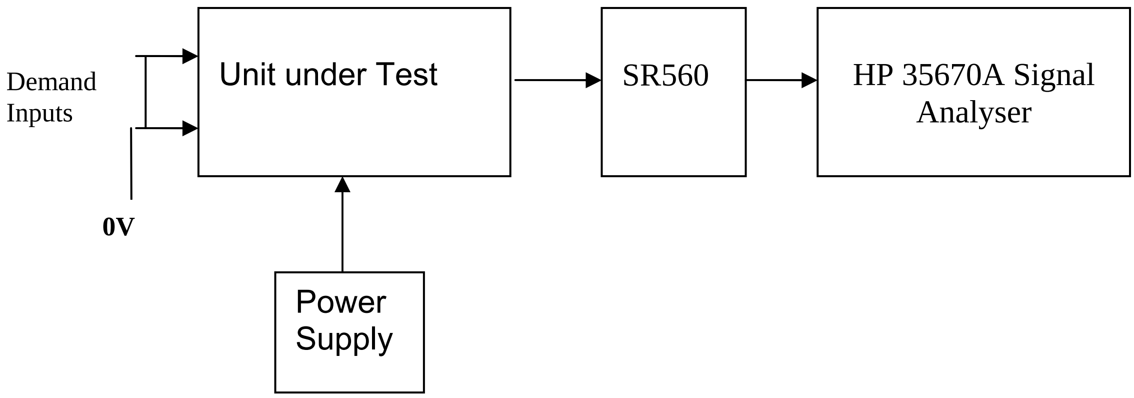
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	40.1	√
CH1 Negative			CH1 IC5	43.8	√
CH2 Positive	24.38	√	CH2 IC1	43.1	√
CH2 Negative			CH2 IC5	44.8	√
CH3 Positive	24.38	√	CH3 IC1	42.3	√
CH3 Negative			CH3 IC5	44.8	√
CH4 Positive	24.38	√	CH4 IC1	41.6	√
CH4 Negative			CH4 IC5	47.2	√

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 KHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB	-99.3	-159.3
Ch2	-161.15dB	-102	-162
Ch3	-161.15dB	-102	-162
Ch4	-161.15dB	-99.7	-159.7

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P38……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..14/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.55	141.2mA	>200mA	>141.4mA	√
2	39.4	5.55	140.9mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.57	141.4mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit………………QTOP38P……………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP38P
Driver board ID	QTOP38P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP38P
Monitor board ID	MON74
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON47P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….………………
Date……………..14/4/10……………….

Drive Card ID……..Q_TOP39P………
Monitor Card ID ….Mon73……..……..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

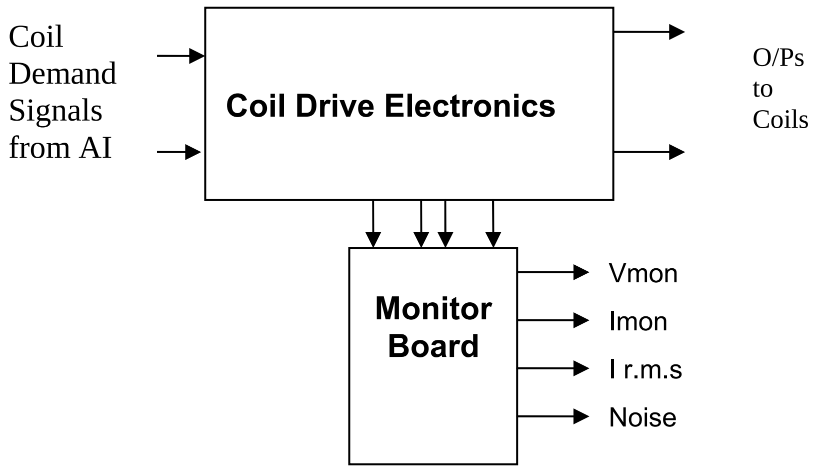


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..14/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P39…………………….Serial No ……………………………….
Test Engineer…..Xen……..…………
Date……………..14/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

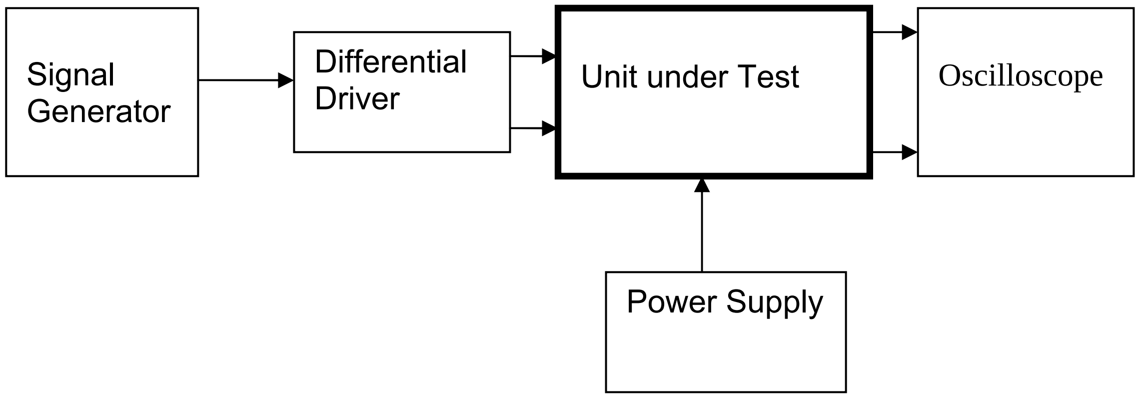
Unit……………….Q_TOP_P39…………………….Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..14/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..14/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.014	√
3	Pin 8	Current Monitor	1v r.m.s	1.012	√
	Pin 7	RMS Current	1v dc	1.015	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.018	√

Unit………………Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.6	2.9μV√Hz	√
2		1.3	2.9μV√Hz	√
3		1.0	2.9μV√Hz	√
4		0.8	2.9μV√Hz	√

Unit……………..Q_TOP_P39…………………..Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..14/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P39…………………….Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

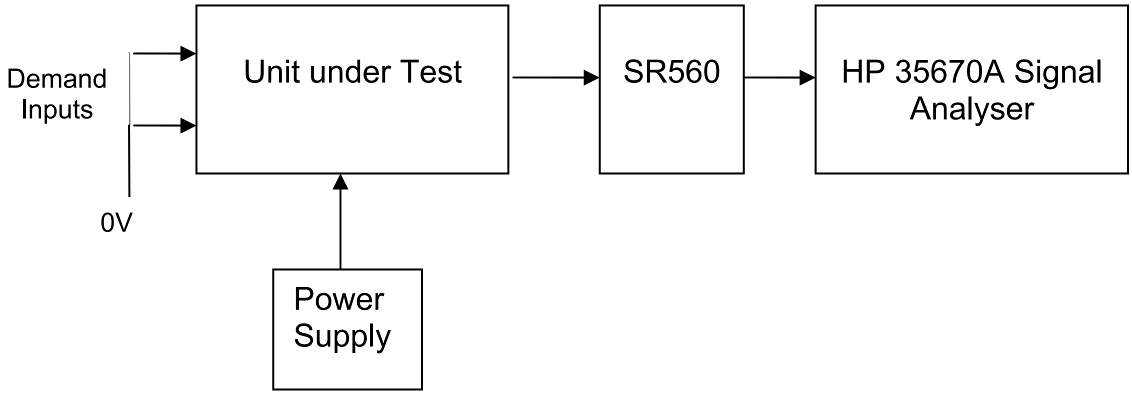
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.38	√	CH1 IC1	41.4	√
CH1 Negative			CH1 IC5	43.1	√
CH2 Positive	24.37	√	CH2 IC1	44.3	√
CH2 Negative			CH2 IC5	47.2	√
CH3 Positive	24.37	√	CH3 IC1	42.8	√
CH3 Negative			CH3 IC5	44.0	√
CH4 Positive	24.37	√	CH4 IC1	44.3	√
CH4 Negative			CH4 IC5	44.8	√

Unit……………….Q_TOP_P39…………………….Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-99	-159
Ch2	-161.15dB	-99	-159
Ch3	-161.15dB	-101	-162
Ch4	-161.15dB	-103	-163

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………..Q_TOP_P39……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.57	141.7mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP39P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………26/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP39P
Driver board ID	QTOP39P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP39P
Monitor board ID	MON73
Monitor board Drawing No/Issue No	D070480-04-K
Monitor board Serial Number	MON73

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10……………….

Drive Card ID……Q_TOP40P………
Monitor Card ID…Mon76…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

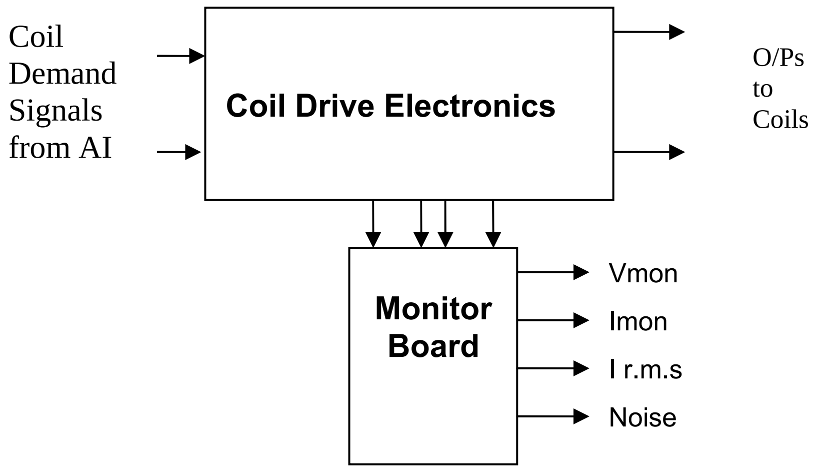


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..14/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

IC8 and IC4 have been replaced by the AD8671 op-amp on CHs 2 & 3.

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

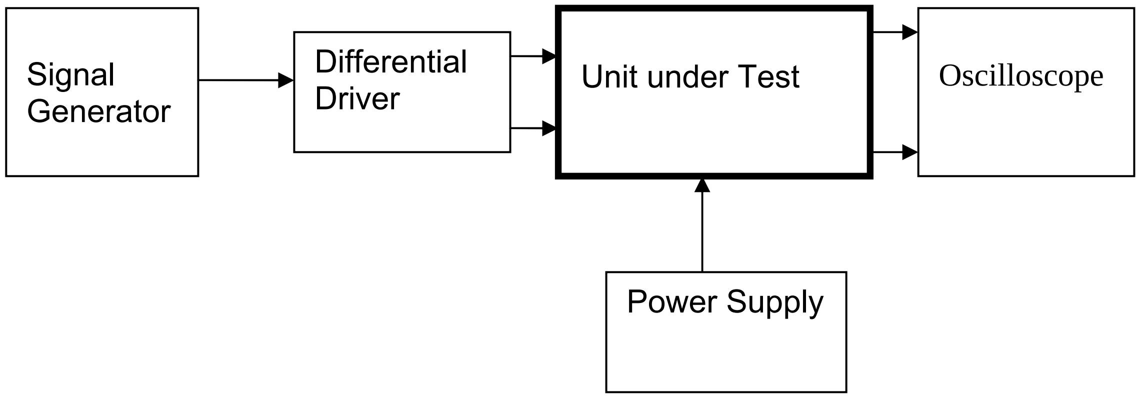
Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen……..……………
Date……………..14/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.021	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit……………..Q_TOP_P40…………………..Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..14/4/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.13	2.9μV√Hz	√
2		1.14	2.9μV√Hz	√
3		1.53	2.9μV√Hz	√
4		1.64	2.9μV√Hz	√

Unit……………..Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	**CH1 IC1**	45.7	√
CH1 Negative			**CH1 IC5**	46.5	√
CH2 Positive	24.37	√	**CH2 IC1**	45.5	√
CH2 Negative			**CH2 IC5**	45.0	√
CH3 Positive	24.37	√	**CH3 IC1**	47.9	√
CH3 Negative			**CH3 IC5**	48.9	√
CH4 Positive	24.37	√	**CH4 IC1**	44.5	√
CH4 Negative			**CH4 IC5**	47.4	√

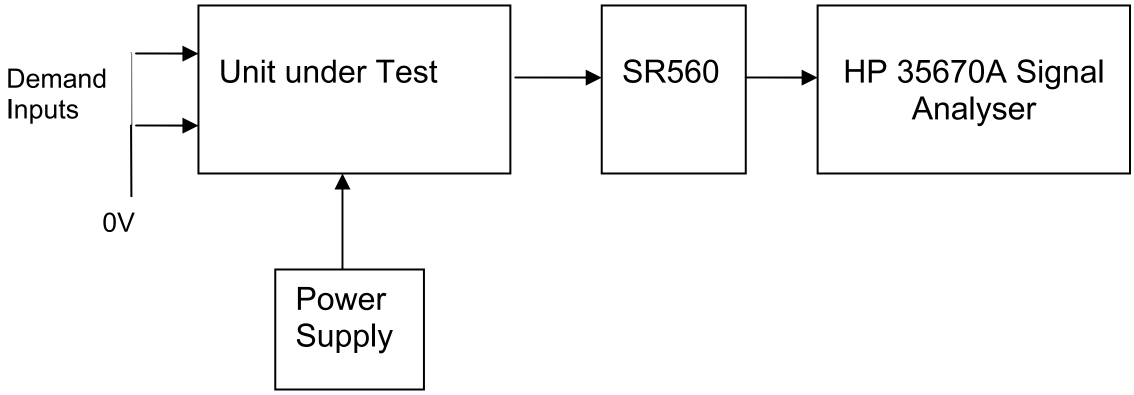
Unit……………..Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..14/6/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100.6	-160.6
Ch2	-161.15dB	-101.7	-161.7
Ch3	-161.15dB	-102.9	-162.9
Ch4	-161.15dB	-99.5	-159.5

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P40……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.56	141.1mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.55	140.9mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP40P..........................Serial No ....
Test Engineer ....RMC
Date 30/6/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP40P
Driver board ID	QTOP40P
Driver board Drawing No/Issue No	D0902747_V9
Driver board Serial Number	QTOP40P
Monitor board ID	MON 76
Monitor board Drawing No/Issue No	D070480_4_k
Monitor board Serial Number	MON 76

10. Check the security of any modification wires. √

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

Drive Card ID……Q_TOP41P………
Monitor Card ID…Mon77…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

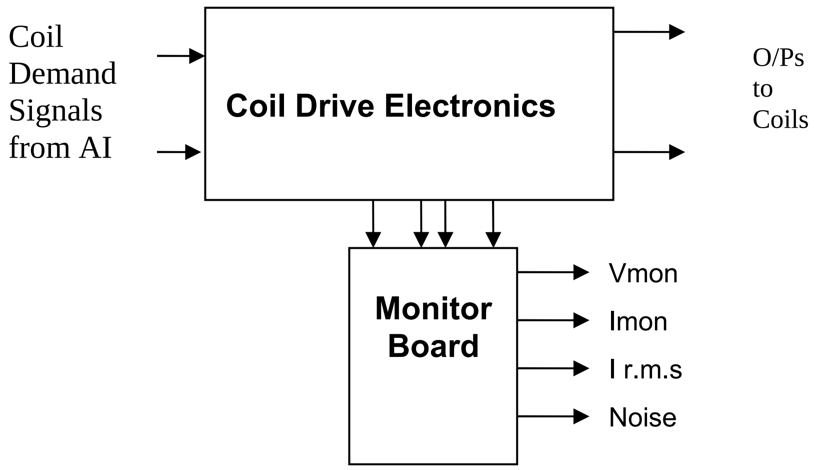


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..Q_TOP_P41…………………..Serial No ……………………………
Test Engineer…..Xen…………………
Date……………..14/4/10……………..

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

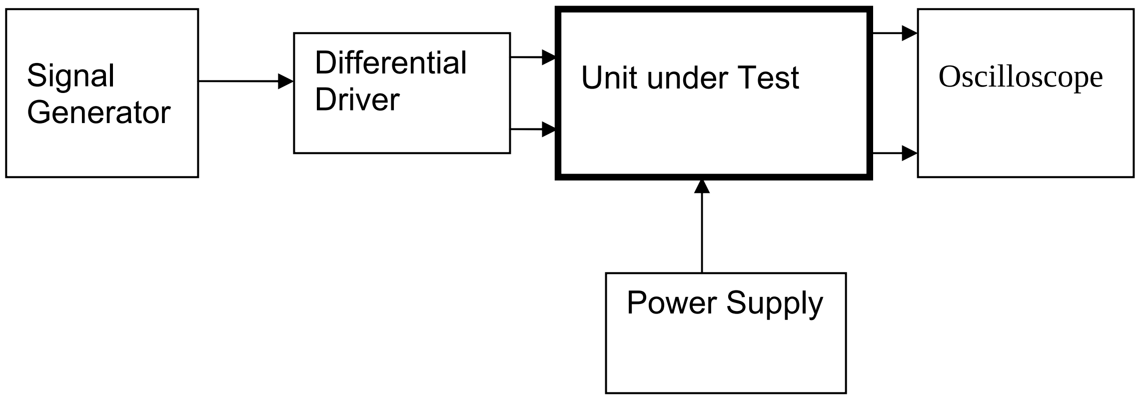
Unit……………….Q_TOP_P41…………………….Serial No ……………………………….
Test Engineer…..Xen…….……………
Date……………..14/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..14/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..14/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..14/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.013	√
	Pin 1	RMS Current	1v dc	1.016	√
2	Pin 5	Current Monitor	1v r.m.s	1.012	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.011	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.012	√

Unit………………Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.9	2.9μV√Hz	√
2		1.6	2.9μV√Hz	√
3		1.4	2.9μV√Hz	√
4		1.6	2.9μV√Hz	√

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..14/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.0		
10Hz	-30.5		
100Hz	-42.9		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	0.9		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.2		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.82		
Ch2	4.82		
Ch3	4.82		
Ch4	4.82		

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10……………..

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

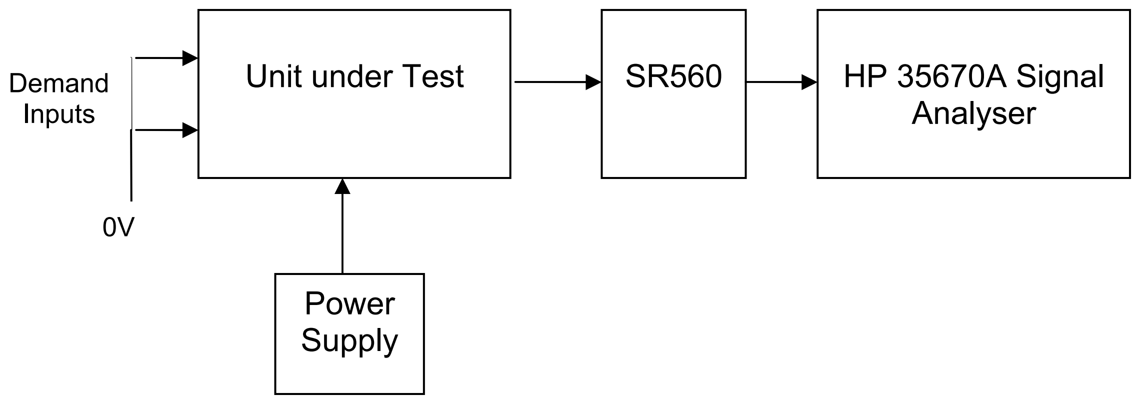
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	CH1 IC1	37.7	√
CH1 Negative			CH1 IC5	42.8	√
CH2 Positive	24.36	√	CH2 IC1	41.6	√
CH2 Negative			CH2 IC5	43.3	√
CH3 Positive	24.37	√	CH3 IC1	41.1	√
CH3 Negative			CH3 IC5	43.3	√
CH4 Positive	24.37	√	CH4 IC1	40.6	√
CH4 Negative			CH4 IC5	41.6	√

Unit……………..Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-101	-161
Ch2	-161.15dB	-100	-160
Ch3	-161.15dB	-101	-161
Ch4	-161.15dB	-98	-158

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P41……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.59	141.9mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit...............QTOP41P...............Serial No ....
Test Engineer ....RMC
Date 27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP41P
Driver board ID	QTOP41P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP41P
Monitor board ID	MON77
Monitor board Drawing No/Issue No	D070480-4-K
Monitor board Serial Number	MON77

10. Check the security of any modification wires.

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10……………..

Drive Card ID……Q_TOP42P………
Monitor Card ID…Mon79…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

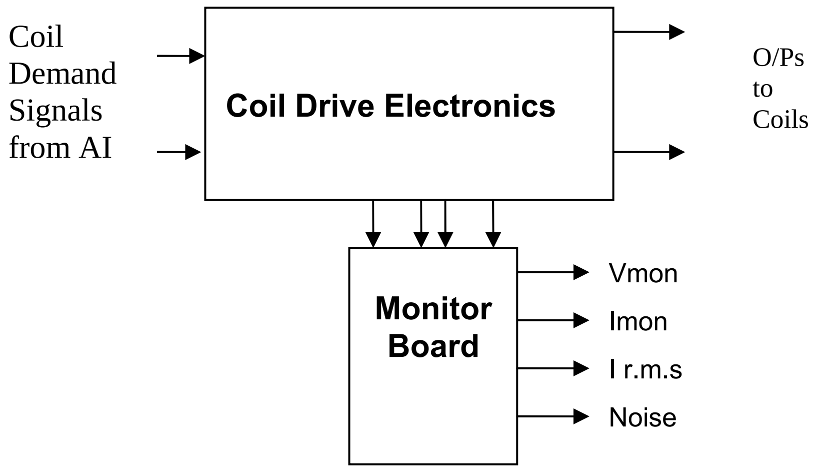


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P42…………………….Serial No ……………………………….
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

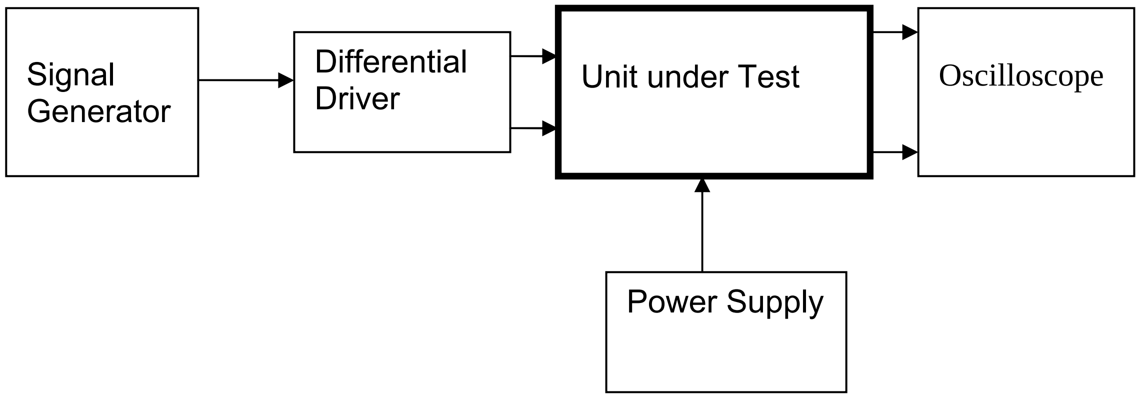
Unit……………….Q_TOP_P42…………………….Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	**Indicator**		**OK?**
	ON	**OFF**	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.016	√
	Pin 1	RMS Current	1v dc	1.013	√
2	Pin 5	Current Monitor	1v r.m.s	1.016	√
	Pin 4	RMS Current	1v dc	1.022	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.020	√
4	Pin 11	Current Monitor	1v r.m.s	1.014	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit………………Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.9	2.9μV√Hz	√
2		1.0	2.9μV√Hz	√
3		1.9	2.9μV√Hz	√
4		1.0	2.9μV√Hz	√

Unit……………..Q_TOP_P42…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..15/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.5		
10Hz	-29.9		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………..Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.39	√	**CH1 IC1**	42.3	√
CH1 Negative			**CH1 IC5**	43.1	√
CH2 Positive	24.39	√	**CH2 IC1**	44.8	√
CH2 Negative			**CH2 IC5**	45.0	√
CH3 Positive	24.40	√	**CH3 IC1**	41.6	√
CH3 Negative			**CH3 IC5**	43.3	√
CH4 Positive	24.39	√	**CH4 IC1**	39.7	√
CH4 Negative			**CH4 IC5**	42.3	√

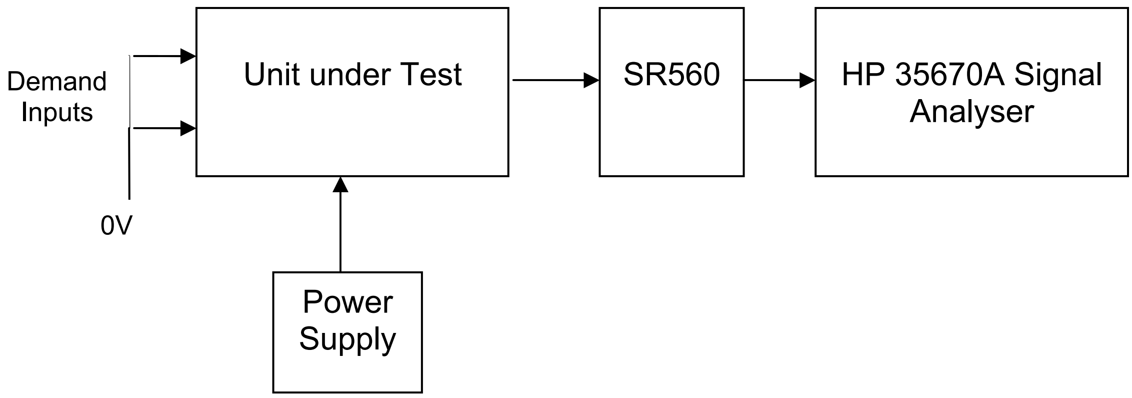
Unit………………Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-101.6	-161.6
Ch2	-161.15dB	-101	-161
Ch3	-161.15dB	-101	-161
Ch4	-161.15dB	-101	-161

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz. The noise floor is about -133dB.

Unit……………...Q_TOP_P42……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	R =	V=	Therefore I =	Spec (peak)	Spec (r.m.s)	Pass?
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.57	141.7mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit..............QTOP42P..............Serial No ....
Test Engineer ....RMC
Date 27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated.

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP42P
Driver board ID	QTOP42P
Driver board Drawing No/Issue No	DO902747-V7
Driver board Serial Number	QTOP42P
Monitor board ID	MON79
Monitor board Drawing No/Issue No	D070480-04-K
Monitor board Serial Number	MON79

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

Drive Card ID……Q_TOP43P………
Monitor Card ID…Mon78…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

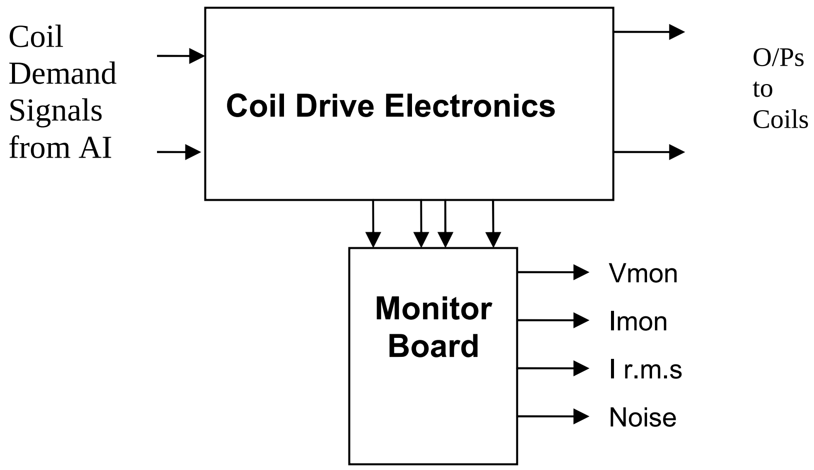


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

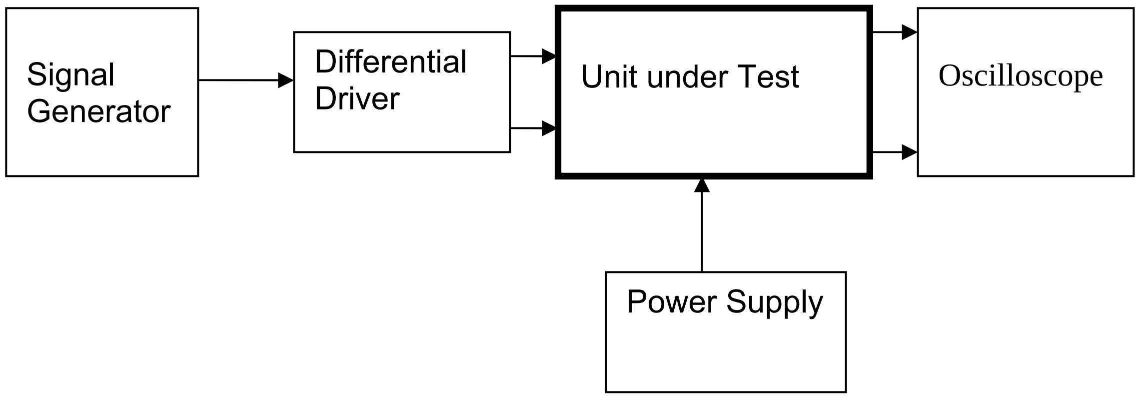
Unit……………..Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….………….
Date……………..15/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………….Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P43…………………..Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………… Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.019	√
2	Pin 5	Current Monitor	1v r.m.s	1.015	√
	Pin 4	RMS Current	1v dc	1.018	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.013	√

Unit……………..Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.5	2.9μV√Hz	√
2		1.3	2.9μV√Hz	√
3		1.1	2.9μV√Hz	√
4		1.67	2.9μV√Hz	√

Unit………………Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.6		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.2		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit……………….Q_TOP_P43…………………….Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..15/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

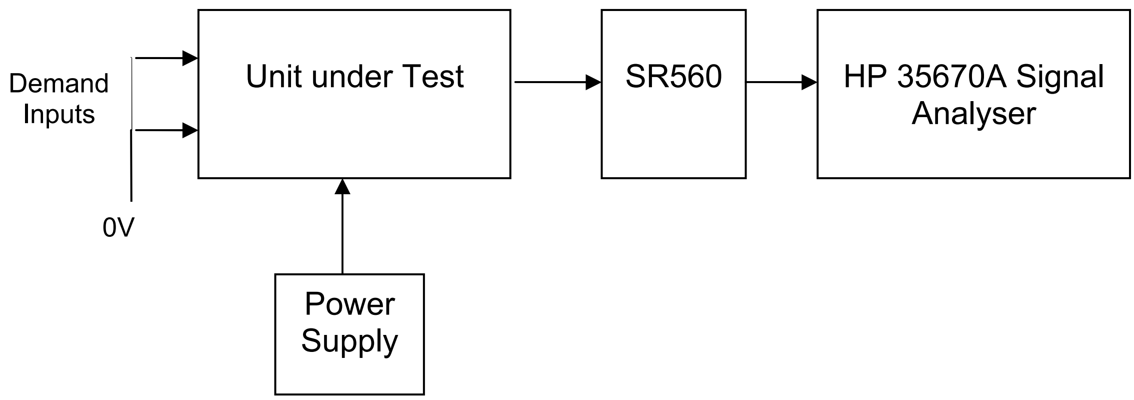
The output voltages should be recorded.

Output	Voltage	> 24v?	DRIVER	Temperature	<60°C?
CH1 Positive	24.36	√	**CH1 IC1**	41.8	√
CH1 Negative			**CH1 IC5**	47.4	√
CH2 Positive	24.37	√	**CH2 IC1**	43.8	√
CH2 Negative			**CH2 IC5**	43.1	√
CH3 Positive	24.36	√	**CH3 IC1**	43.6	√
CH3 Negative			**CH3 IC5**	43.1	√
CH4 Positive	24.36	√	**CH4 IC1**	41.4	√
CH4 Negative			**CH4 IC5**	43.3	√

Unit…………….…Q_TOP_P43……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-102	-162
Ch2	-161.15dB	-99.7	-159.7
Ch3	-161.15dB	-98.2	-158.2
Ch4	-161.15dB	-101.1	-161.1

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P43…………………..Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10……………..

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.58	141.6mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.57	141.4mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit.................QTOP43P.................Serial No ....
Test Engineer ....RMC
Date 27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP43P
Driver board ID	QTOP43P
Driver board Drawing No/Issue No	D0903747 V7
Driver board Serial Number	QTOP43P
Monitor board ID	MON78
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON78

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

Drive Card ID……Q_TOP44P………
Monitor Card ID…Mon80…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

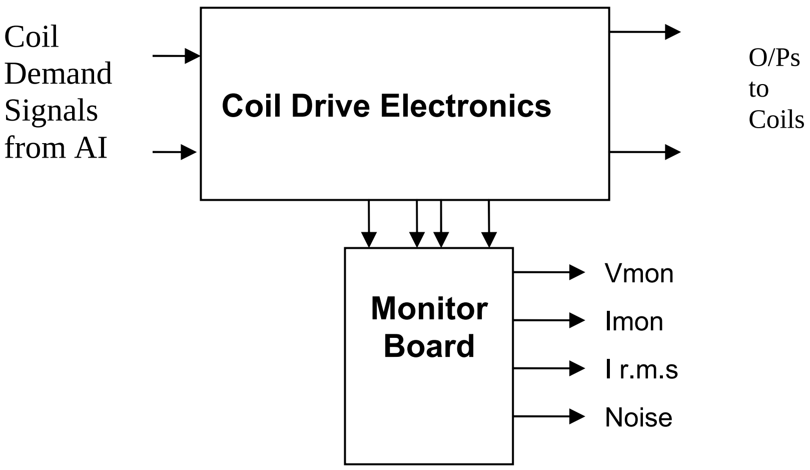


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit……………..Q_TOP_P44…………………..Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..15/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

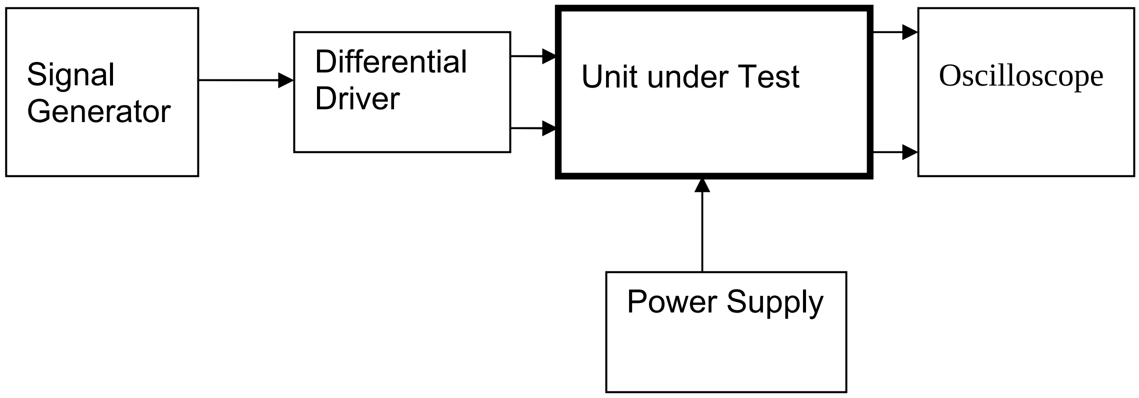
Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen……..…………..
Date……………..15/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.018	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.017	√
3	Pin 8	Current Monitor	1v r.m.s	1.014	√
	Pin 7	RMS Current	1v dc	1.016	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.015	√

Unit……………..Q_TOP_P44…………………..Serial No ……………………………
Test Engineer…..Xen…….……………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1		1.0	2.9μV√Hz	√
2		2.1	2.9μV√Hz	√
3		1.5	2.9μV√Hz	√
4		1.2	2.9μV√Hz	√

Unit……………..Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..15/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13.
Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.4		
10Hz	-30.0		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

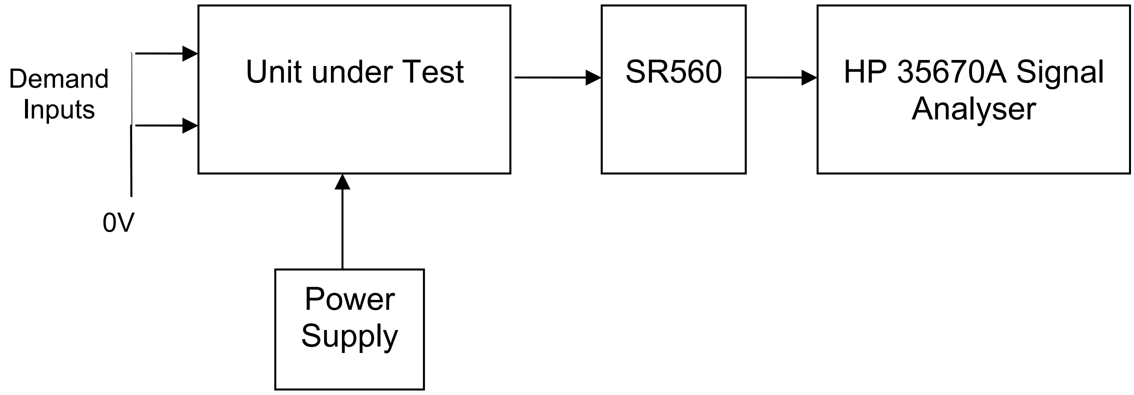
The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.37	√	**CH1 IC1**	45.3	√
CH1 Negative			**CH1 IC5**	43.6	√
CH2 Positive	24.37	√	**CH2 IC1**	41.4	√
CH2 Negative			**CH2 IC5**	43.3	√
CH3 Positive	24.37	√	**CH3 IC1**	41.4	√
CH3 Negative			**CH3 IC5**	45.7	√
CH4 Positive	24.37	√	**CH4 IC1**	40.6	√
CH4 Negative			**CH4 IC5**	42.8	√

Unit……………..Q_TOP_P44…………………..Serial No ……………………………
Test Engineer…..Xen…….…………….
Date……………..15/4/10……………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-98.5	-158.5
Ch2	-161.15dB	-102	-162
Ch3	-161.15dB	-100	-160
Ch4	-161.15dB	-99	-159

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz. The noise floor is about -133dB.

Unit………………Q_TOP_P44……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..15/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.56	141.5mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.57	141.4mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………………QTOP44P…………………Serial No ………………………………
Test Engineer ………RMC
Date …………………26/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP44P
Driver board ID	QTOP44P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP44P
Monitor board ID	MON80P
Monitor board Drawing No/Issue No	D07480-4-K
Monitor board Serial Number	MON80P

10. Check the security of any modification wires.

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

    Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

Drive Card ID……Q_TOP45P………
Monitor Card ID…Mon81…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

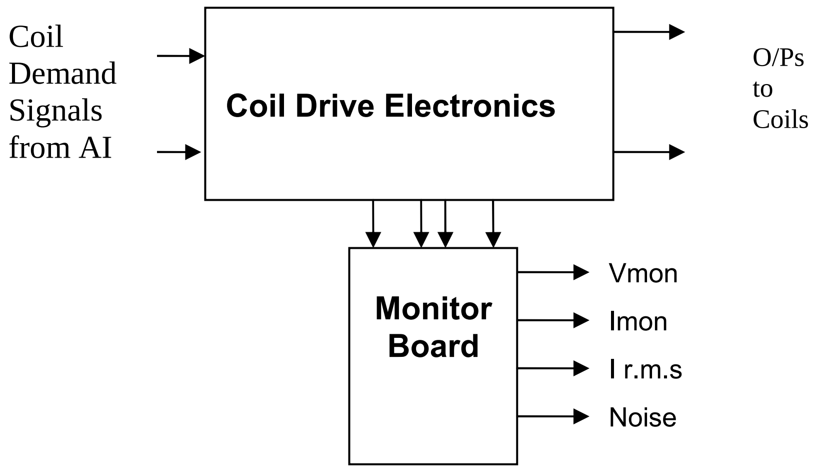


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..16/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………….Q_TOP_P45…………………….Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

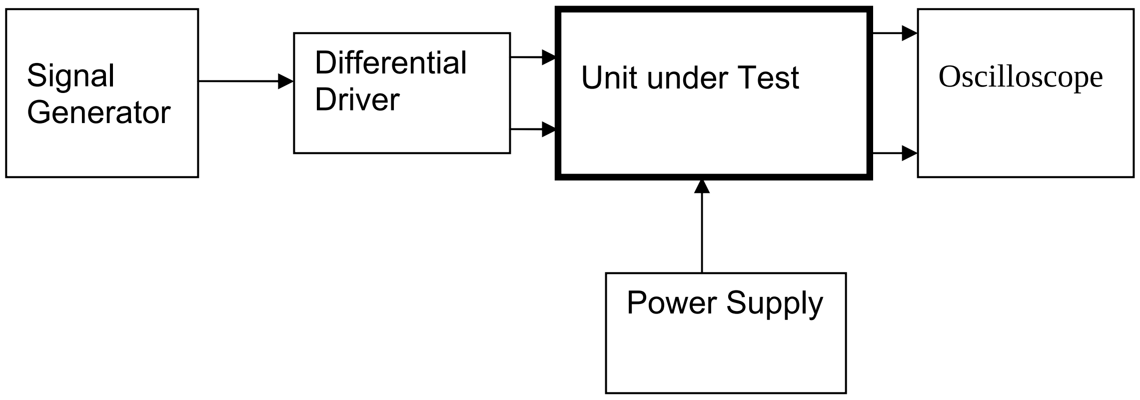
Unit……………….Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.012	√
	Pin 1	RMS Current	1v dc	1.011	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.021	√
3	Pin 8	Current Monitor	1v r.m.s	1.013	√
	Pin 7	RMS Current	1v dc	1.014	√
4	Pin 11	Current Monitor	1v r.m.s	1.012	√
	Pin 10	RMS Current	1v dc	1.020	√

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..25/5/10……………..

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.37	2.9μV√Hz	√
2		2.1	2.9μV√Hz	√
3		1.76	2.9μV√Hz	√
4		1.4	2.9μV√Hz	√

Unit……………….Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.9		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.2		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..16/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.37	√	**CH1 IC1**	41.1	√
CH1 Negative			**CH1 IC5**	43.1	√
CH2 Positive	24.37	√	**CH2 IC1**	42.8	√
CH2 Negative			**CH2 IC5**	43.8	√
CH3 Positive	24.37	√	**CH3 IC1**	42.6	√
CH3 Negative			**CH3 IC5**	44.0	√
CH4 Positive	24.37	√	**CH4 IC1**	41.6	√
CH4 Negative			**CH4 IC5**	43.6	√

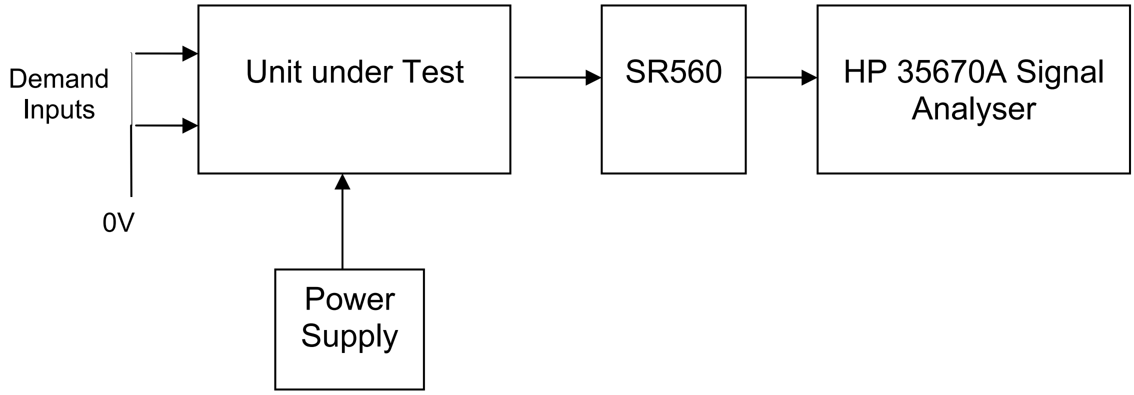
Unit……………..Q_TOP_P45…………………..Serial No ……………………………
Test Engineer…..Xen…….…………….
Date……………..25/5/10………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-101	-161
Ch2	-161.15dB	-100	-160
Ch3	-161.15dB	-99	-159
Ch4	-161.15dB	-101	-161

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit……………..Q_TOP_P45……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..16/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.57	141.4mA	>200mA	>141.4mA	√
3	39.3	5.56	141.5mA	>200mA	>141.4mA	√
4	39.4	5.57	141.4mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………QTOP45P…………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections. √

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	QTOP45P
Driver board ID	QTOP45P
Driver board Drawing No/Issue No	D0902747 V7
Driver board Serial Number	QTOP45P
Monitor board ID	MON81
Monitor board Drawing No/Issue No	D070480-04-K
Monitor board Serial Number	MON81

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

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of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/4/10………………

Drive Card ID……Q_TOP46P………
Monitor Card ID…Mon83…...………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

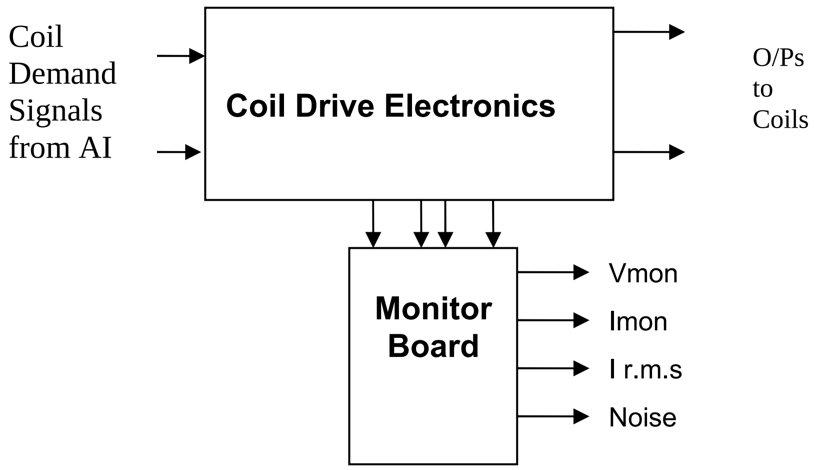


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77III	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/4/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V	√		
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V	√		
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

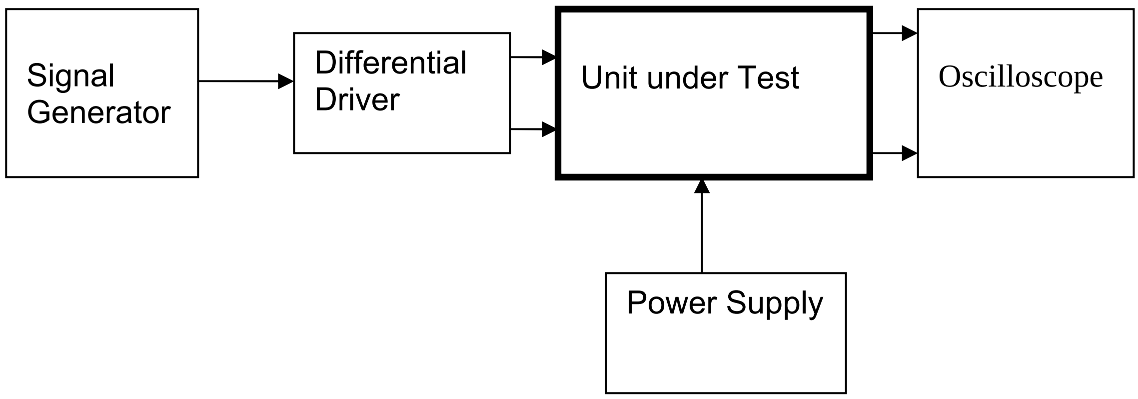
Unit……………..Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………..Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
600mA	500mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………..Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen……..…………
Date……………..16/4/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen………………….
Date……………..16/4/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s	1.014	√
	Pin 1	RMS Current	1v dc	1.020	√
2	Pin 5	Current Monitor	1v r.m.s	1.013	√
	Pin 4	RMS Current	1v dc	1.015	√
3	Pin 8	Current Monitor	1v r.m.s	1.015	√
	Pin 7	RMS Current	1v dc	1.018	√
4	Pin 11	Current Monitor	1v r.m.s	1.013	√
	Pin 10	RMS Current	1v dc	1.016	√

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…………………
Date……………..25/5/10………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3	3.32	3.2v to 3.4v	√
2	Pins 3,11	Pin 6	3.32	3.2v to 3.4v	√
3	Pins 5,13	Pin 9	3.32	3.2v to 3.4v	√
4	Pins 7, 15	Pin 12	3.32	3.2v to 3.4v	√

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.45	2.9μV√Hz	√
2		1.1	2.9μV√Hz	√
3		2.39	2.9μV√Hz	√
4		1.1	2.9μV√Hz	√

Unit……………..Q_TOP_P46…………………..Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10……………..

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.1		
10Hz	-30.4		
100Hz	-42.8		
1kHz	-43.3		

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.3		
10Hz	-30.1		
100Hz	-42.8		
1kHz	-43.3		

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz	1.2		
10Hz	-30.3		
100Hz	-42.8		
1kHz	-43.3		

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1	4.85		
Ch2	4.85		
Ch3	4.85		
Ch4	4.85		

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….…………….
Date……………..16/4/10………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	√
Ch2	√
Ch3	√
Ch4	√

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive	24.35	√	**CH1 IC1**	43.3	√
CH1 Negative			**CH1 IC5**	44.8	√
CH2 Positive	24.35	√	**CH2 IC1**	43.1	√
CH2 Negative			**CH2 IC5**	44.3	√
CH3 Positive	24.35	√	**CH3 IC1**	44.5	√
CH3 Negative			**CH3 IC5**	46.5	√
CH4 Positive	24.36	√	**CH4 IC1**	42.6	√
CH4 Negative			**CH4 IC5**	43.3	√

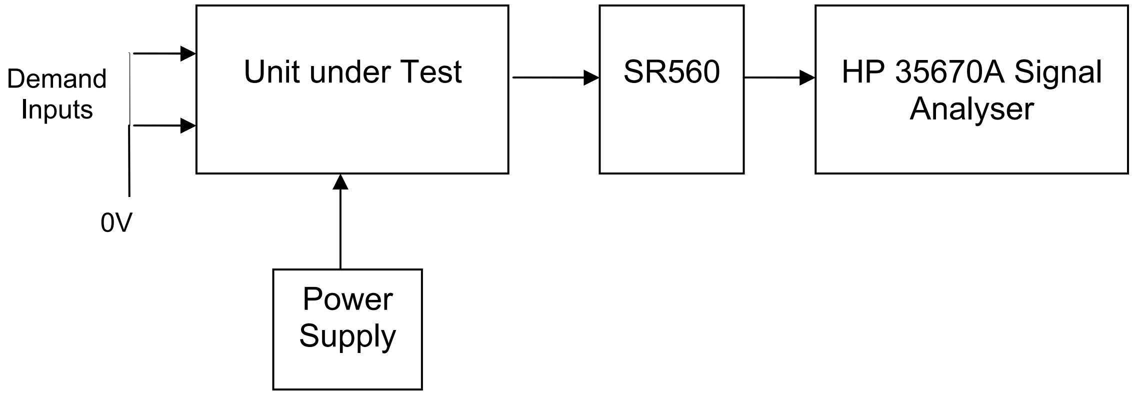
Unit……………..Q_TOP_P46…………………..Serial No ……………………………
Test Engineer…..Xen…...………………
Date……………..25/5/10……………..

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode

Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =
Ch1	-161.15dB	-100	-160
Ch2	-161.15dB	-101	-161
Ch3	-161.15dB	-98.9	-158.9
Ch4	-161.15dB	-100	-160

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.The noise floor is about -133dB.

Unit………………Q_TOP_P46……………………Serial No ………………………………
Test Engineer…..Xen…….……………
Date……………..16/4/10………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3	5.57	141.7mA	>200mA	>141.4mA	√
2	39.4	5.59	141.9mA	>200mA	>141.4mA	√
3	39.3	5.55	141.2mA	>200mA	>141.4mA	√
4	39.4	5.56	141.1mA	>200mA	>141.4mA	√

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit…………QTOP46P…………………………Serial No ………………………………
Test Engineer ………RMC
Date …………………27/5/10

15. Final Assembly Checks

1. Remove the lid of the box. √

2. Unplug all external connections.

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. √

4. Check that all internal connectors are firmly mated. √

5. Tighten the screw-locks holding all the external connectors. √

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. √

7. Check that all the LEDs are nicely centred. √

8. Check that links W4 and W5 are in place. √

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below: √

UoB box ID	QTOP46P
Driver board ID	QTOP46P
Driver board Drawing No/Issue No	D0902747-V7
Driver board Serial Number	QTOP46P
Monitor board ID	MON83
Monitor board Drawing No/Issue No	D070480-04-K
Monitor board Serial Number	MON83P

10. Check the security of any modification wires.

11. Visually inspect. √

12. Put the lid on and fasten all screws, √

Check all external screws for tightness. √

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900230-V2 Advanced LIGO UK 30 November 2009

Quad TOP Coil Drive Unit Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document:
Inform aligo_sus

This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html
http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP DRIVER
COMPLETED UNIT TEST PLAN

Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…….……………
Date……………..1/7/10………………

Drive Card ID……Q_TOP4P………
Monitor Card ID…Mon174…..………..

Contents

1. Description

The TOP Driver Unit will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the TOP mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One TOP unit controls four OSEMs.

The TOP Coil Drive Unit contains a Coil Drive board and a Monitor board. The Monitor Board monitors the Output voltage, Output Current, RMS Current and Output Noise from the unit.

The TOP Driver Unit also passes the amplified signals from the Photodiodes, which detect the position of the TOP mirror, back to the control electronics without processing them in any way.

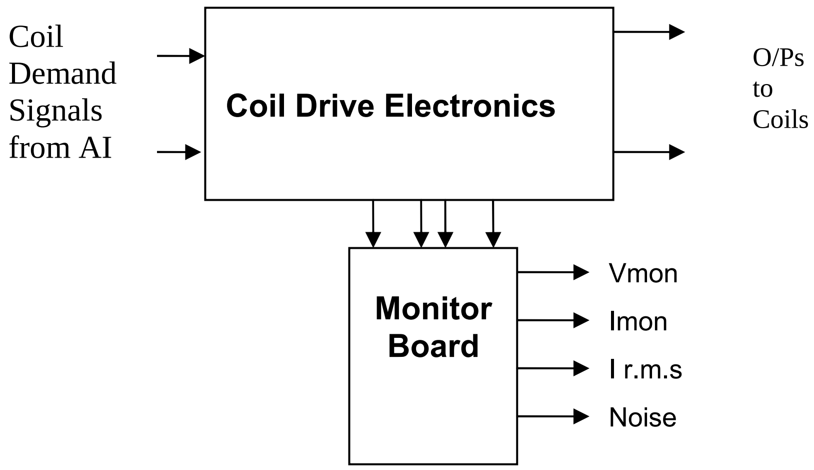


FIG. 1 TOP Driver Unit Block Diagram

Each TOP Driver Unit consists of four identical differential coil drive channels. It also contains the monitor board which monitors the output voltage, current, r.m.s current and noise from each channel

Unit……………….Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33120A	MY40016550
Oscilloscope	Tenma	72-6800	0900889
Power supply	Digimess	BP3002	211259
DVM	Fluke	115	
Signal Analyser	HP	35665A	3342A02392
Pre-amplifier	Stanford Systems	SR560	
DVM	TENMA	72-7730	
V/I calibrator	Time Electronics	1044	

Unit……………..Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt………………….
Date……………..1/7/10………………

3. Inspection

Remove the lid of the case.

Workmanship

Inspect the general workmanship standard and comment: √

A 390nF capacitor has been placed across resistors R5 and R23 on all channels to form a low pass filter to remove possible high frequency oscillations.

Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

4. Continuity Checks

Use a multi-meter to check the connections below.

Photodiode outputs

Pd Out to AA	SIGNAL	DESCRIPTION	Pd in from Sat	OK?
1	PD1P	Photodiode A+	1	√
2	PD2P	Photodiode B+	2	√
3	PD3P	Photodiode C+	3	√
4	PD4P	Photodiode D+	4	√
5	0V			
6	PD1N	Photodiode A-	14	√
7	PD2N	Photodiode B-	15	√
8	PD3N	Photodiode C-	16	√
9	PD4N	Photodiode D-	17	√

LED Monitors

LED Mon	SIGNAL	Monitors:	In from Sat	OK?
1	Imon1P	Current Source 1+	5	√
2	Imon2P	Current Source 2+	6	√
3	Imon3P	Current Source 3+	7	√
4	Imon4P	Current Source 4+	8	√
5	0V			
6	Imon1N	Current Source 1-	18	√
7	Imon2N	Current Source 2-	19	√
8	Imon3N	Current Source 3-	20	√
9	Imon4N	Current Source 4-	21	√

Power Supply to Satellite box

In from Sat	SIGNAL	DESCRIPTION	DC in Connector	OK?
9	V+	+17v Supply	A1	√
10	V+	+17v Supply	A1	√
11	V-	-17v Supply	A3	√
12	V-	-17v Supply	A3	√
13	0V	Return	A2	√
22	0V	Return	A2	√
23	0V	Return	A2	√
24	0V	Return	A2	√
25	0V	Return	A2	√

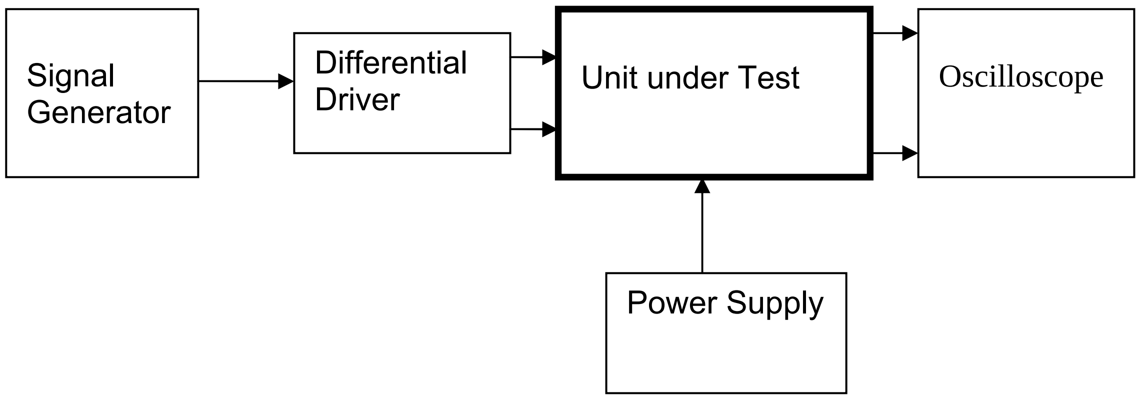
Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

Isolation Checks

Check that the driver ICs IC11 and IC12 are isolated from chassis on all channels. Apply a DVM on ohms range and measure the resistance between each transistor tab and the chassis.

IC Tab	Resistance	OK?
IC11 Channel 1	OL	√
IC12 Channel 1	OL	√
IC11 Channel 2	OL	√
IC12 Channel 2	OL	√
IC11 Channel 3	OL	√
IC12 Channel 3	OL	√
IC11 Channel 4	OL	√
IC12 Channel 4	OL	√

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the Drive Input of the unit under test:
Drive Input pins 1, 2, 3, 4 = positive input
Drive Input pins 6, 7, 8, 9 = negative input
Drive Input pin 5 = ground

Power (depending on connector availability)

Pd In from Sat pin 9, 10 = +16.5v	or DC in A1
Pd In from Sat pin 11, 12 = -16.5	or DC in A3
Pd In from Sat pins 22, 23, 24, 25 = 0v	or DC in A2

Coil Drive Outputs

Ch1+ = Coil out to Sat pin 1	Ch1- = Coil out to Sat pin 9
Ch2+ = Coil out to Sat pin 3	Ch2- = Coil out to Sat pin 11
Ch3+ = Coil out to Sat pin 5	Ch3- = Coil out to Sat pin 13
Ch4+ = Coil out to Sat pin 7	Ch4- = Coil out to Sat pin 15

Voltage, Current and R.M.S monitors

1	Voltage Monitor 4
2	Current Monitor 4
3	R.M.S Current 4
4	Voltage Monitor 3
5	Current Monitor 3
6	R.M.S Current 3
7	Voltage Monitor 2
8	Current Monitor 2
9	R.M.S Current 2
10	Voltage Monitor 1
11	Current Monitor 1
12	R.M.S Current 1
13 to 25	0v

Noise Monitor

1	Channel 1 Noise Monitor
2	Channel 2 Noise Monitor
3	Channel 3 Noise Monitor
4	Channel 4 Noise Monitor
5 to 9	0v

Unit……………… Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

6. Power

Check the polarity of the wiring from the 3 Pin Power Connector, to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

If this is correct,
Connect power to the unit
Set the supplies to 16.5v
Turn on

Record supply currents:

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
540mA	490mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	√	√
Rear Panel	√	√

If the power supplies are correct, proceed to the next section.

Unit……………….Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt…………………
Date……………..1/7/10………………

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

TEST SWITCHES

Channel	Indicator		OK?
	ON	OFF	
Ch1	√	√	√
Ch2	√	√	√
Ch3	√	√	√
Ch4	√	√	√

Unit………………Q_TOP_P49……………………Serial No ………………………………
Test Engineer…..Simon Pyatt………………….
Date……………..1/7/10………………

8. Current Monitor tests

The purpose of this test is to perform a functionality test on the current monitor and RMS circuits.

To do this, we need to draw a known current from each coil drive output. This is done by plugging the 39 ohm loads into each output, then adjusting the signal generator until the required voltage appears across each load resistor.

Remove all links W4 and W5.

Plug the power 39 ohm dummy load plug into the coil drive output.

Set the signal generator output to 2.5v at 100Hz.

Connect a scope probe to each end of one of the load resistors. Check that a sine wave of around 2v peak appears across each resistor.

Connect a true r.m.s meter across the channel 4 resistor, and carefully adjust the signal generator to give an r.m.s reading of 1.5 volts.

Record the peak output from each of the current monitors using the true r.m.s dvm, and each of the RMS circuits with the meter set to d.c.

Channel	Monitor Connector	Parameter	Theoretical Value (+/- .1v)	Measured Value	Pass/ Fail
1	Pin 2	Current Monitor	1v r.m.s		
	Pin 1	RMS Current	1v dc		
2	Pin 5	Current Monitor	1v r.m.s		
	Pin 4	RMS Current	1v dc		
3	Pin 8	Current Monitor	1v r.m.s		
	Pin 7	RMS Current	1v dc		
4	Pin 11	Current Monitor	1v r.m.s		
	Pin 10	RMS Current	1v dc		

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

9. Voltage and noise monitor tests

The purpose of this test is to verify and calibrate the Voltage Monitor circuit on each channel.

Switch all filters out. Remove the dummy loads and make differential voltage output measurements on the coil drive outputs at 100 Hz. Adjust the signal generator to give a voltage to 10v on the coil drive outputs.
Record the peak voltage on each Voltage Monitor pin, and check against the theoretical figure.

Channel	Coil Drive Output pins	Voltage Monitor socket Pin	Monitor output?	Expected value	OK?
1	Pins 1,9	Pin 3		3.2v to 3.4v	
2	Pins 3,11	Pin 6		3.2v to 3.4v	
3	Pins 5,13	Pin 9		3.2v to 3.4v	
4	Pins 7, 15	Pin 12		3.2v to 3.4v	

Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in μV√Hz on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA√Hz should give 2.9μV√Hz out.

Ch.	**Output (μV√Hz)**	**÷(Pre-amplifier gain)**	**Expected Value**	**Comparison**
1			2.9μV√Hz	
2			2.9μV√Hz	
3			2.9μV√Hz	
4			2.9μV√Hz	

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

10. Corner frequency tests

The purpose of this test is to verify that the frequency response of each filter stage of each channel is correct.
Ensure that links W4 and W5 in place.

Use the Dynamic Signal Analyser and signal generator.

With the filter switched in, measure the frequency response of each channel in turn between 1 Hz and 1 kHz. Measure the gain at the spot frequencies below and record them. Measure the gain at 0.1 Hz using the signal generator and scope, using a 1v peak input signal, and recording the peak output. In each case the output is measured differentially between TP9 and TP13. Connect the 39 ohm loads across each coil output to simulate the coils.

Channel 1

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz			
10Hz			
100Hz			
1kHz			

Channel 2

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz			
10Hz			
100Hz			
1kHz			

Channel 3

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz			
10Hz			
100Hz			
1kHz			

Channel 4

Frequency	Gain (dB)	Expected Gain	Pass/Fail
1Hz			
10Hz			
100Hz			
1kHz			

0.1 Hz measurements with the signal generator and oscilloscope

Frequency	Output	Expected O/P	Pass/Fail
Ch1			
Ch2			
Ch3			
Ch4			

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

11. Distortion

Remove links W4 and W5. Plug in the 5 Watt 39 Ohm dummy loads. Increase input voltage to 10v peak, f = 1kHz. Check the differential voltage across each load for distortion with an analogue oscilloscope.

	Distortion Free?
Ch1	
Ch2	
Ch3	
Ch4	

12. Full Load Test

Apply the DC source to the input to the differential amplifier. Connect the 39 Ohm 5 watt loads to the outputs.
Increase the input voltage to 10v with respect to 0v, and monitor the temperatures of the drive amplifiers. If their temperature increases above 100°C, flag a problem!
Leave running for 10 minutes, then record the temperatures of drive amplifiers, and the differential output voltages from the amplifier (TP9 and TP13).

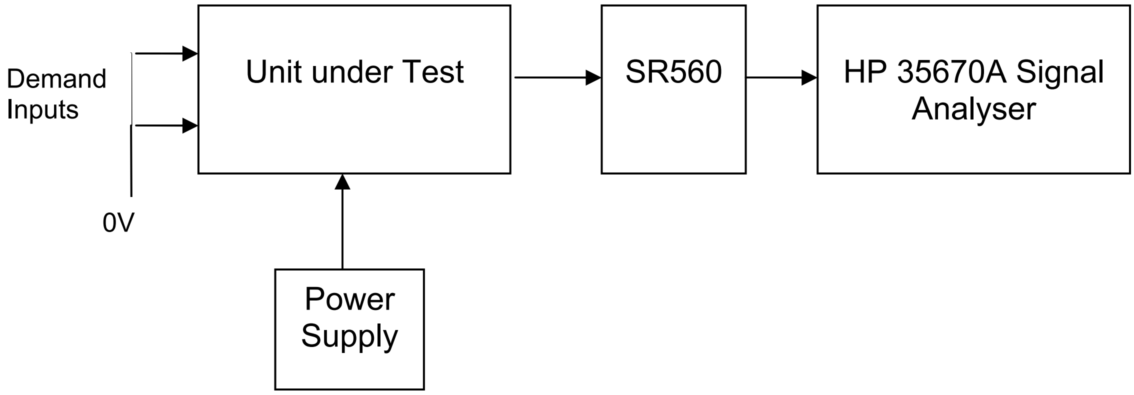
The output voltages should be recorded.

Output	**Voltage**	**> 24v?**	**DRIVER**	**Temperature**	**<60°C?**
CH1 Positive			**CH1 IC1**		
CH1 Negative			**CH1 IC5**		
CH2 Positive			**CH2 IC1**		
CH2 Negative			**CH2 IC5**		
CH3 Positive			**CH3 IC1**		
CH3 Negative			**CH3 IC5**		
CH4 Positive			**CH4 IC1**		
CH4 Negative			**CH4 IC5**		

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

13. Noise Tests

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.
Replace the filter links W4 and W5 on each channel.
Replace the lid of the box, and replace screws.
Connect the filter test box, and switch in all filters.
Switch it out of Test Mode
Use the HP 35670A Dynamic Signal Analyser.
Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 39 Ohm loads to the outputs.
Switch the filters in.
Use Stuart Aston's noise measurement set up, loaded from disc.
Measure the noise output from each channel in turn at the amplifier outputs. The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-161.15dB		
Ch2	-161.15dB		
Ch3	-161.15dB		
Ch4	-161.15dB		

Notes:
Specified noise output current at 10 Hz = 73 pA/√Hz
Total output resistance = 120 Ohms
Amplifier noise voltage should therefore be = 8.76nV/√Hz or -161.15 dB

The noise monitor amplifier has an internal gain of 42dB at 10Hz.
The noise floor is about -133dB.

Unit……………………………………Serial No ………………………………
Test Engineer…………………
Date……………………………

14. Full Current Tests

High power dummy loads are needed for this test.

With the dummy loads removed, measure and record the value of each resistor. Nominal 39 Ohm power resistors should be used.

Plug in the dummy load.

Remove the filter links.

Drive the unit with a 10v peak sine wave on each channel, which should measure 7.07 volts on a true r.m.s meter.

Measure the voltage across each load resistor and record it. Calculate the current through each resistor, and compare with the specification. If a true r.m.s meter is used to make the measurement, compare with the r.m.s specification

Channel	**R =**	**V=**	**Therefore I =**	**Spec (peak)**	**Spec (r.m.s)**	**Pass?**
1	39.3			>200mA	>141.4mA	
2	39.4			>200mA	>141.4mA	
3	39.3			>200mA	>141.4mA	
4	39.4			>200mA	>141.4mA	

(The measured output is slightly low due to not being able to adjust the input voltage to the correct level of 7.07V)

Unit……………………………………Serial No ………………………………
Test Engineer ………
Date …………………

15. Final Assembly Checks

1. Remove the lid of the box.

2. Unplug all external connections.

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.

4. Check that all internal connectors are firmly mated.

5. Tighten the screw-locks holding all the external connectors.

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.

8. Check that links W4 and W5 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	
Driver board ID	
Driver board Drawing No/Issue No	
Driver board Serial Number	
Monitor board ID	
Monitor board Drawing No/Issue No	
Monitor board Serial Number	

10. Check the security of any modification wires.

11. Visually inspect.

12. Put the lid on and fasten all screws,

    Check all external screws for tightness.