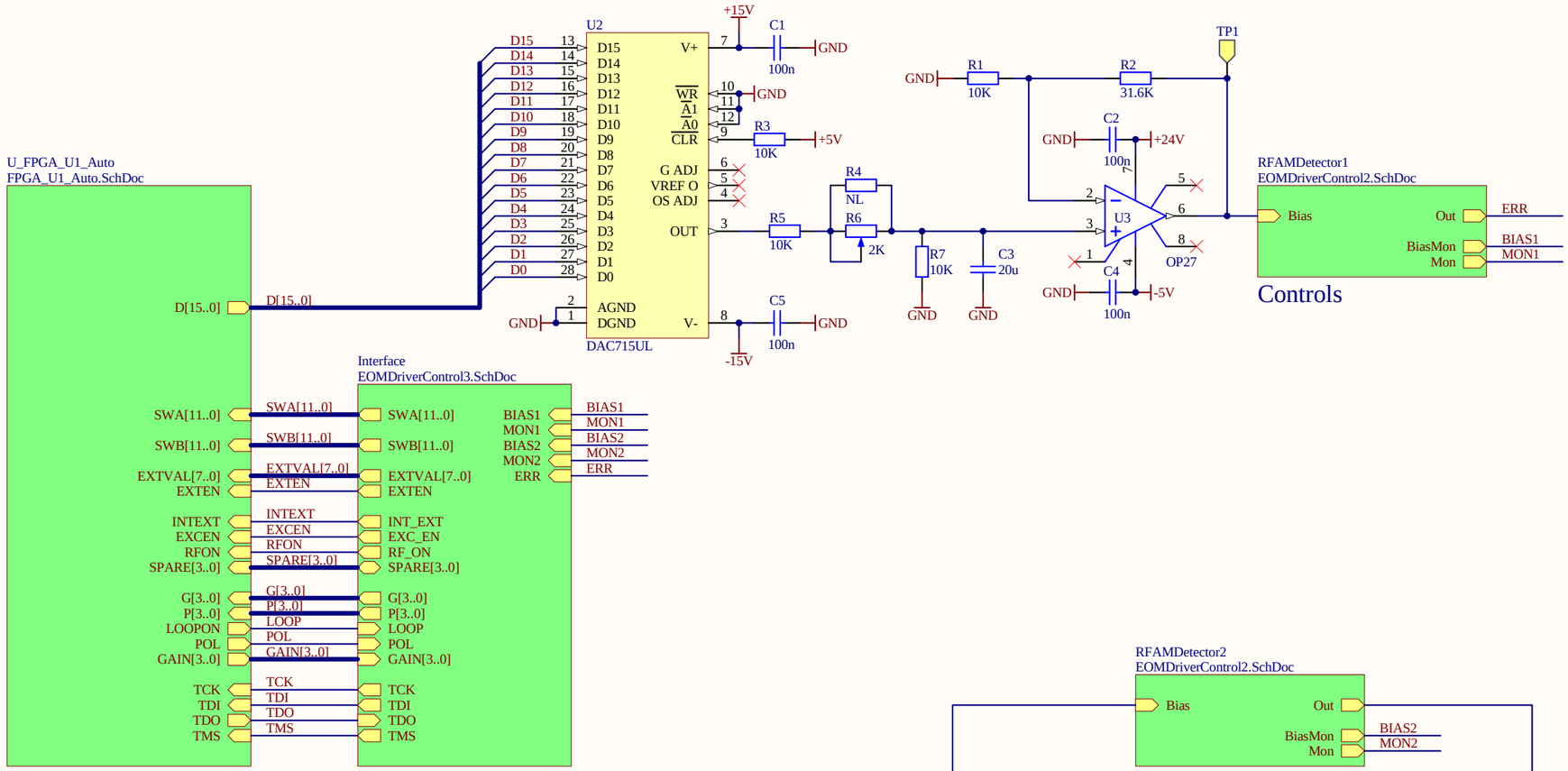
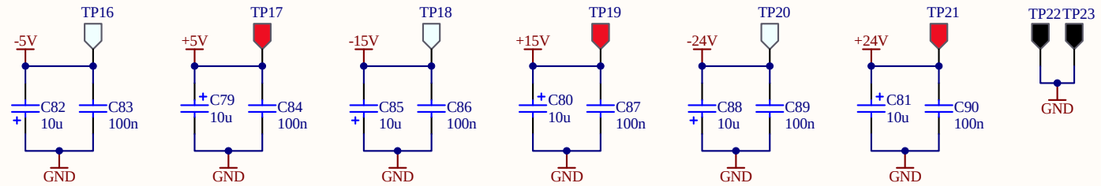
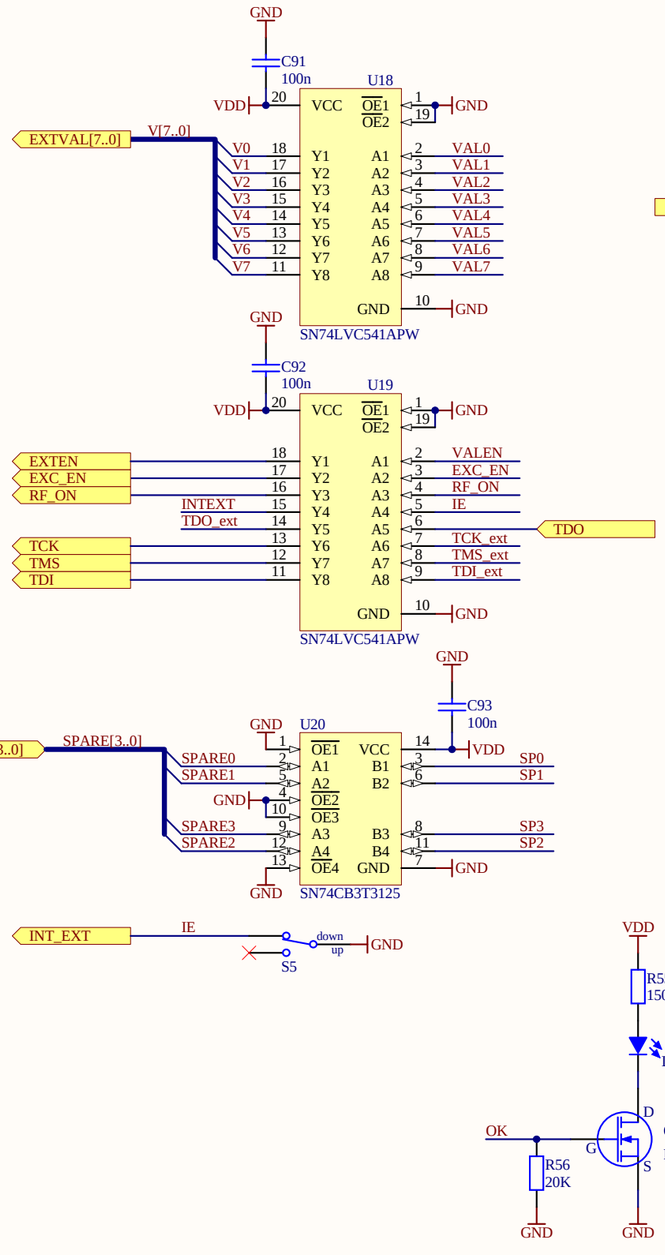


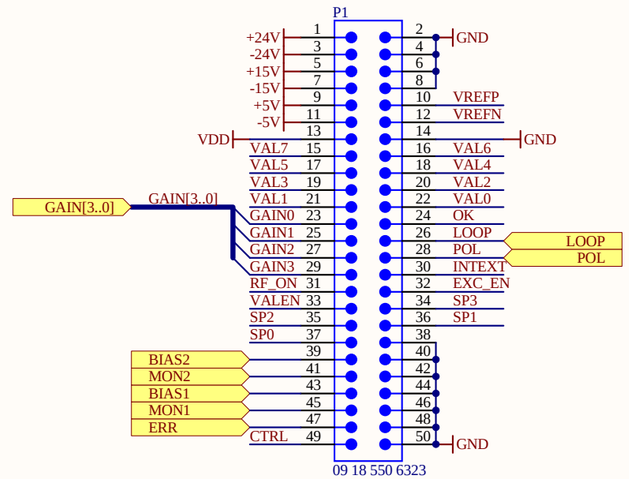
Title	**RF AM Stabilization**	
Size: B	Number: **D0900761**	Revision: **A**
Date: 1/31/2010	Sheet 1 of 4	
File: C:\Users\..\EOMDriverControl1.SchDoc	Drawn By: Daniel Sigg	

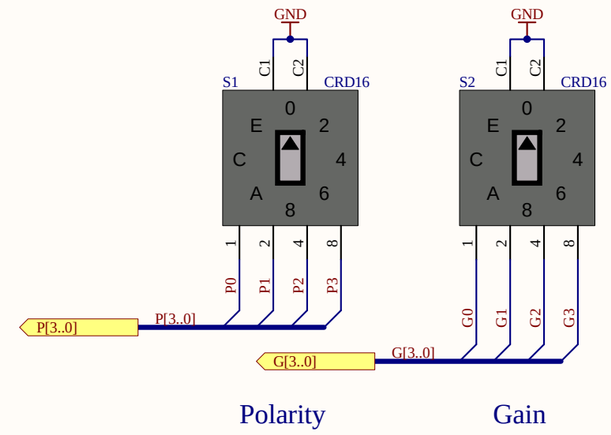
RF in
24dBm max.

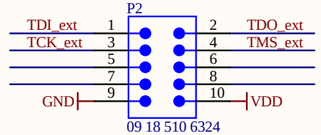
Title	RF AM Stabilization		
Size: B	Number: D0900761	Revision: A	
Date: 1/31/2010		Sheet 2 of 4	
File: C:\Users\..\EOMDriverControl2.SchDoc		Drawn By: Daniel Sigg	

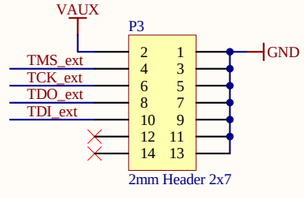


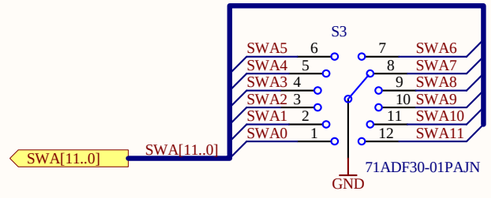


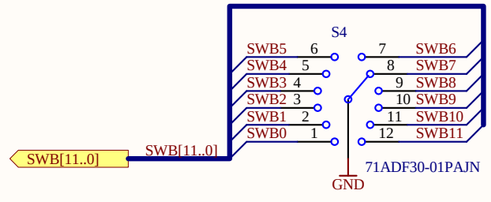




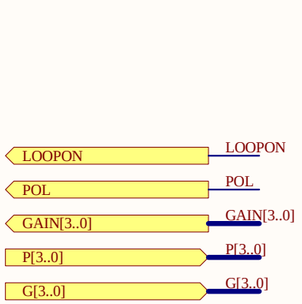


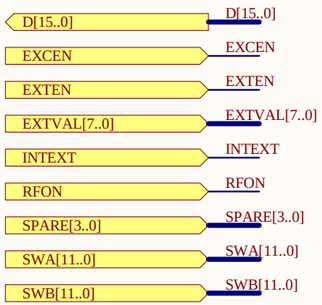


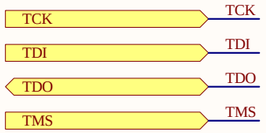


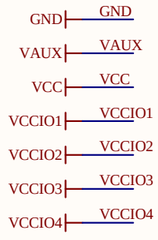


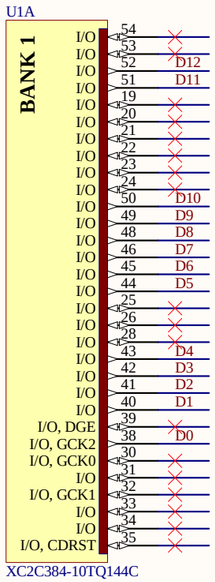
Title: **RF AM Stabilization**		
Size: B	Number: **D0900761**	Revision: **A**
Date: 1/31/2010		Sheet 3 of 4
File: C:\Users\..\EOMDriverControl3.SchDoc		Drawn By: Daniel Sigg

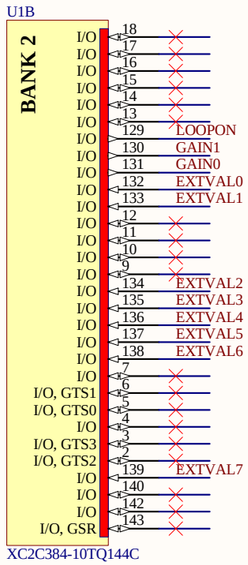


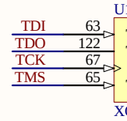


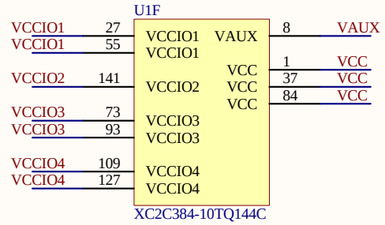


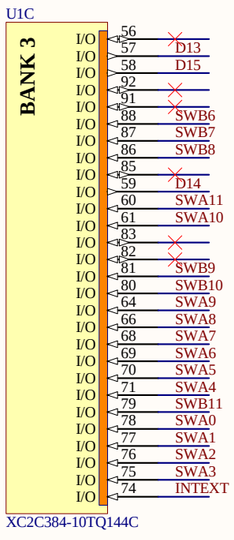


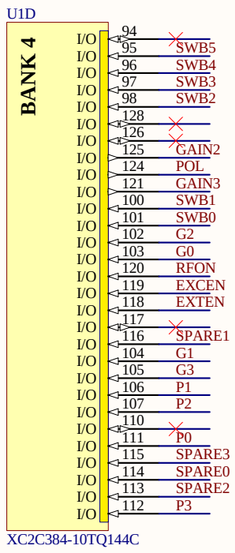


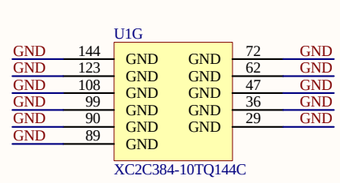






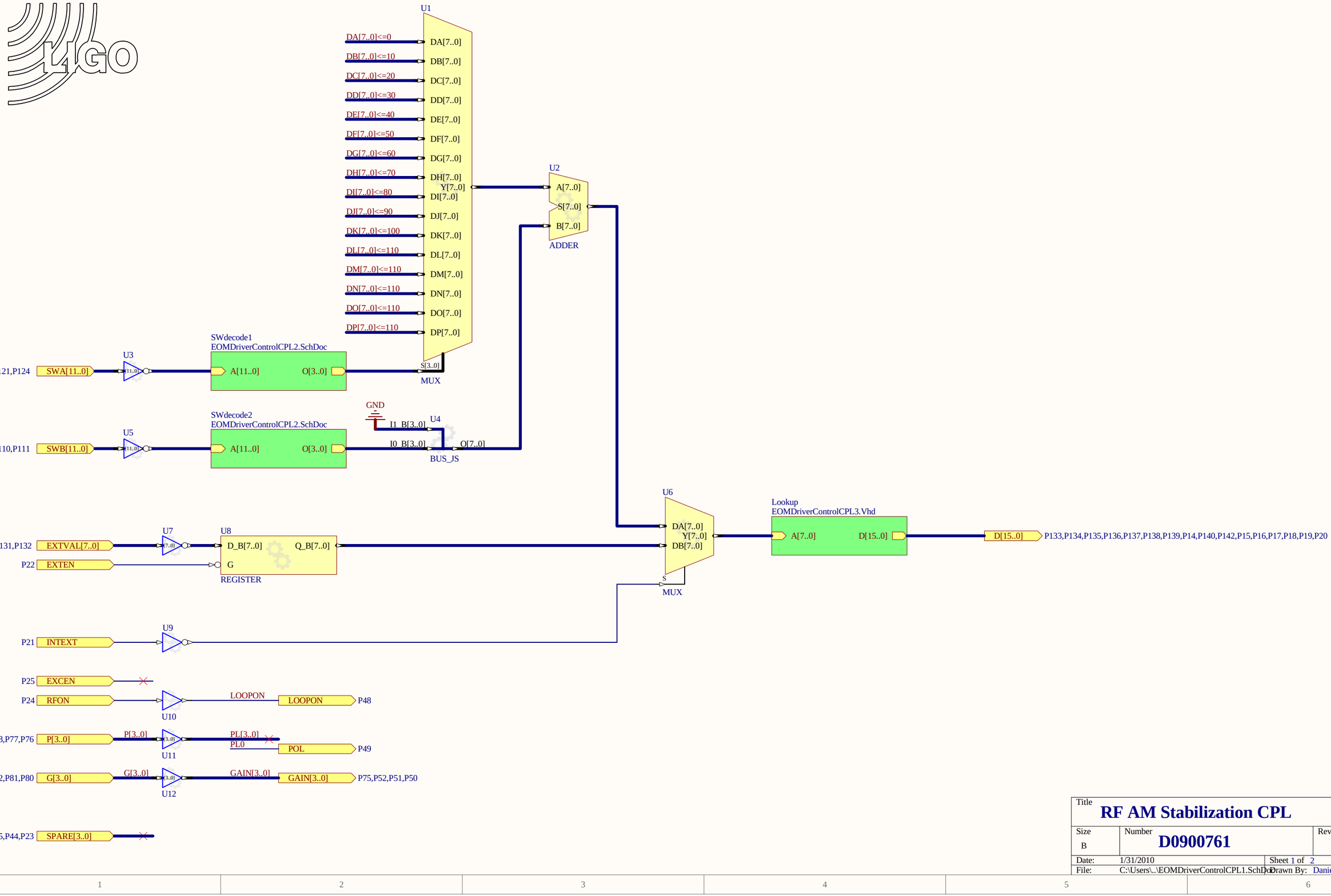




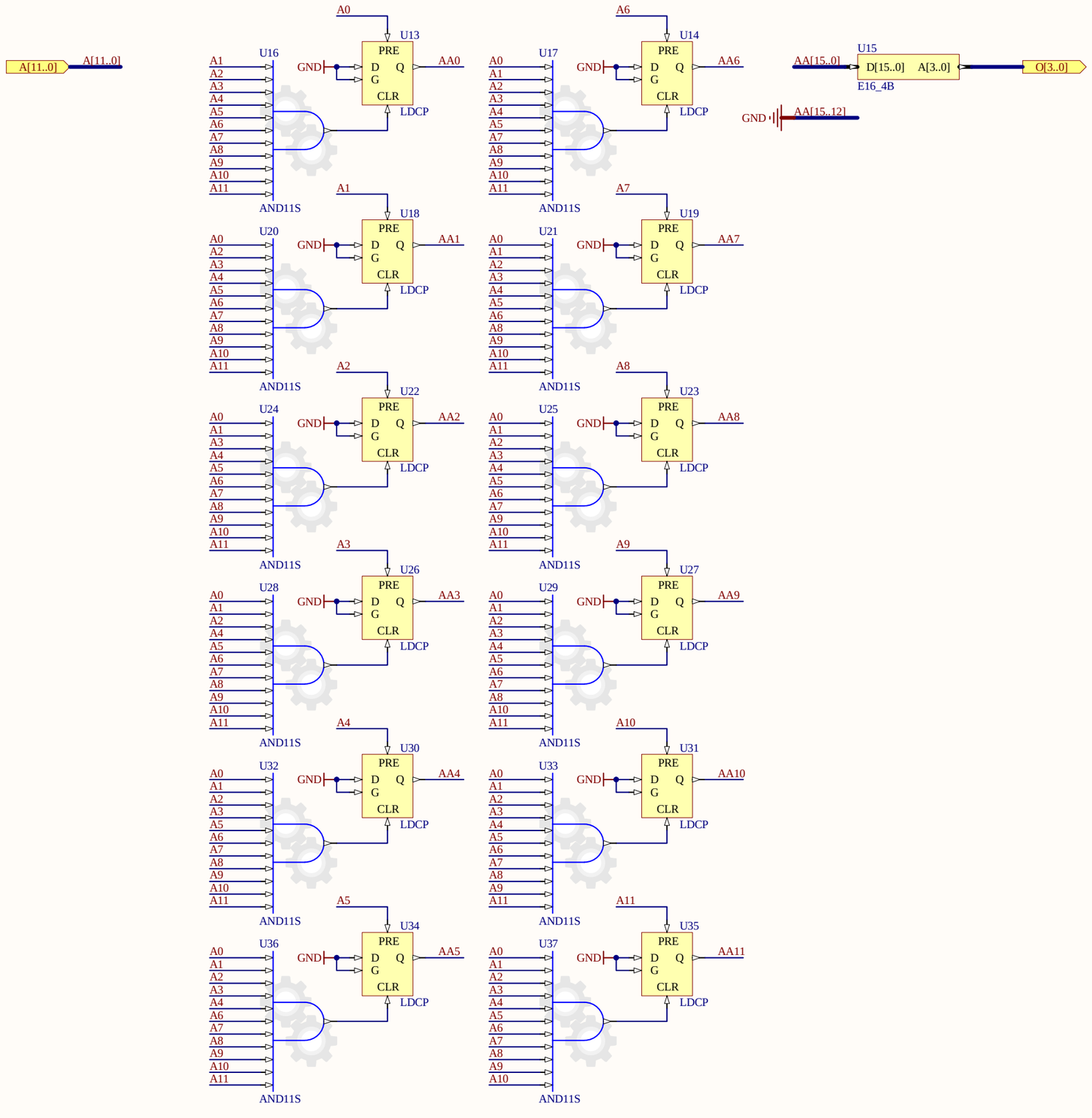


WARNING : THIS IS AN AUTOGENERATED FILE

Title: **RF AM Stabilization**		
Size: B	Number: **D0900761**	Revision: **A**
Date: 1/31/2010		Sheet 4 of 4
File: C:\Users\..\FPGA_U1_Auto.SchDoc		Drawn By: Daniel Sigg



Title	**RF AM Stabilization CPL**	
Size: B	Number: **D0900761**	Revision: **A**
Date: 1/31/2010		Sheet 1 of 2
File: C:\Users\..\EOMDriverControlCPL1.SchDoc		Drawn By: Daniel Sigg



Title	**RF AM Stabilization CPL**	
Size: B	Number: **D0900761**	Revision: **A**
Date: 1/31/2010	Sheet 2 of 2	
File: C:\Users\..\EOMDriverControlCPL2.SchDoc	Drawn By: Daniel Sigg	

```
-------------------------------------------------------------------------------
-- SubModule EOMDriverControlCPL3
-- Created   4/27/2009 3:32:35 PM
-------------------------------------------------------------------------------
Library IEEE;
Use IEEE.Std_Logic_1164.all;
Use IEEE.Numeric_Std.all;

entity EOMDriverControlCPL3 is port
   (
     A        : in    std_logic_vector(7 downto 0);
     D        : out   std_logic_vector(15 downto 0)
   );
end EOMDriverControlCPL3;
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
architecture Structure of EOMDriverControlCPL3 is

-- Type Declarations
type word is range 0 to 65535;
type rom_type is array (0 to 255) of word;

-- constant Declarations
constant rom : rom_type :=
(4231, 4330, 4431, 4534, 4640, 4748, 4858, 4971, 5087, 5206, 5327,
5451, 5578, 5708, 5841, 5977, 6116, 6259, 6404, 6554, 6706, 6862,
7022, 7186, 7353, 7524, 7700, 7879, 8063, 8250, 8443, 8639, 8840,
9046, 9257, 9473, 9693, 9919, 10150, 10387, 10629, 10876, 11129,
11389, 11654, 11925, 12203, 12487, 12778, 13076, 13381, 13692, 14011,
14337, 14671, 15013, 15363, 15721, 16087, 16462, 16845, 17237, 17639,
18050, 18470, 18901, 19341, 19791, 20252, 20724, 21207, 21701, 22206,
22723, 23253, 23794, 24349, 24916, 25496, 26090, 26698, 27320, 27956,
28607, 29273, 29955, 30653, 31367, 32098, 32845, 33610, 34393, 35194,
36014, 36853, 37711, 38590, 39489, 40409, 41350, 42313, 43299, 44307,
45339, 46395, 47476, 48582, 49713, 50871, 52056, 53269, 54510, 55779,
57079, 58408, 59769, 61161, 62585, 64043, 65535, others => 65535);

-- Functions
   function get_word (r : in rom_type; i : natural) return natural is
      variable c : word;
   begin
      c := r (i);
      return natural(c);
   end function get_word;

-- Signal Declarations
   signal addr : unsigned (7 downto 0);

begin

   addr <= unsigned (A);
   D <= std_logic_vector (To_unsigned (get_word (rom, To_integer (addr)), 16));

end Structure;
-------------------------------------------------------------------------------
```