LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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| "UK SUS Satellite Amplifier" Test Plan Production Version | | | | |
| Original Test Plan by J. Heefner Revisions by C. Adams and V. Sandberg | | | | |

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1 Introduction

This document describes the tests of the production version of the aLIGO Quad Suspension Satellite Amplifier with modifications described in LIGO-E1100767-v1. The amplifiers were designed and fabricated by the UK group located at the University of Birmingham. The schematic drawings describing the circuits are in document LIGO-D0901284-v1, with modifications to the original design described in documents LIGO-E1100767 and LIGO- G1100856-v5. The modifications were necessary to solve a number of problems: the need to match the dynamic range of the preamps to the range of operating currents encountered from the bOSEMs and aOSEMs, to cure an instability when connecting a long input cable to the preamp, and to replace problematic parts. The design requirements for the driver can be found in document LIGO-T060067-00-C, "AdL Quad Suspension UK Coil Driver Design Requirements". The requirements for the satellite amplifiers are not called out explicitly in the requirements document and have been interpreted from it to create the criteria used in this test plan.

The "SUS satellite amplifiers" (as they will be called) consist of three subsystems: a front-end current-to-voltage preamplifier to process the OSEM photodiode currents (typically 60uA DC), a whitening filter with a differential cable driver following the preamp, and a DC current source to provide a constant 35mA DC current to power the OSEM LEDs. The satellite box chassis also provides a connector pass through for the OSEM coils' signals. A simplified model used to derive the SPICE simulation of the photodiode whitening stage and schematics for the preamp and the current source are shown in Appendix 1. The response of the photodiode preamplifier is shown in Fig. 1. The whitening stage passes DC signals with a unity gain and amplifying high frequency signals (frequencies above 1Hz) with a gain of ~x30.

The tests described in the test plan are: to measure noise spectra and to verify that the amplifiers meet the design requirements. It is assumed that the amplifiers have been thoroughly tested by the University of Birmingham prior to shipment.

A warning about output voltages, ranges, and factors of x2: We are using $\pm 10V$ as the useful output range of the op amps used in the circuits. The circuits can drive a larger range, but with larger deviations from linear behavior, so we restrict ourselves to $\pm 10V$. When referenced to chassis ground, all signal voltages measured will be less than 10V in absolute magnitude. When measured across two outputs, e.g., "J2+" and "J2-", it is possible to measure a differential voltage ranging from -20V to +20V and to thereby realize a dynamic range of 40V. The noise and transfer function output voltages will always refer to the differential voltages measured at the outputs from the cable driver op amps.

2 Test Equipment

- Stanford Research SR785 Dynamic Signal Analyzer
- Voltmeter for DC measurements
- Oscilloscope
- Board Schematics- D0901284-v1
- Testing scripts (located in the aLIGO SVN repository at: "sus/trunk/electronicstesting/sus_gpib_scripts/")



Fig. 1 Transresistance transfer function for the full satellite photodiode amplifier, from i-to-v preamp through the whitening filter to the differential cable driver. The plot is derived from a SPICE simulation of the aLIGO SUS Satellite Amplifier, D0901284-v1, with feedback resistor Rx02 = 121k. The vertical scales are (on the left side) the transresistance magnitude ratio V_{out}/I_{in} in ohms and (on the right side) the phase change of the output with respect to the input signals in units of "degrees". The horizontal scale is frequency in Hz. Note: The output voltage is the differential voltage (e.g., taken across the output jacks "J2+" and "J2-").

The features of this curve are a described by a zero at $f_{21} = 0.4$ Hz, a pole at $f_{p1} = 10$ Hz, and a pole at $f_{p2} = -4$ kHz. The first zero-pole pair is from the whitening stage. The pole at 4 kHz is from the RC compensation in the feedback loop in the current-to-voltage stage. The transresistance at 10 Hz is 4.60×10^6 ohms. For comparison, note that the transresistance at DC is 242k ohms, as expected from the 121k resistor in the feedback loop of the i-to-v stage and the factor of x2 from the differential output stage.

3 Tests

The tests are broken into three categories—photodiode amplifier noise and signal conditioning, LED current drive, and monitoring and indicators. The tests for each of these categories are described in the sections below.

3.1 Photodiode Amplifier Tests

3.1.1 Amplifier Noise

The noise floor for the B-OSEM used in the AdL Quad noise prototype is approximately 5×10^{-11} m/ $\sqrt{\text{Hz}}$ at 10 Hz. This corresponds to a current noise of $1.3\text{pA}/\sqrt{\text{Hz}}$ at the output of the B-OSEM photodiode. The feedback resistor in the photodiode preamplifier current-to-voltage converter portion of the circuit is 121K ohms. The i-to-v stage is followed by a whitening-filter circuit with a zero at 0.4Hz, a pole at 10Hz, and a differential output stage. The transfer function for the full circuit is shown in Fig. 1. At 10 Hz the transresistance is 4.60×10^6 Ohms. This value leads to a differential-output-referred-noise voltage of $6.0\mu\text{V}/\sqrt{\text{Hz}}$:

 $(1.3 \text{pA}/\sqrt{\text{Hz}}) \text{ x} (4.60 \text{ x} 10^6 \text{ Ohms})_{[10\text{Hz}]} = 6.0 \mu \text{V}/\sqrt{\text{Hz}_{[10\text{Hz}]}},$

The differential-output-referred-noise voltage of the satellite amplifier should be less than $6.0\mu V/\sqrt{Hz}_{[10H_2]}$, to not degrade the sensitivity of the B-OSEM photodiode signal.



Fig. 2 Amplifier noise power spectrum test setup.

The test setup for the noise measurements is shown in Fig. 2. The inputs to the satellite amplifier should not be connected during the noise test. *The inputs to the satellite amplifier under test should be floating*. Do not connect them to ground. (The i-to-v preamp expects a high resistance current source for its input source.) In the table below, record the output voltage noise measured at 10Hz. In addition, save the power spectra files created by the scripts to disk and record the file name in the space provided below.

| Channel Number (Measurement Point) | Noise at 10Hz [µVrms/√ Hz] |
|--|-------------------------------|
| 1 (J2-14, J2-1) | |
| 2 (J2-15, J2-2) | |
| 3 (J2-16, J2-3) | |
| 4 (J2-17, J2-4) | |

File Name for noise measurement (0.1 Hz < freg < 100 Hz):

Name of saved file:

3.1.2 Amplifier Response

The photodiode amplifier is a current-to-voltage converter followed by a whitening-filter circuit with a zero at 0.4Hz, a pole at 10Hz, and a differential output driver. The nominal gain is 242k ohms at DC and rising to 6.68MEG ohms for frequencies above 100Hz. The test setup for measurement of the frequency response of the amplifier is shown in the figure below.

The voltage generator (inside the SR785) used to create the input signal and is connected in series with a 240k ohm resistor to mockup a current source. The choice of a 242k ohm resistor in series with the source will make the overall voltage gain of this test setup 1.0. *To avoid overdriving and saturating the amplifier, the input voltage source should be set to 0.3 V amplitude.* A plot of expected V_{out}/V_{in} transfer function is shown in Fig. 4 below.



Fig. 3 Photodiode Amplifier Response Test Setup.



Fig. 4 Voltage transfer function expected from setup as shown in Fig. 3 above. A 240k ohm series resistor is assumed. The output is plotted on the y-axis as V_{out}/V_{in} . The frequency is plotted on the x-axis and is in Hz. The plot on the left plots the voltage ratio and the plot on the right plots the ratio in dB(V/V).

The table below tabulates the simulation's voltage gains as a function of frequency for the configuration shown in Fig. 3.

| Frequency [Hz] | Voltage Gain [V/V] | Gain [dB] | Phase [deg] |
|----------------|--------------------|-----------|-------------|
| 0.1 | 1.04 | 0.35 | -165.9 |
| 1 | 2.80 | 8.95 | -116.4 |
| 10 | 19.1 | 25.6 | -135.6 |
| 100 | 27.7 | 28.86 | -175.2 |
| 1000 | 27.5 | 28.79 | -189.9 |

Serial Number: _____

Tech: _____

In the tables below, record the measured gain for each channel. Expect agreement at the 5% level of tolerance.

| Freq (Hz) Input=J1-25 Return=J1-13 | Nominal Gain (dBV/V) Output= J2-14, J2-1 | Nominal Phase (Degrees) | Actual Gain (dBV/V) | Actual Phase (Degrees) |
|--|--|-------------------------------|------------------------|---------------------------|
| 0.1 | 0.35 | -165.9 | | |
| 1 | 8.95 | -116.4 | | |
| 10 | 25.64 | -135.6 | | |
| 100 | 28.86 | -175.2 | | |
| 1K | 28.79 | -189.9 | | |

Table 1: Channel 1 Transfer Function Measurements

 Table 2: Channel 2 Transfer Function Measurements

| Freq (Hz) | Nominal Gain | Nominal | Actual Gain | Actual Phase |
|--------------|---------------------|-----------|-------------|--------------|
| Input=J1-22 | (dBV/V) | Phase | (dBV/V) | (Degrees) |
| Return=J1-13 | Output= J2-15, J2-2 | (Degrees) | | |
| 0.1 | 0.35 | -165.9 | | |
| 1 | 8.95 | -116.4 | | |
| 10 | 25.64 | -135.6 | | |
| 100 | 28.86 | -175.2 | | |
| 1K | 28.79 | -189.9 | | |

Table 3: Channel 3 Transfer Function Measurements

| Freq (Hz) Input=J1-19 | Nominal Gain (dBV/V) | Nominal Phase | Actual Gain (dBV/V) | Actual Phase (Degrees) |
|--------------------------|-------------------------|------------------|------------------------|---------------------------|
| Return=J1-13 | Output= J2-16, J2-3 | (Degrees) | | |
| 0.1 | 0.35 | -165.9 | | |
| 1 | 8.95 | -116.4 | | |
| 10 | 25.64 | -135.6 | | |
| 100 | 28.86 | -175.2 | | |
| 1K | 28.79 | -189.9 | | |

| Table 4: Channel 4 Transfer J | Function Measurements |
|-------------------------------|-----------------------|
|-------------------------------|-----------------------|

| Freq (Hz) Input=J1-16 | Nominal Gain (dBV/V) | Nominal Phase | Actual Gain (dBV/V) | Actual Phase (Degrees) |
|--------------------------|-------------------------|------------------|------------------------|---------------------------|
| Return=J1-13 | Output= J2-17, J2-4 | (Degrees) | | _ |
| 0.1 | 0.35 | -165.9 | | |
| 1 | 8.95 | -116.4 | | |
| 10 | 25.64 | -135.6 | | |
| 100 | 28.86 | -175.2 | | |
| 1K | 28.79 | -189.9 | | |

| Serial Nun | nber: |
|------------|-------|
| | |

The LED driver circuit is a current source that produces a constant 35mA into a load (LED). During these tests a 10 ohm resistor in place of the OSEM LED is used to measure the current source output. Connect a 10 ohm resistor between the output pins for each LED drive output and using a voltmeter record the output current for each channel. Record the results in the table below. (For convenience, it is possible to perform the current and voltage monitor measurements described in section 3.3.1 of this test plan at the same time as these tests are being conducted.)

| Channel Number | Output Pins (Connect 10 ohms Across) | Measured Voltage Vmeas | Actual Current= Vmeas/10ohms |
|----------------|--|---------------------------|---------------------------------|
| 1 | J1-24, J1-11 | | |
| 2 | J1-21, J1-8 | | |
| 3 | J1-18, J1-5 | | |
| 4 | J1-15, J1-2 | | |

Table 5: LED Drive Current Measurements

3.3 Monitoring and Indicators

3.3.1 LED Current and Voltage Monitors

The test setup for these measurements is the same as that used in section 3.2 of this test plan. The nominal gain of the LED current monitor is 1V/35mA and the nominal gain of the LED voltage monitor is 1V/V. The nominal readings for the current and voltage monitors are 1V and 5.495V, respectively. In the table below record the LED current and voltage monitors for each channel.

 Table 6: LED Drive Current and Voltage Monitor Measurements

| Channel Number | Output Pins (Connect 10 ohms Across) | Current Monitor Pins | Measured Current Monitor Value | Voltage Monitor Pins | Measured Voltage Monitor Value |
|-------------------|--|----------------------------|--------------------------------------|----------------------------|-----------------------------------|
| 1 | J1-24, J1-11 | J2-5, J2-18 | | J4-5, J4-24 | |
| 2 | J1-21, J1-8 | J2-6, J2-19 | | J4-6, J4-25 | |
| 3 | J1-18, J1-5 | J2-7, J2-20 | | J4-7, J4-26 | |
| 4 | J1-15, J1-2 | J2-8, J2-21 | | J4-8, J4-27 | |

3.3.2 LED Current Source Fault Indicators

The satellite amplifier has four fault indicators that illuminate when the current output by the current source is not 35 mA, +/-TBD. With no connections to J1, verify that all four fault LEDs are illuminated and record the results below.

All four fault indicators illuminated?

7

| Serial Number: | |
|----------------|--|
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3.3.3 Photodiode Amplifier Local Monitor

The satellite amplifier design provides for local monitoring of the output of each photodiode amplifier. Using the test setup shown in Fig. 3, replace the SR785 by a 1VDC source and keep the 240k ohm series resistor. Connect the 1V DC source through the 240k ohm to pins J1:[25, 22, 19, 16] and use J1-13 as signal return for all channels. The output voltage should be read between "J4+" and "J4-" and should be 1VDC. Record the results in the table below.

| Channel Number & Inputs | Monitor Pins (J4+, J4-) | Measured Voltage |
|----------------------------|----------------------------|------------------|
| 1 (J1-25, J1-13) | J4-9, J4-28 | |
| 2 (J1-22, J1-13) | J4-10, J4-29 | |
| 3 (J1-19, J1-13) | J4-11, J4-30 | |
| 4 (J1-16, J1-13) | J4-12, J4-31 | |

Table 7: Photodiode Amplifier Monitor Measurements

Notes

Serial Number: _____

Tech: _____

Appendix

Schematic diagrams of the photodiode preamplifier, the LED current source, and the SPICE simulations.



Schematic circuit diagram of channel 1 photodiode preamplifier, from D0901284-v1 and modifications as described in E1100767-v1.

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Schematic circuit diagram of channel 1 LED current source, from D0901284-v1

Date: _____

SPICE Simulations Circuit Schematic Drawings



LTspice circuit for simulating the i-to-v photodiode preamplifer transresistance. Circuit has a current source input.



LTspice circuit for simulating the v-to-v photodiode preamplifer voltage transfer function. Circuit has a voltage source and series resistor input.