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UK Upper Intermediate Mass Driver Pre-Production Prototype Bench Test and Evaluation		
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1 Introduction

We report on the bench-test results and evaluation of the Advanced LIGO Suspension Upper Intermediate Mass Driver chassis (UIM) supplied as a pre-production prototype by the University of Birmingham. Bench tests were conducted in accordance with the test plan described in LIGO document T080021-00-C, “UK UIM Driver Pre-Production Test Plan”. A copy of the scanned version of the test plan evaluation results with bench notes is included in Appendix A of this document. The design requirements for the UIM Driver can be found in LIGO document number T060067-00-C, “AdL Quad Suspension UK Coil Driver Design Requirements”. We assume familiarity with these documents in the descriptions that follow. For reference, the relevant requirements for the UIM driver are listed below:

Upper Intermediate Mass (UIM) Requirements

The UIM requirements cover the 4 coils used in the UIM. They are commonly referred to as UL, LL, UR and LR, denoting their relative positions.

Output Current

The maximum output current indicated by the suspension system models occurs for the High Dynamic Range mode of operation (also known as the “noisy state” or the “acquire mode”) for the UIM is $\sim 90\mu\text{A}_{\text{rms}}$. Assuming a safety factor of $\times 20$ to cover transient events, each UIM coil driver should be capable of sourcing or sinking at least 2mA_{rms} . The UIM coil driver current is frequency dependent. For frequencies less than 1 Hz, the coil driver must be capable of supplying the full 2mA_{rms} , and the driver shall be capable of supplying currents of up to $16\mu\text{A}_{\text{rms}}$ ($0.8\mu\text{A} \times 20$) for frequencies of 100Hz.

Output Noise

Frequency	Current Noise Requirement
1Hz	0.500 nA/ $\sqrt{\text{Hz}}$
10 Hz	3 pA/ $\sqrt{\text{Hz}}$
100 Hz	200 nA/ $\sqrt{\text{Hz}}$
1000 Hz	1000 nA/ $\sqrt{\text{Hz}}$

This report follows the outline of LIGO document T070288-00-C, “AdL Noise Prototype Electronics Test Plan”. The tests outlined in T0700288-00-C are a series of tests and evaluations that will be used to evaluate the full set of electronics provided by the University of Birmingham for the AdL Quad Suspension system.

2 Observations

The packaging, labeling, and configuration of the UIM Driver-Monitor is similar to the Top Driver and the PUM Driver units. The test reviews of the Top Driver (T080034-00-C) and the PUM Driver (T080050-00-C) document details of shared concerns on the physical properties, cabling, mechanical layout, serviceability, labeling, and maintenance issues. The same concerns and recommendations also apply to this system and will not be repeated here. In the following we describe some specific concerns to the UIM Driver electronics. These are presented as major, minor, and cosmetic.

2.1 Major

1. We need the ability to inject a test signal without breaking the control loop. In the present design enabling the test input disables the main drive signal. A possible alteration would be to add two switches to the input in parallel: one for the test input and a second for the main input (to preserve the ability to have a watchdog circuit).
2. What circuit drives this board? This is a question of input and output impedances. If there are, e.g., 100 ohm resistors in series with the outputs (or 300 ohms in the advanced LIGO AA and AI Filters, D070081) the loading by the input circuit will lower the DC gain by ~5% (or ~12%, respectively). This is a broader, system level question, but the loading of stages and out impedances need to be specified.
3. The default setting for the DC bias of the input circuit op-amps needs to be settled. Leaving the bias current returns open leads the device vulnerable to common mode noise and problems when connected into different settings.
4. The AD743 is no longer available in a DIP package and the only other package is a 16-pin SOIC. This is a major drawback to using this chip and will require a re-layout.
5. The switching speed of the relays is slow and raises the question of long-term stability of the delay time. From the time the drive signal is asserted to when the relay contacts close (measured using the readback circuit) was ~1ms. This action needs to be synchronized with a corresponding software-switched digital filter, which defines the meaning of simultaneity in this case. A long delay and any variation in that delay will be problematic and lead to stability problems in the overall control system. Since we are often trying to switch a digital filter simultaneously with the analog switch this could be a problem. We also noticed some ringing and contact closure bounces.

2.2 Minor

1. The signal arrangement on J6 and J7 is unusual. It starts on pin 19/37 skipping every third line and then switches to using every pair. The way the channels are arranged between the two connectors is also odd. We would be tempted to put all the binary inputs on one connector and the outputs on the other connector, starting with pin 1 for the first channel and continuing in pairs (1-20, 2-21, etc.). If we use twisted ribbon cable, the pairs will match up with the pairs in the cable. These are binary signals so there's no real reason to skip lines between the channels.
2. On J4 we recommend connecting the unused lines to GND.
3. The power connector is an IDC style, which is not appropriate for long term stability and safety. (This has been mentioned before in the other test report summaries.)
4. Put low value resistors in the feedback path of unity gain followers. The slew rate of the AD734 is relatively slow at 2.8V/us and this could lead to problems. Considering the bandwidth of the driver in low noise mode it's probably not a performance issue as much as a best-practice recommendation.
5. We like the independent readback circuit for switching the filters.
6. We like having a slow and fast current sense circuit. That will be very useful.
7. We found a solder bridge on channel 1 between R7 and R8 of the driver board. We also found that R30 on channel 4 of the monitor board had been jumpered out. These and similar production related issues will need a good QA program.
8. The rms monitor did not seem to work as expected and its dynamic range came into question.

2.3 Cosmetic

1. The boards had a good proliferation of testpoints. The addition of more GND connections on the board should be considered. One for the whole board made testing a bit awkward.
2. Some of the diode and capacitor footprints are wrong.
3. There are minor errors on the footprint for J1 on the monitor board. The holes for the board locks are too small.
4. The chassis has a very nice, clean layout.
5. Move the monitor board LEDs to the back panel. That way there will be LEDs on the front and rear of the chassis.
6. There needs to be heat shrink insulation on the exposed wires in the chassis on the 3W3 connector and on the switch.
7. Move the 3W3 connector to the other side of the switch. The wiring will be a little bit cleaner that way.
8. Update the chassis to our newer chassis and front panels.
9. Create a chassis drawing or assembly drawing to detail what goes where.
10. The colors used for the wiring does not match the “LIGO standard”. In particular black for the DC return is not used. (The establishment of color codes for wiring is in some dispute; however we recommend, for consistency with past use, the codes recommended in T080034, the Top Test Mass Driver report.)
11. The connectors on both boards are nicely labeled. We encourage a more permanent marking in the field versions, such as silk screening, engraving, or laser etching.

2.4 Adequacy of Documentation

The documentation was incomplete, only a bare set of schematics was provided. No bill of materials, layout or assembly drawings, test plans, test results, quick start guide or other documentation was provided. Prior to production all materials listed in Electronics Requirements document (T060067) and LIGO document T000053-04-D, “Universal Suspension Subsystem Design Requirements Document” need to be supplied.

2.5 Misc Comments

DC Bias Return: The lack of a DC path for the bias currents of IC4 and IC8 on the driver board should be addressed and resolved. For example, a 1 M ohm resistor parallel to jumper W2 would eliminate the bias question and would not contribute to the differential output noise.

3 Performance

Performance of the chassis was measured using the set of tests described in LIGO document T080021-00-C. The completed report is included in Appendix A. The categories are dynamic range, transfer function, monitor, noise, and cross talk. The sections below summarize the tests results.

3.1 Dynamic Range and Transfer Function Tests

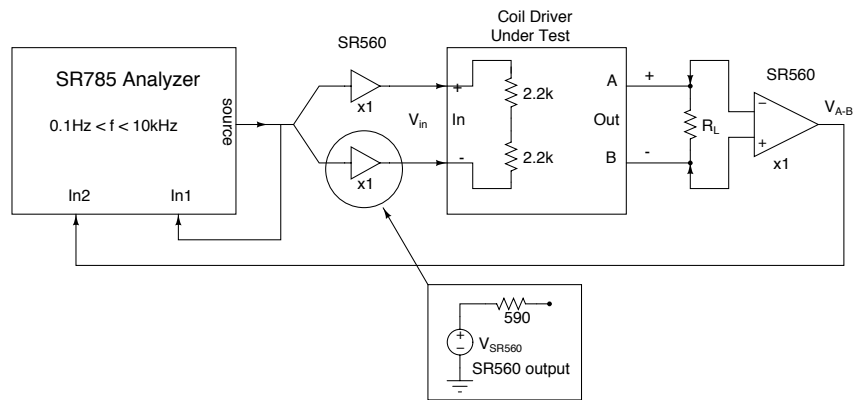


Fig. 1 Test set up for transfer function measurements. There is a correction for the input impedance of the driver loading the SR560 output. The voltage divider formed by the series 590 ohm resistor in the output of the SR560 and the 2k ohm input resistance of the UIM driver board result in a 0.79 factor or -2.06 dB correction of the input voltage.

3.1.1 Dynamic Range

All channels meet the dynamic range requirements in DC tests of being capable of supplying 2mA into a 19.6 ohm load.

3.1.2 Transfer Functions

The transfer functions for each channel of the UIM Driver were measured with resistive loads of 19.6 ohms. The output was measured across the load resistor. The test setup is shown in Fig. 1. The test signal for the differential input was formed by splitting the output of the SR785 using two SR560 amplifiers, each with unity gain. This doubles the input signal in relation to the reference signal into the SR785 analyzer. The 2.2k input resistance of the UIM Driver loads the 590 ohm output resistance of the SR560 amplifier. The input to the Driver channel is reduced by the voltage divider in the ratio $2200/(2200+590)=0.79$. The combined corrections of the factor two from the single to differential input and the factor of 0.79 from the loading of the SR560 by the input circuit of the driver board amounts to 3.97 dB correction. This brings the simulation and the measured values into good agreement, as shown in Fig. 2 for the high dynamic range

mode and Fig. 4 for the low noise mode transfer functions. Residual deviations appear to be consistent with component tolerances.

3.1.3 High Dynamic Range Transfer Function

The High Dynamic Range mode is defined as the configuration of the driver board with all gain control relays de-energized. Table 1 below lists the nominal and measured magnitude ratio (in dB) and phase of input to output. In order to convert from a voltage ratio, which is what is read out from the SR785, to a transfer resistance the value of the load resistor must be divide out. This is also shown in table 1.

Table 1: Channel 1 Transfer Function Measurements, High Dynamic Range Mode

Freq (Hz)	Nominal Gain [dB(amps/Volt)]	Nominal Phase (Degrees)	Actual Gain† [dB(Volt _{out} / Volt _{in})]	Actual Phase (Degrees-180)
0.1	-76.2	178.2	-46.4 (-29.8=76.2)	-0.81
1	-76.2	180.7	-46.3 (-29.8=76.1)	0.98
10	-76.2	189.5	-46.2 (-29.8=76.20)	9.79
100	-70.4	237.0	-40.1 (-29.8=69.9)	57.8
1K	-52.5	241.4	-22.1 (-29.8=51.9)	58.59
10K	-45.3	191.2	-15.5 (-29.8=45.3)	1.22

†Subtract $20 * (\log(2) + \log(19.6) + \log(0.79)) = 6.02 + 25.85 - 2.06 = 29.8$ to convert to dB[amps/volt]. The number listed in the table was the number readout on the SR785. See the text for details.

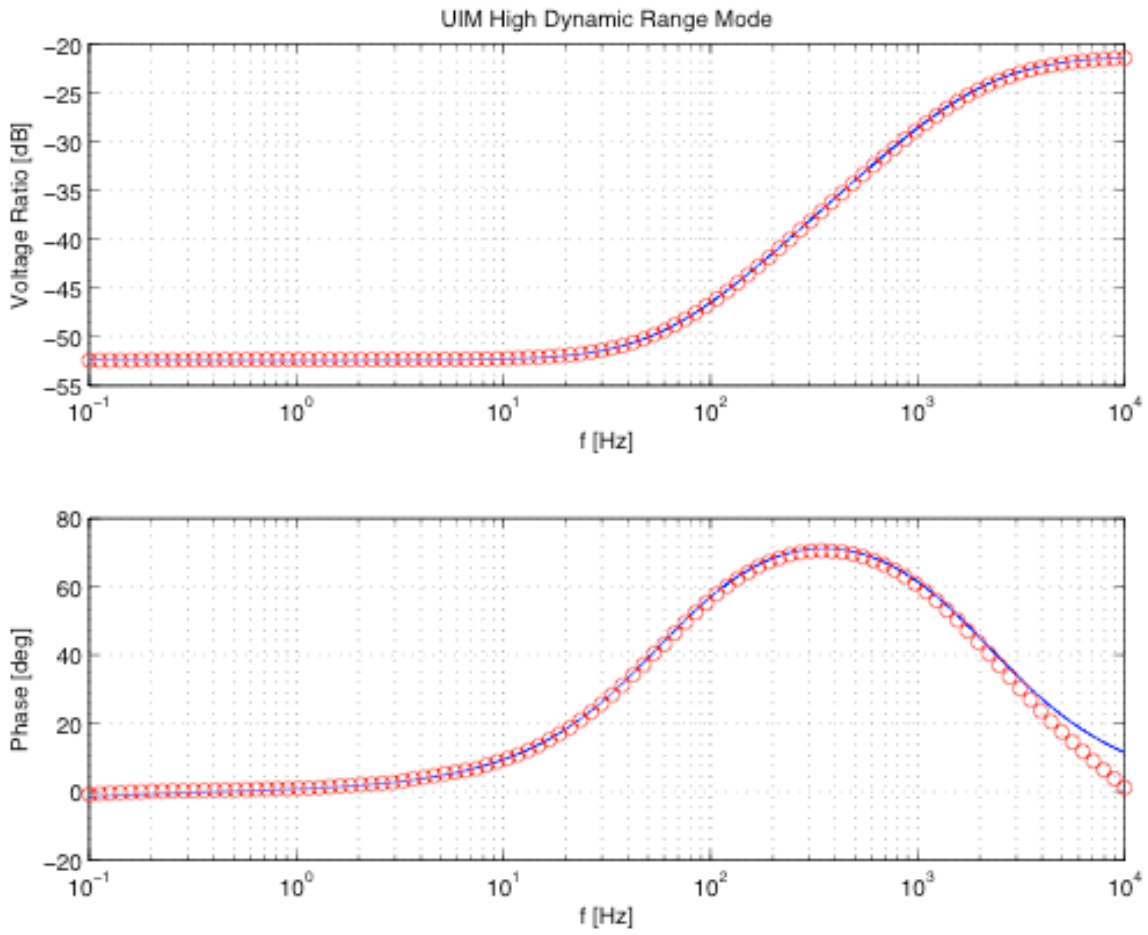


Fig. 2 Transfer function for the UIM driver in high dynamic range mode. The measured values are shown as red circles. The solid blue curve is the spice simulation. Agreement is seen to be very good. The voltage ratio is plotted in dB. To convert to the values appropriate for a transresistance transfer function, divide the output voltage by the load resistor, which was 19.6 ohms for these tests; i.e., subtract 25.85 dB.

The simulation data was produced from a spice model based on the schematic shown below in Fig. 3.

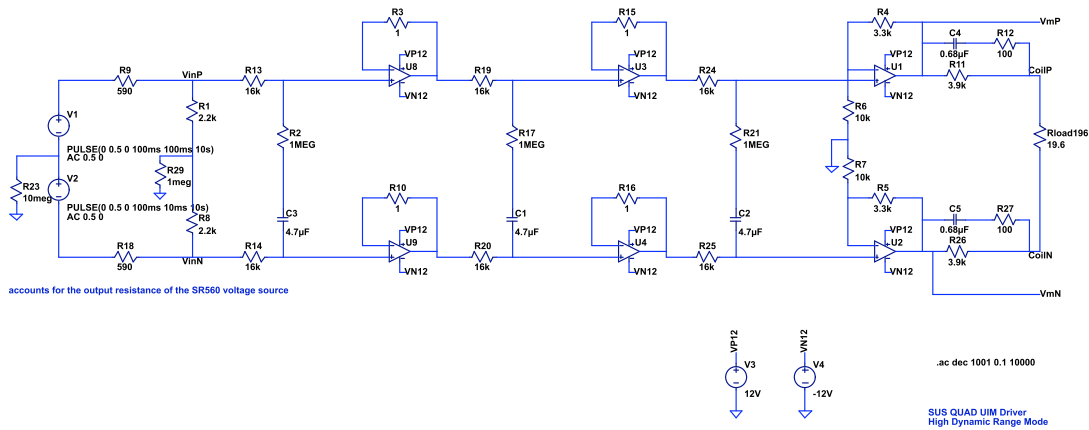


Fig. 3 Schematic diagram of the spice simulation for the High Dynamic Range case. For his case all the relays switching the intra-stage filter setting resistors were de-energized.

3.1.4 Low Noise Mode

The Low Noise mode is defined as the configuration of the driver board with all gain control relays energized. Table 2 below lists the nominal and measured magnitude ratio (in dB) and phase of input to output. In order to convert from a voltage ratio, which is what is read out from the SR785, to a transfer resistance the value of the load resistor must be divide out. This is also shown in table 2.

Table 2: Channel 1 Transfer Function Measurements, Low Noise Mode

Freq (Hz)	Nominal Gain [dB(amps/Volt)]	Nominal Phase (Degrees)	Actual Gain† [dB(Volt /Volt)] out in	Actual Phase (Degrees+180)
0.1	-75.5	163.9	-25.9 (-49.8=75.7)	-15.5
1	-84.9	58.8	-35.4 (-49.8=85.2)	-122.8
10	-127.9	68.9	-78.6 (-49.8=128.4)	-106.3
100	-131.2	221.1	-81.7 (-49.8=131.5)	41.4
1K	-113.4	239.8	-63.3 (-49.8=113.1)	57.1
10K	-106.2	191.0	-56.8 (-49.8=106.6)	7.3

†Subtract $20 * (\log(10) + \log(2) + \log(19.6) + \log(0.79)) = 6.02 + 25.85 - 2.06 = 49.8$ to convert to dB[amps/volt]. The number listed in the table was the number measured on the SR785.

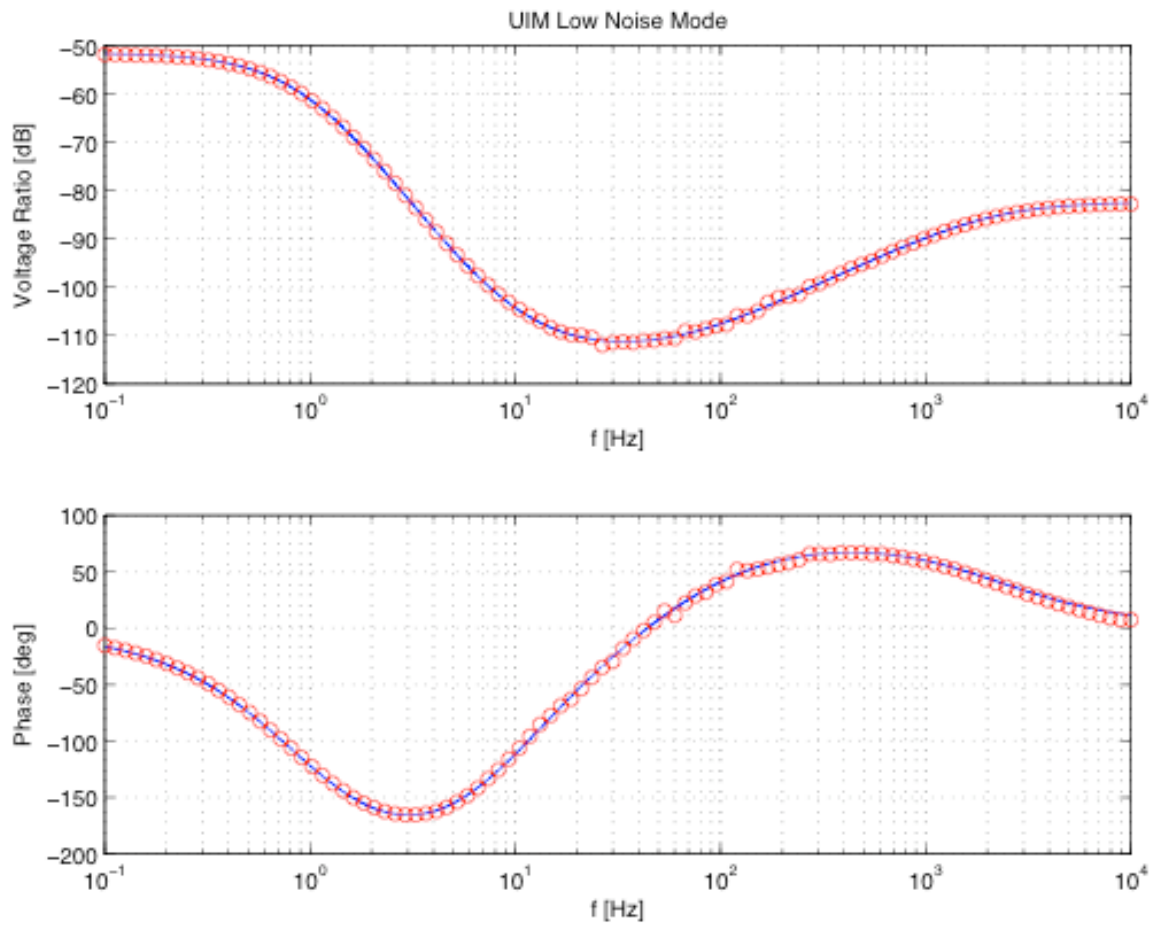


Fig. 4 Transfer function for the Low Noise driver in high dynamic range mode. The measured values are shown as red circles. The solid blue curve is the spice simulation. Agreement is seen to be very good. The voltage ratio is plotted in dB. To convert to the values appropriate for a transresistance transfer function, divide the output voltage by the load resistor, which was 19.6 ohms for these tests; i.e., subtract 25.85 dB.

The simulation was produced from a spice simulation based on the schematic shown below.

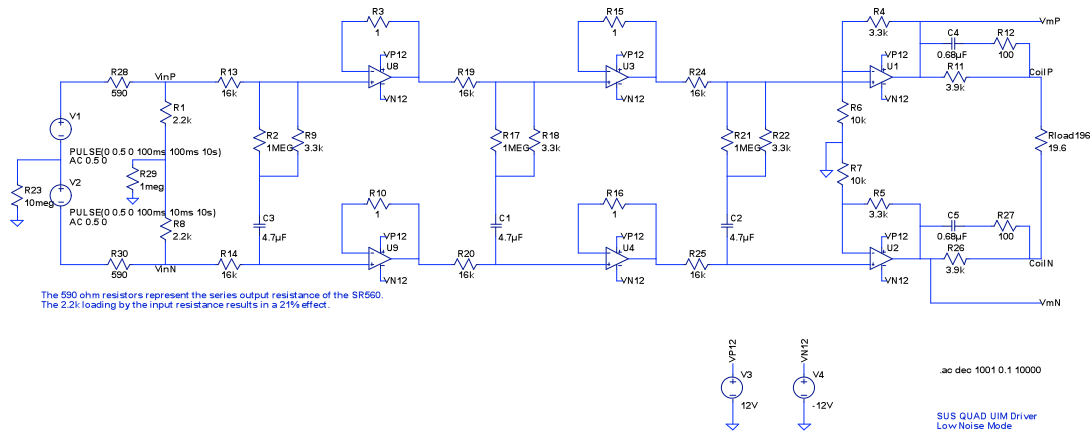


Fig. 5 Schematic for the spice simulation for the low noise mode.

The low noise mode has all the intra-stage relays energized, which selects the shorter time constant RC networks.

3.2 Driver Noise and Dynamic Range Measurements

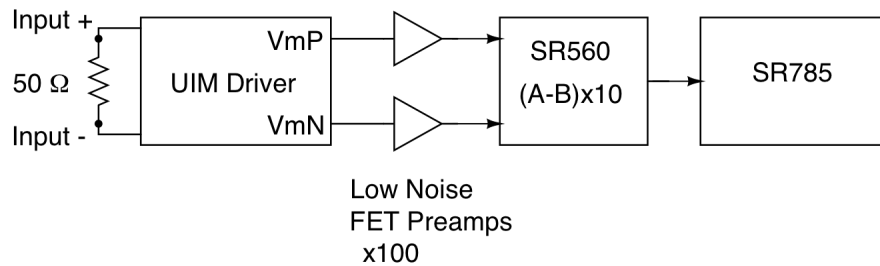


Fig. 6 Test setup for noise and dynamic range measurements of the UIM driver board. The low-noise preamp (~ 1 nV/ $\sqrt{\text{Hz}}$) [LIGO-D060205] and the SR560 provide a gain of x1000 to extend the SR785.

3.2.1 Driver Noise

The noise requirements for the low noise mode of operation (specified as the more conservative SRD state) are outlined in T060067. The summary table was shown in the introduction of this document. The noise is given in units of current spectral density. Measuring this low of a current noise directly is very difficult. For these tests we measured the output voltage noise of the driver at the test points before the RC-network in the output stage and the current noise was inferred by dividing the measured voltage by the load impedance at the frequency of interest. A plot of this impedance is shown in Fig. 7.

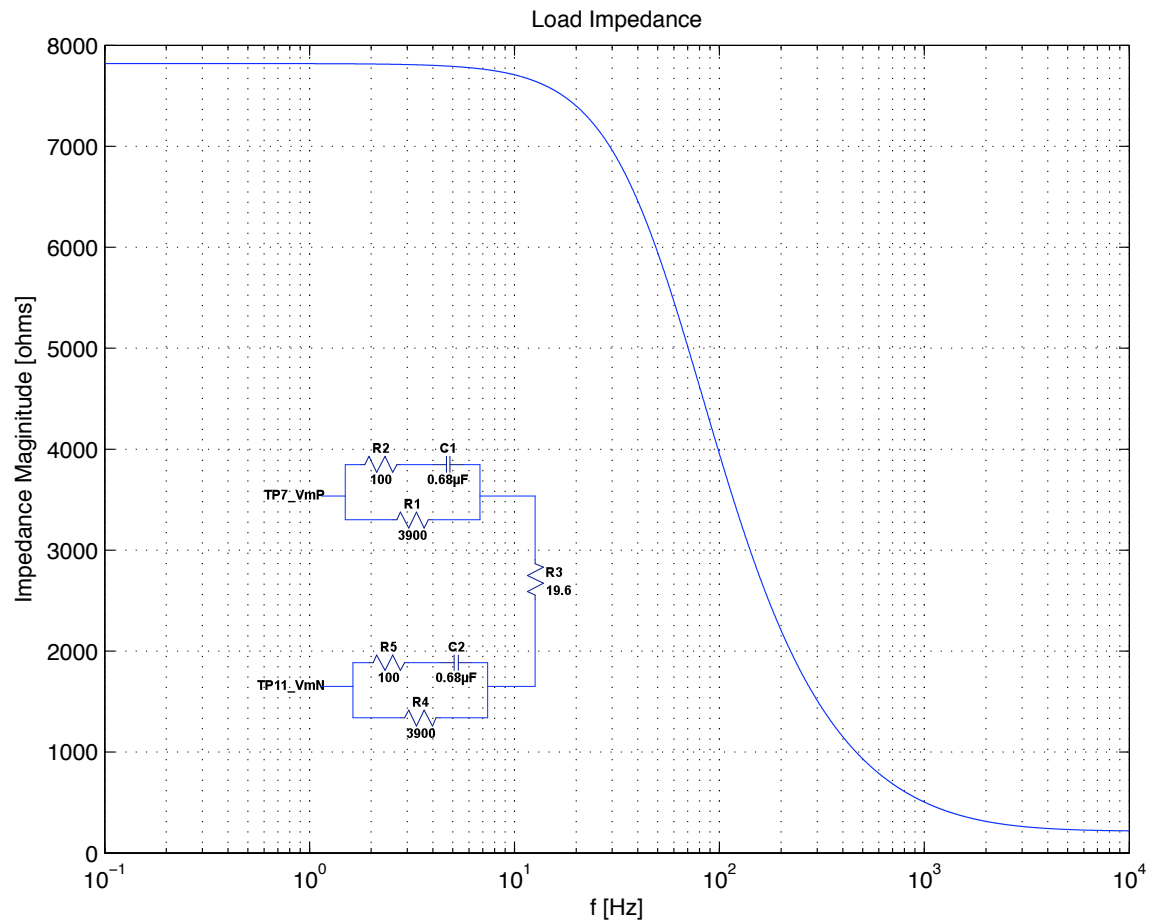


Fig. 7 Magnitude of the Driver load impedance as seen from the monitor points VmP and VmN of the Driver circuit. At 10 Hz the magnitude is 7.7k ohms.

Assuming a 19.6 ohm coil load and the particular design values chosen by the University of Birmingham, the noise requirements in terms of output voltage noise can be calculated for each of the frequencies in the table. We have ignored the effect of the OSEM coil inductance and compare the test and simulation results for a purely resistive load of 19.6 ohms. The voltage noise requirements are shown in the table below.

Table 3: Voltage referred noise requirements

Frequency	Voltage Noise Requirement
1 Hz	$0.500 \text{ nA}/\sqrt{\text{Hz}} * 7850 \text{ ohms} = 3.9 \text{ uV}/\sqrt{\text{Hz}}$
10 Hz	$3 \text{ pA}/\sqrt{\text{Hz}} * 7700 \text{ ohms} = 23 \text{ nV}/\sqrt{\text{Hz}}$
100 Hz	$200 \text{ nA}/\sqrt{\text{Hz}} * 3900 \text{ ohms} = 780 \text{ uV}/\sqrt{\text{Hz}}$
1000 Hz	$1000 \text{ nA}/\sqrt{\text{Hz}} * 500 \text{ ohms} = 500 \text{ uV}/\sqrt{\text{Hz}}$

The plots in Fig. 8 show the measured and simulated output noise versus frequency for the UIM Driver. The simulated noise data was generated using spice simulation software from Linear Technologies, Inc. using an improved noise model in the op-amps.

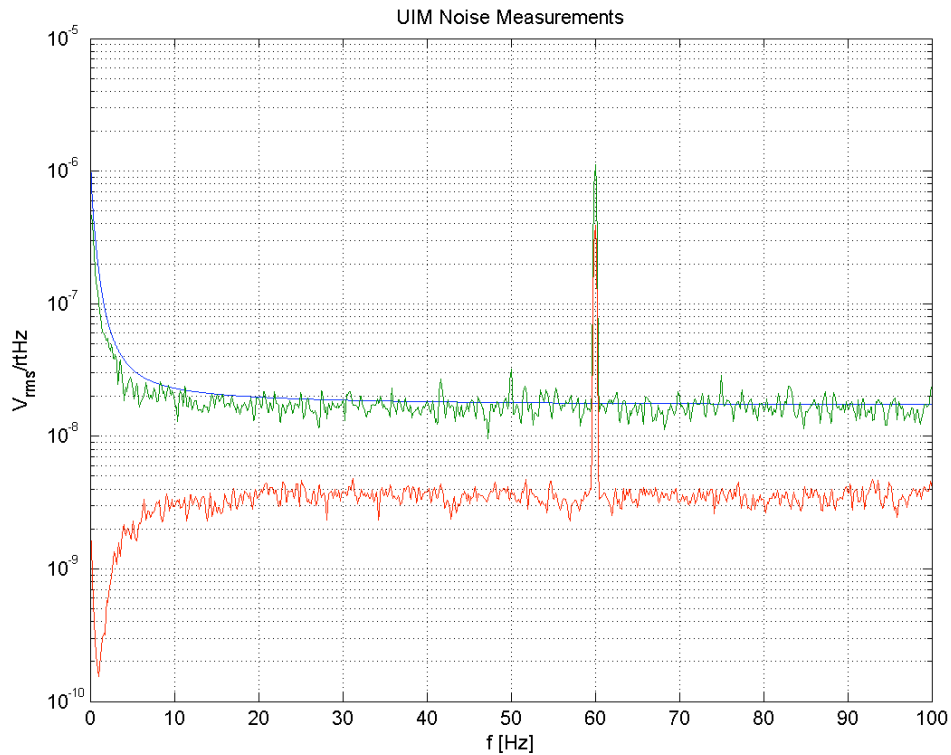


Fig. 8 Driver noise measurements and comparison with spice simulation. Note the test setup had a x1000 preamp in front of the SR785. The spice simulation used conservative noise models for the opamps, which slightly over estimates the corner noise for frequencies below 10 Hz. The drop in the baseline noise for frequencies less than 10 Hz is an artifact of the capacitive coupling used in the test set up for this particular measurement and should be ignored. The trace legend is: Red: Test setup baseline noise, Green: Driver Output noise, Blue: Spice simulation

3.3 Monitor Board

Measurements of the monitor board's transfer function and noise are shown below.

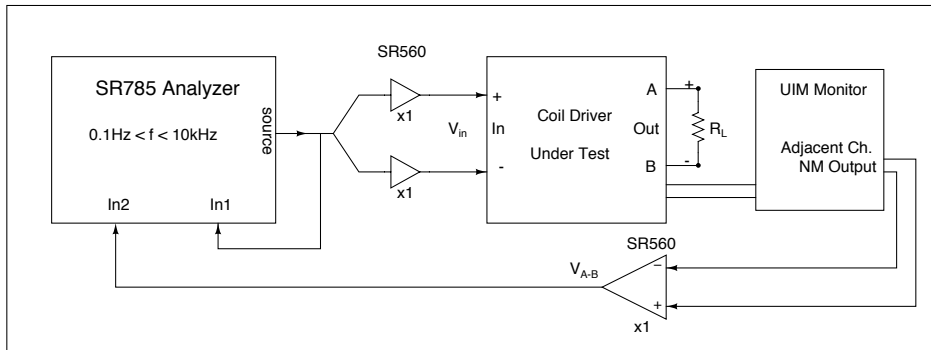


Fig. 9 Test setup used to determine adjacent channel crosstalk. The output was measured through the monitor board.

3.3.1 Noise Monitor Transfer Function

The transfer function from the input of the driver to the output of the noise monitor circuit was measured. A plot comparing the expected transfer function with measured data is shown in Fig. 10.

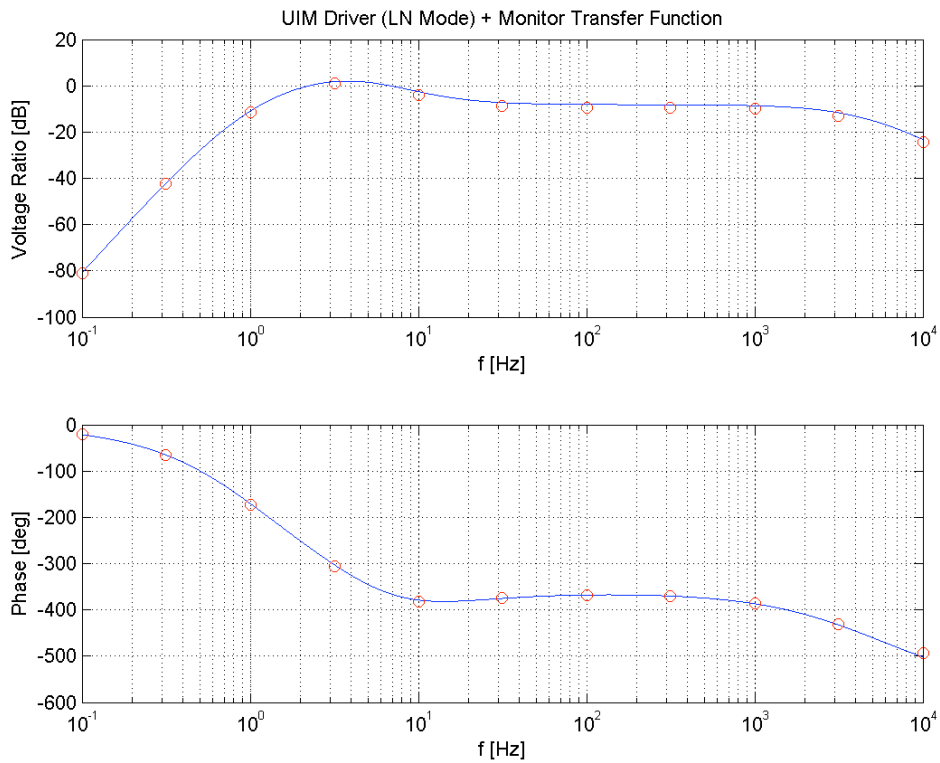


Fig. 10 Combination Driver and Monitor boards cascaded to measure the combined transfer function. The red circles are measured data and the blue lines are spice simulations.

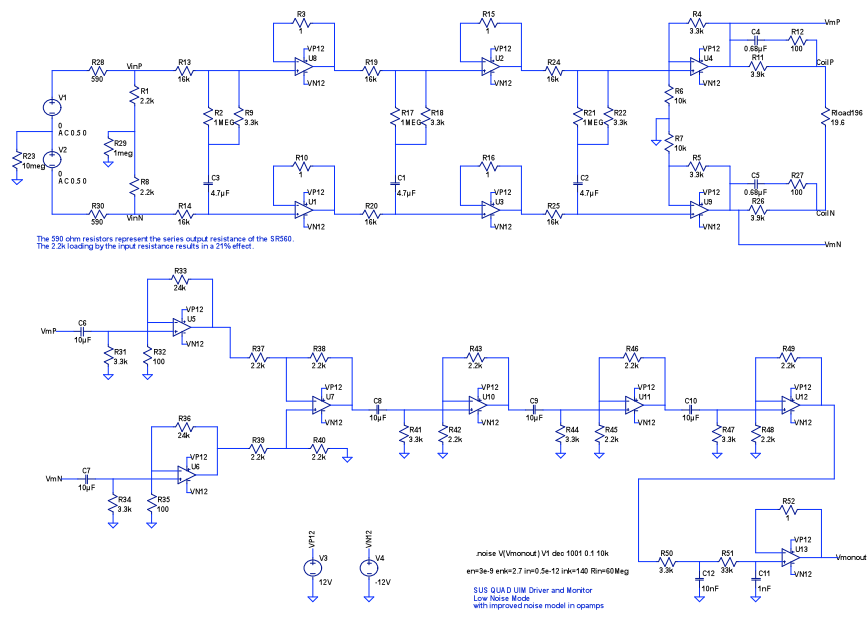


Fig. 11 Spice schematic documenting the simulation of the combined driver card connected to the monitor card. The Driver board is in the “Low Noise” mode.

The monitor board also provides rms capability through the AD736 IC. This chip provides an analog computation of an averaged rms voltage. The measured results show a distinct error of a factor of ~10 and this sub-circuit may need some tweaking. For the full dynamic range, the input attenuator to the AD736 will need to be adjusted to prevent exceeding its 200mV maximum input.

3.3.2 Monitor Board Noise Measurements

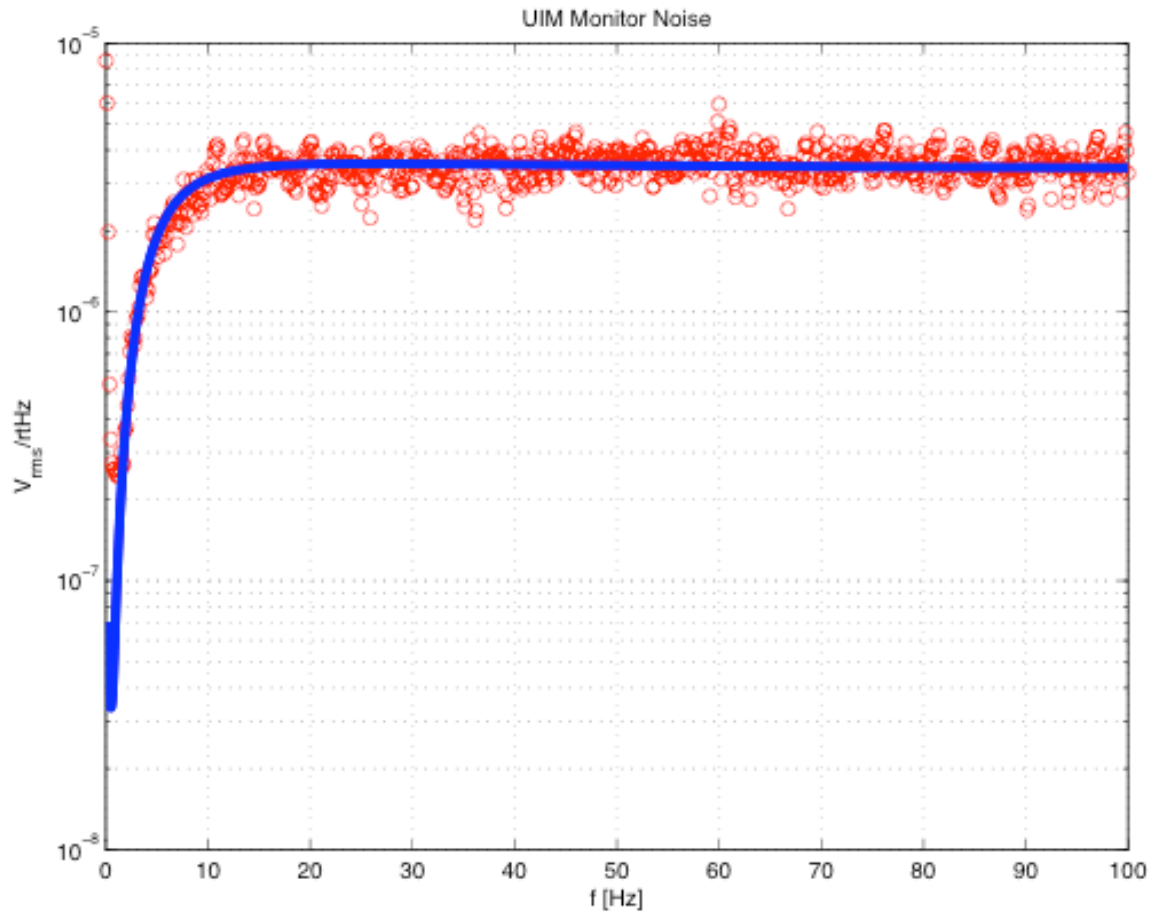


Fig. 12 Monitor board noise measurements in low noise mode. The red circles are data and the solid blue line is the simulation. The schematic of the simulation is shown in Fig. 11.

3.4 Cross-Coupling

The cross coupling between adjacent channels on the driver board was measured using the procedure in section 3.3 of the test plan. The plot below shows the typical coupling observed from the input of one channel to noise monitor output of the adjacent channel.

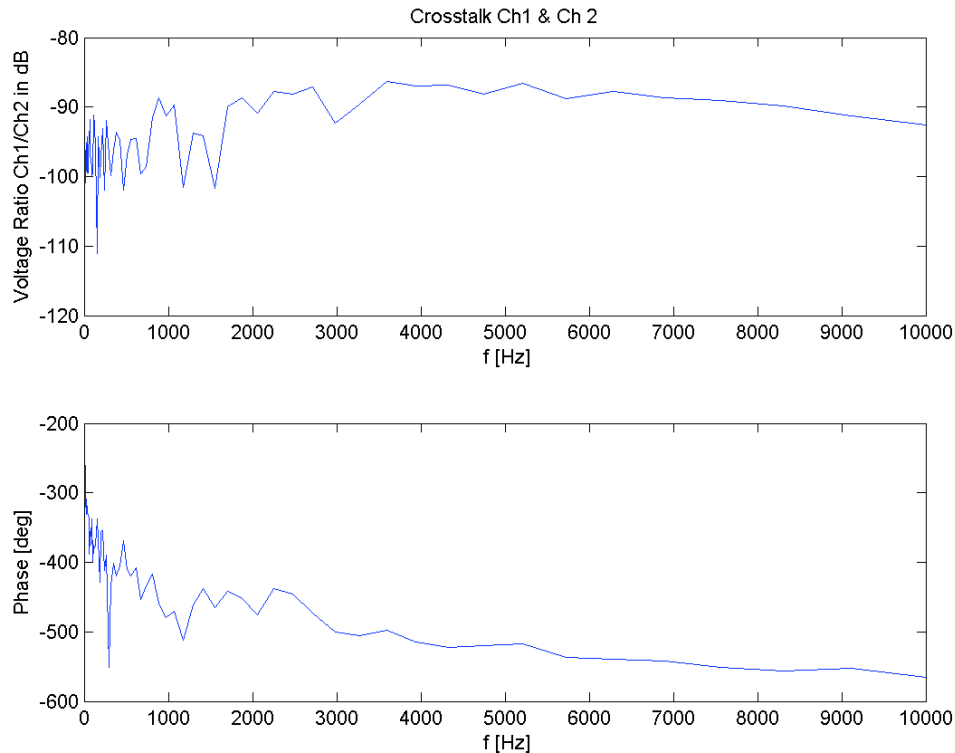


Figure 13 Cross coupling measurement between adjacent channels of the combination driver and monitor boards.

3.5 Mode Switching and Glitch Tests

The design of the Top Driver provides for one relay that can be used to switch each channel from what can be called “acquire” mode to a lower noise “run” mode. The design is such that the relay can be switched using either a set of contacts or an open-collector output from the US provided control system. The design also uses another set of contacts from the mode switch relay (K3) to monitor the relay position. The design meets the requirements called out in the Suspension Universal Design Requirements document (T000053).

An attempt was made to measure any glitches or transients in the current output of the driver caused by the switching of relay K3. These tests are described and the results documented in section 3.4 of the test plan. During the tests glitches were observed across the load. The glitches were very small (50 mV) and fast (2 usec) impulses. They carried little energy, but were noted here for the sake of completeness. The switching time of the relays used on the board was found to be approximately 1milli-second and consistent from channel to channel. This is significantly better than the maximum 3 milli-seconds specified by the manufacturer of the relay. However, we do not have a sufficient lifetime test to determine the long term stability of the delay.

Additional tests should be conducted once the entire electronics package has been assembled to control the Noise Prototype suspension at LASTI. These tests should include:

- A more sensitive test for glitches possibly using an optical cavity
- A test of the ability to coordinate the switching of a hardware mode switch with a software

compensation filter. An optical cavity would also be useful during these tests.

3.6 “Glitch” tests of relay transitions

Fig. XXX Test setup for glitch measurements, illustrating what the test setup was at the time. The loa for these tests was a 1mH inductor, with an internal 40ohm series resistance, to more closely simulate the actual setup in the field.

Ch 1 is the control signal that energizes relay 3. Ch 2 shows the contact closure. Ch 3 is the voltage x 100 (effectively 20 mV/Div because of the gain of 100 in the SR560) across the load inductor, which in this case was 1 mH and 40 ohms. The transient induced by the inrush current is seen on Ch 3 in the lower left image. The change in mirror momentum by this impulse is expected to be small and of negligible consequences, but a detailed evaluation of such impulses needs to be carried out. The closure of the contacts is seen in the illustration on the lower right. Some mild contact chatter is seen. This is of negligible effect on performance, of more concern is the long (~800 usec) delay between the assertion of the control signal (Ch 1's falling edge) and the closure of the contacts.

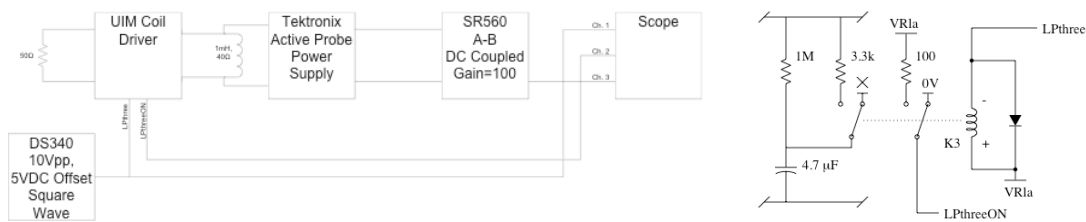


Fig. 14 Test setup to measure relay switching transients. An idealized version of the relay circuit are shown in the schematic on the left.

The oscilloscope traces shown in Fig. 15 illustrate the glitches that occur when the coil in the relay is energized and when the relay contacts close. For these tests the load was an 1 mH inductor with 40 ohms of equivalent series resistance. For investigating transients it was thought an inductor would be a more realistic choice for the load and highlight any glitches. The large frame image provides an overall view of what's going on and the time scale involved, 200 us/div. It takes 1msec for the relay to respond once you send a the signal to switch. The lower left image shows the first part of the switching process. Here you can clearly see the spike that's seen across the inductor. Taking into account the DC resistance and gain of the SR560 this works out to ~1mA of current through the load inductor. In the right image there's a smaller transient when the relay contacts actually close, but it's considerably smaller than the first one. Because we see this before the relay actually engages we believe we are seeing a transient from the relay coil charging, but these explanations are preliminary. The relay contacts chatters quite a bit when it closes. This is in addition to the glitches from the coil energizing.

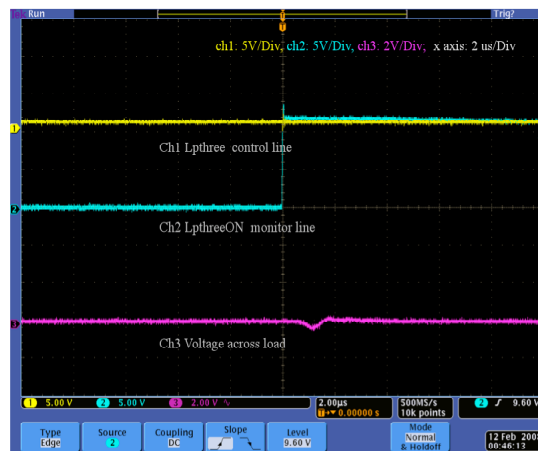
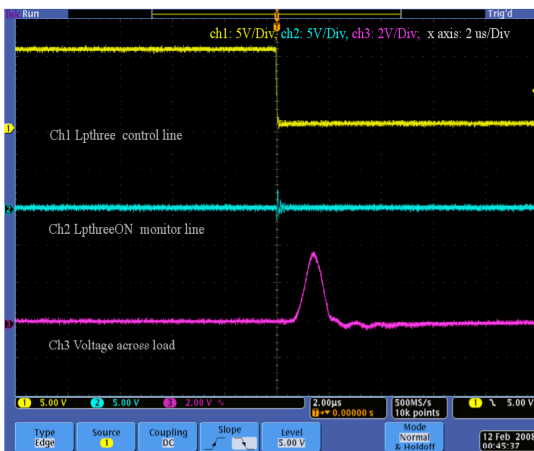
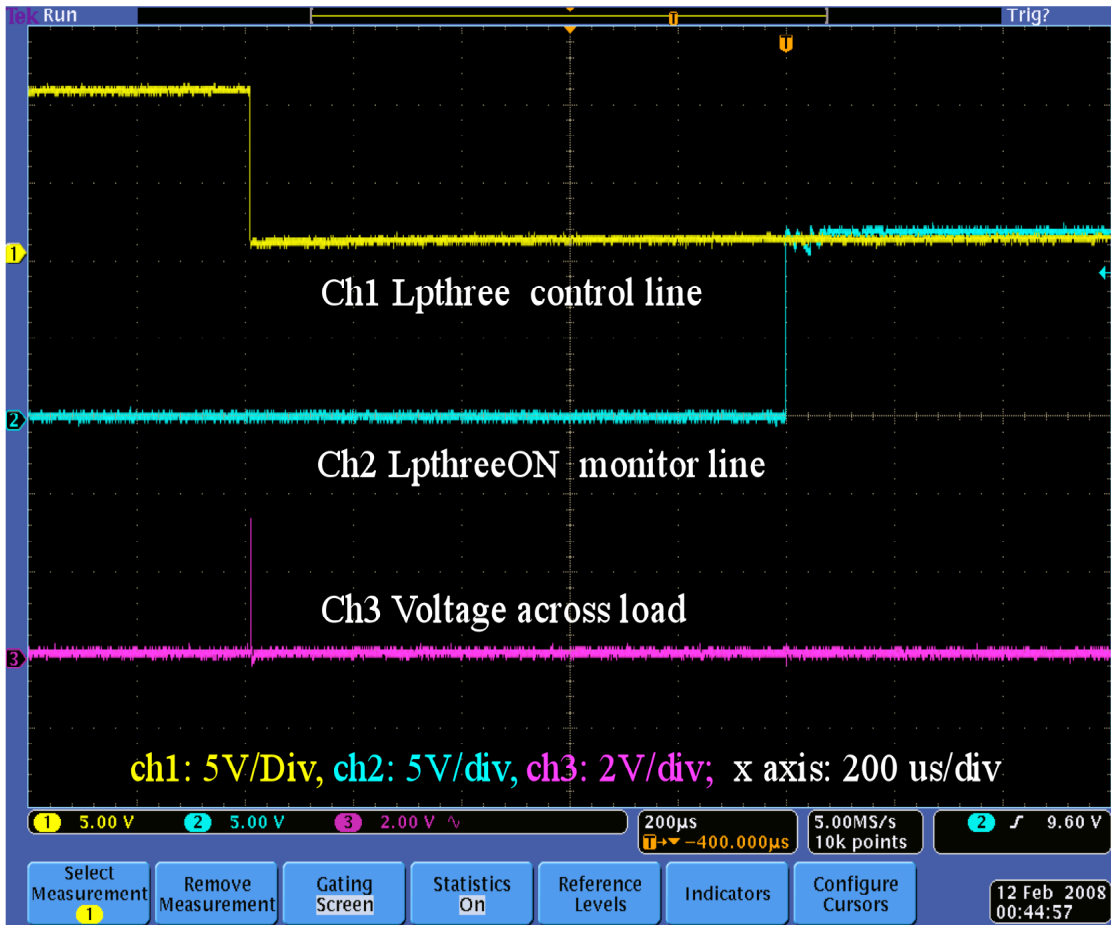


Fig. 15 Glitch-test oscilloscope traces of the relay-3 control signal, relay-3 contact closure, and the voltage across the load. For these tests the load was a 1mH inductor with a series equivalent resistance of 40 ohms. The lower right oscilloscope image shows the details of the energizing coil. The lower left image shows the details of the contact closure. The time between the energizing of the relay coil and the contact closure is 1ms, as may be seen in the top image.

4 Appendix

COPY TEST PROCEDURE: UIM COIL DRIVER & MONITOR First Article.

Serial Number: UIMD 1

Date: 2008-FEB-20

Tech: J.M. (Josh Meyer)

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<i>W. Heffner Josh Meyer</i>		

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1 Introduction

The tests described below will be utilized to test the first production prototype of the AdL Quad Suspension UIM Coil Driver. These drivers are being designed and built by the UK group located at the University of Birmingham. The design requirements for the driver can be found in LIGO document number T060067-00-C, "AdL Quad Suspension UK Coil Driver Design Requirements".

These tests are not comprehensive and will only be utilized to verify that the driver meets the design requirements. It is assumed that the drivers have been thoroughly tested by the University of Birmingham prior to shipment.

2 Test Equipment

- Stanford Research SR785 analyzer
- Voltmeter
- Oscilloscope
- Board Schematics- TBD

*3x SR 560
Add Drivers?
VS 340
SR 650*

*Power draw?
Input Voltage?
±16.5 @ 0.65A each*

3 Tests

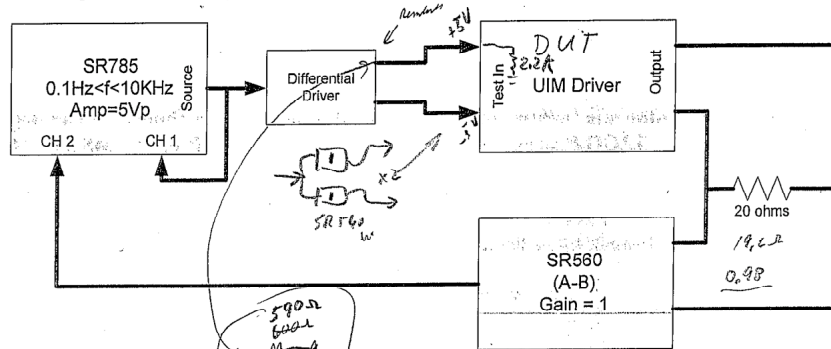
The tests are broken into the same categories used in the design requirements document, noise, dynamic range and monitors/controls. The tests for each of these categories are described in the sections below.

3.1 Dynamic Range and Transfer Function Tests

Each channel of the UIM coil driver is equipped with three relays that are used to change the response from a very high dynamic range high noise to a low dynamic range, low noise response. In reality, these relays (K1, K3 and K4) are switched in one at a time, but in the interest of conserving test time only the extremes of the four possible modes are tested. The high dynamic range mode does not have any of the relays energized and the low noise mode has all relays energized. The tests for each of these two modes are described in the sections that follow. Note that it has been assumed that the actual response of each individual mode has been tested by the UK group prior to delivery of the unit. The transfer function for each mode of operation is measured by injecting a signal into the test input of a channel and measuring the current through a 20 ohm resistor connected across the corresponding channel output. Measurements are made for frequencies from 0.1Hz to 10KHz. A block diagram of the test setup is shown in the figure below.

8 modes - 2

*19.6
for these tests*



*590Ω
600Ω
M
Q_{nom}
SR 560
OUTPUT*

Trans. Fcn. Test setup

$$\Rightarrow \frac{2200}{2200 + 590} = 0.79$$

0.79

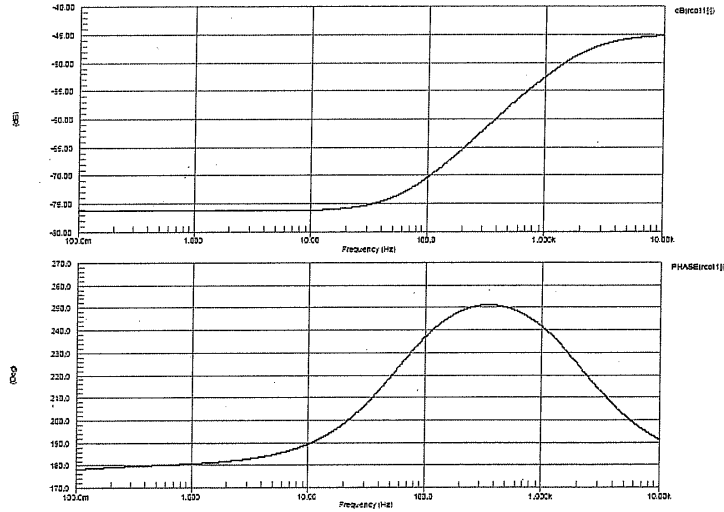
Serial Number: _____

Date: _____

Tech: _____

3.1.1 High Dynamic Range Mode

In the high dynamic range mode, relays K1, K3 and K4 are NOT energized. The nominal response of the coil driver this mode is a zero at 60Hz and a pole at 2.3KHz and is shown in the plot below. Note that the transfer function is in units of volts in to amps output into a 20 ohm load. *in dB/V to 1V*



Recorded base circuit number removed of the SR 785 analysis

In the tables below, record the measured magnitude and phase of the response for each channel. In addition, save the transfer function for one representative channel to disk and record the file name in space provided below.

Table 1: Channel 1 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-76.2	178.2	-46.56	-0.82
1	-76.2	180.7	-46.73	0.92
10	-76.2	189.5	-46.23	9.18
100	-70.4	237.0	-48.23	66.32
1K	-52.5	241.4	-22.76	60.76
10K	-45.3	191.2	-15.48	-16.7

SR 5001

Volts into

*Acceptable range for measurements?
6.02 dB from SR 5605 &
19.6 ohm resistors not accounted for (-31.87 dB total)*

Table 2: Channel 2 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-76.2	178.2	-46.88	3.84
1	-76.2	180.7	-46.80	0.94

$\frac{2200}{2200 + 590} =$

$20 \log_{10}(2) + 20 \log_{10}(19.6) = 6.02 + 25.85 = 31.87 \text{ dB}$

x2 on input to deriv differential inputs *output resistor load (be measured volts)*

Serial Number: _____

Date: _____

Tech: _____

10	-76.2	189.5	-46.81	9.4
100	-70.4	237.0	-41.01	56.78
1K	-52.5	241.4	-23.17	59.02
10K	-45.3	191.2	-16.12	-11.5

Table 3: Channel 3 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-76.2	178.2	-46.45	-0.81
1	-76.2	180.7	-46.75	0.97
10	-76.2	189.5	-46.75	9.57
100	-70.4	237.0	-40.84	57.13
1K	-52.5	241.4	-23.08	58.62
10K	-45.3	191.2	-16.08	-11.83

Table 4: Channel 4 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-76.2	178.2	-46.42	-0.82
1	-76.2	180.7	-46.34	0.94
10	-76.2	189.5	-46.23	9.47
100	-70.4	237.0	-40.35	56.98
1K	-52.5	241.4	-22.54	59.83
10K	-45.3	191.2	-15.45	0.41

File Name for transfer function measurement (High Dynamic Range Mode): SV5002.T8V

Channel No. 1
3.1.2 Low Noise Mode

In the acquire mode, relay K1, K3 and K4 are energized. The nominal response of the coil driver in low noise mode is three poles at 1Hz, three zeros at 10Hz, one zero at 60Hz and one pole at 2.3KHz. The nominal response is shown in the plot below. Note that the transfer function is in units of volts in to amps output into a 20 ohm load.

$$H : \left[\frac{\text{amps}}{\text{volts}} \right]$$

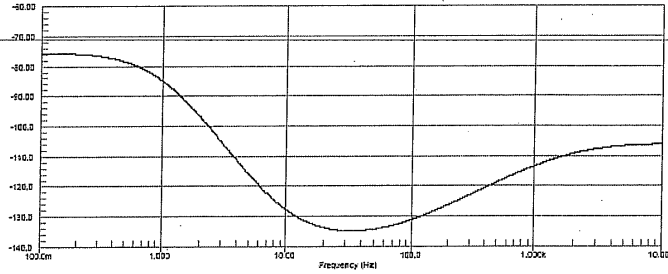
Serial Number: _____

Date: _____

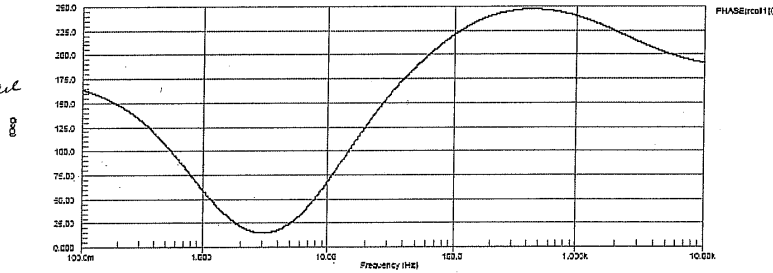
Tech: _____

low noise mode

Current through the low mag. dB



phase



In the tables below, record the measured magnitude and phase of the response for each channel. In addition, save the transfer function for one representative channel to disk and record the file name in space provided below.

Table 5: Channel 1 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-75.5	163.9	-26.89	-15.98
1	-84.9	58.8	-38.6	-127.2
10	-127.9	68.9	-76.59	-103.8
100	-131.2	221.1	-78.62	29.29
1K	-113.4	239.8	-64.06	59.35
10K	-106.2	191.0	-56.75	9.25

Table 6: Channel 2 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-75.5	163.9	-26.88	-15.46
1	-84.9	58.8	-34.91	-121.7
10	-127.9	68.9	-77.29	-111.1
100	-131.2	221.1	-81.89	40.71

Added gain of 10 to output SW. Total offset now -51.87 dB.

repeated on next page

$$20 \log_{10}(2) + 20 \log_{10}(19.6) + 20 \log_{10}(10) = 51.87$$

Serial Number: _____

Date: _____

Tech: _____

1K	-113.4	239.8	-68.93	58.99
10K	-106.2	191.0	-56.57	44.8

Table 7: Channel 3 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-75.5	163.9	-26.89	-15.65
1	-84.9	58.8	-36.267	-121.9
10	-127.9	68.9	-79.68	-112.8
100	-131.2	221.1	-80.5	32.5
1K	-113.4	239.8	-53.9	58.47
10K	-106.2	191.0	-56.70	4.89

Table 8: Channel 4 Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBamps/Volt)	Nominal Phase (Degrees)	Actual Gain (dBamps/Volt)	Actual Phase (Degrees)
0.1	-75.5	163.9	-26.89	-15.47
1	-84.9	58.8	-36.12	-121.2
10	-127.9	68.9	-78.49	-81.16
100	-131.2	221.1	-81.54	43.92
1K	-113.4	239.8	-63.87	58.63
10K	-106.2	191.0	-56.75	9.13

SR5001
002
003

File Name for transfer function measurement (Low Noise Mode): SR5003.78V
 Channel Number for saved file: 4 SR5003.78D

Large scale →
current drive
tests

3.1.3 Dynamic Range Tests

The maximum output current requirement for the driver is +/- 2mA_{rms} for frequencies less than 1Hz. The tests below will verify that the design meets this requirement. In addition the chassis and components will be checked for overheating. The tests for all channels should be conducted simultaneously and each test step/reading should be held for a minimum of 5 minutes to allow the temperature of the chassis and components to stabilize. In the tables below, record the output current versus input voltage (DC), note any component heating and if possible the temperature of the component. Output current should be measured across the 20 ohm load resistor connected to the channel under test. In an effort to save test setup and execution time, this test may be conducted in conjunction with the current monitor testing described in section 3.5.3 below.

Table 9: Channel 1 Output Current vs. Input Voltage

Input Voltage	Nominal Output Current (mA)	Actual Output Current (mA)	Notes
+1V	0.17	0.158	
-1V	-0.17	-0.171	
+5V	0.84	0.842	
-5V	-0.84	-0.841	
+10V	1.67	1.678	
-10V	-1.67	-1.681	
+20V	3.35	3.143	
-20V	-3.35	-3.143	

Serial Number: _____

Date: _____

Tech: _____

Table 10: Channel 2 Output Current vs. Input Voltage

Input Voltage	Nominal Output Current (mA)	Actual Output Current (mA)	Notes
+1V	0.17	0.164	
-1V	-0.17	-0.171	
+5V	0.84	0.847	
-5V	-0.84	-0.839	
+10V	1.67	1.680	
-10V	-1.67	-1.680	
+20V	3.35	3.144	
-20V	-3.35	-3.143	

Table 11: Channel 3 Output Current vs. Input Voltage

Input Voltage	Nominal Output Current (mA)	Actual Output Current (mA)	Notes
+1V	0.17	0.163	
-1V	-0.17	-0.170	
+5V	0.84	0.846	
-5V	-0.84	-0.841	
+10V	1.67	1.680	
-10V	-1.67	-1.681	
+20V	3.35	3.143	
-20V	-3.35	-3.144	

Table 12: Channel 4 Output Current vs. Input Voltage

Input Voltage	Nominal Output Current (mA)	Actual Output Current (mA)	Notes
+1V	0.17	0.165	
-1V	-0.17	-0.170	
+5V	0.84	0.845	
-5V	-0.84	-0.833	
+10V	1.67	1.680	
-10V	-1.67	-1.677	
+20V	3.35	3.143	
-20V	-3.35	-3.141	

3.2 Noise Tests

SR5004
005
006

The most stringent noise requirement for the UIM Driver comes at 10Hz where the output noise current from the driver needs to be less than 3 pA/√Hz. Measuring the actual noise current into the 20 ohm load resistor is a very difficult measurement, so the noise current must be implied by measuring the output noise voltage of the driver using test points on the board (TP7 and TP11). The total series impedance in the output of the driver including the 20 ohm load is 7.8 Kohms at 10Hz. The means that the output voltage noise measured between TP7 and TP11 needs to be less than 23.4nV/√Hz at 10Hz. A plot of the simulated noise versus frequency is shown in the figure below.

Actual Low Noise Voltage

Johnson noise of the 20Ω resistor

$$v_n(\text{Johnson } 20\Omega) = \sqrt{1\Omega \times 27^\circ} \cdot \sqrt{20(\Omega)} = 130\text{pV} \times 4.472 = 581 \times 10^{-12}\text{V}$$

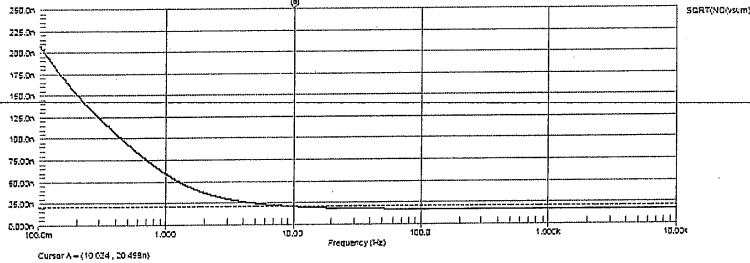
$$= 580\text{pV}/\sqrt{\text{Hz}}$$

$$i_n(20\Omega) = 29\text{pA}/\sqrt{\text{Hz}}$$

Serial Number: _____

Date: _____

Tech: _____



Noise tests are back page of Admin report.
 diff. of approx.
 f: 0.1 - 100 Hz f_{max} = 100 Hz
 " 0.01 - 1 kHz " = 1.66 Hz
 " 0.005 " 0.06
 " 0.006 " 2.5 Hz

The simulation predicts that the noise at 10Hz should be approximately 20.5nV/√Hz. In the table below, record the output noise at 10Hz measured between TP7 and TP11 for each channel. The inputs to the channel under test should be tied to circuit ground and relays K1, K3 and K4 should be energized (Low Noise Mode). In addition, save the noise data for one representative channel to disk and record the file name in space provided below. The frequency range for the saved file should be from 0.1Hz to 100Hz.

Channel Number	Measured Noise at 10Hz
1	27.4 nV/√Hz 18.62 nV/√Hz
2	27.92 18.92
3	23.03 20.86
4	20.68 18.86

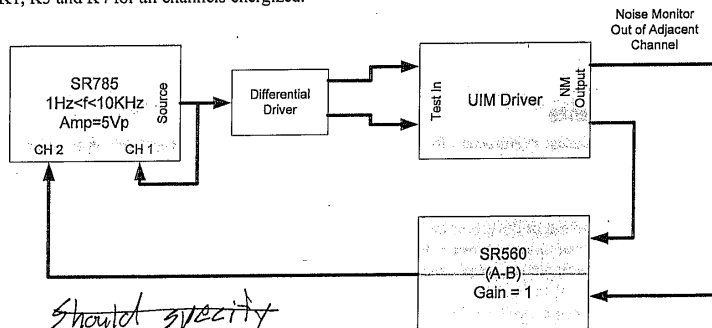
File Name for noise measurement (Low Noise Mode): *SR5004, 5, 6* settings: *SR5001, 785*
 Channel Number for saved file: 1

~~Baseline: SR5008, 9, 10~~
~~(same term as 785)~~

3.3 Crosstalk Tests

In this set of tests the crosstalk from one channel to another is measured. The measurement is made by measuring the transfer function from the input of one channel to the noise monitor output of adjacent channels. The noise monitor is used because it is a convenient measurement point and it provides a high gain, AC coupled measurement of the voltage output of the channel. The test setup is shown in the figure below. The driver channels should be setup for Low Noise operation, i.e. relays K1, K3 and K4 for all channels energized.

4 min. at 100 Hz approx.



Should specify drive level.
Source amp 72V overloads SR560s used as diff. drivers.

SR5004: noise f: 0.1-100 Hz
 SR5005: noise driver at
 SR5006:

Serial Number: _____

Date: _____

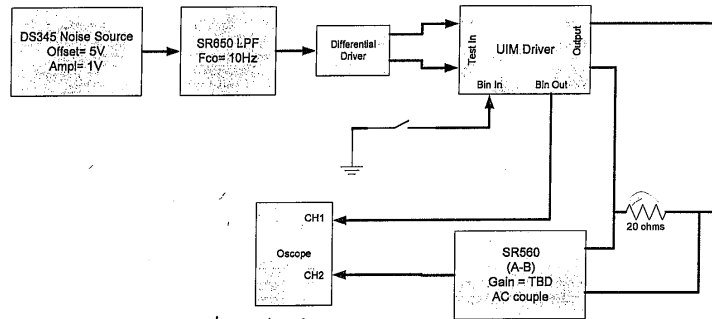
Tech: _____

The inputs to the unused driver channels should be tied to circuit ground, the coil driver outputs should be loaded with 20 ohms and the transfer function from each channel to the noise monitor output of the adjacent channels should be measured. The transfer function showing the highest cross coupling should be stored to a file. The file name is recorded in the space below.

File Name for Crosstalk Measurement: SRS CA1.78V *n.b. its entries are complex.*
Input and output channel numbers for saved file: 1 → 2

3.4 Mode Switching and Glitch Tests

In the test described below, an attempt is made to measure any transient currents that occur when relays K1, K3, and K4 are enabled. Each of the three relays should be tested sequentially in the order K1, then K3, then K4, leaving the previously tested relay energized when moving on to the next relay. The test setup is shown in the figure below.



4V, 5 overloads SR650
The signal source is a Stanford Research DS345 or equivalent that is set to produce random noise on top of a ~~5V~~ DC offset. The output of the signal generator is then low pass filtered by the SR650. This is done in an effort to simulate the types of signals that will be input to the driver during operation. A switch should be connected to the binary input controls for relays K1, K3 and K4 and the binary output monitor for the corresponding relay connected to channel 1 of the scope. The scope should be set to trigger on the rising edge of channel 1. Any changes in the output current caused by enabling the relays should be coincident with the corresponding monitor signal. If any glitches are observed note them in the space below and record the oscilloscope trace to disk.

Glitches Observed? Yes
Description: see attached pic.

File Name of recorded trace: TEK 00001.PNG

3.5 Monitors, Controls and Circuit Protection

3.5.1 Noise Monitor Transfer Function Tests

The noise monitor board in the driver chassis provides a low-noise, AC coupled monitor of the voltage output of each channel. The nominal transfer function of the monitor is 4 zeros at DC, 4

Serial Number: _____

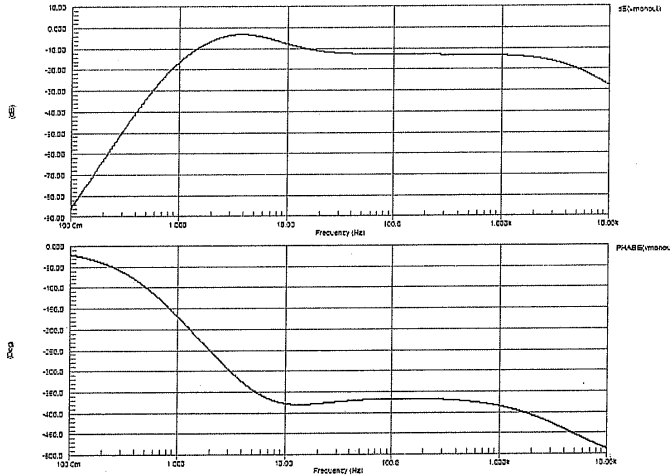
Date: _____

Tech: _____

poles at 5Hz and 2 poles at 5KHz which are added to the response of the driver channel. These tests measure the transfer function from the input of a particular driver channel to the corresponding noise monitor output. The coil driver output should be load with 20 ohms during the tests. The test setup for the measurements is the same as that for the crosstalk measurements with the exception that the noise monitor used is the monitor for the channel under test. Relays K1, K3 and K4 should be energized during the tests. The figure below shows the response nominal response.

→ LN-mode.

measurements set
SR3612



In the tables below, record the measured magnitude and phase of the response for each channel. In addition, save the transfer function for one representative channel to disk and record the file name in space provided below.

Table 13: Channel 1 Noise Monitor Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBV/Volt)	Nominal Phase (Degrees)	Actual Gain (dBV/Volt)	Actual Phase (Degrees)
0.1	-86.3	-20.9	-80.931	-21.26
1	-16.2	-169.5	-11.33	-172.7
10	-7.8	-377.6	-3.910	-381.7
100	-12.9	-366.7	-9.488	-367.6
1K	-13.4	-384.8	-10.091	-386
10K	-27.7	-486.6	-24.439	-494.3

Table 14: Channel 2 Noise Monitor Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBV/Volt)	Nominal Phase (Degrees)	Actual Gain (dBV/Volt)	Actual Phase (Degrees)
0.1	-86.3	-20.9	-80.682	-20.37
1	-16.2	-169.5	-10.607	-171

Serial Number: _____

Date: _____

Tech: _____

10	-7.8	-377.6	-3.408	-384
100	-12.9	-366.7	-9.841	-388.2
1K	-13.4	-384.8	-10.066	-388.59
10K	-27.7	-486.6	-24.152	-493.8

Table 15: Channel 3 Noise Monitor Transfer Function Measurements

Freq (Hz)	Nominal Gain (dBV/Volt)	Nominal Phase (Degrees)	Actual Gain (dBV/Volt)	Actual Phase (Degrees)
0.1	-86.3	-20.9	-81.063	-20.66
1	-16.2	-169.5	-11.154	-171.3
10	-7.8	-377.6	-3.638	-382
100	-12.9	-366.7	-9.471	-368
1K	-13.4	-384.8	-10.091	-386.96
10K	-27.7	-486.6	-24.947	-496.7

Table 16: Channel 4 Noise Monitor Transfer Function Measurements

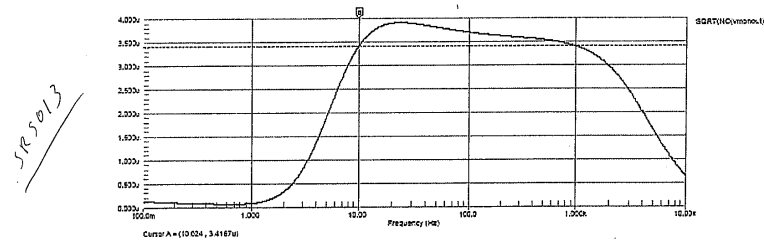
Freq (Hz)	Nominal Gain (dBV/Volt)	Nominal Phase (Degrees)	Actual Gain (dBV/Volt)	Actual Phase (Degrees)
0.1	-86.3	-20.9	-81.173	-20.35
1	-16.2	-169.5	-11.13	-170.5
10	-7.8	-377.6	-3.545	-382.4
100	-12.9	-366.7	-9.488	-381
1K	-13.4	-384.8	-10.092	-387
10K	-27.7	-486.6	-24.495	-496.9

File Name for Noise Monitor Measurement: SR5012.78V

Channel number for saved file: 1

3.5.2 Noise Monitor Output Noise Tests

A plot of the simulated noise versus frequency is shown in the figure below.



Serial Number: _____

Date: _____

Tech: _____

As can be seen from the plot, the noise at 10Hz at the monitor output should be approximately 3.4uV/√Hz. In the table below, record the output noise at 10Hz. The inputs to the channel under test should be tied to circuit ground and relays K1, K3 and K4 should be energized (Low Noise Mode). In addition, save the noise data for one representative channel to disk and record the file name in space provided below. The frequency range for the saved file should be from 0.1Hz to 100Hz.

Channel Number	Measured Noise at 10Hz
1	3.296 $\mu\text{V}/\sqrt{\text{Hz}}$
2	3.189
3	2.94
4	3.171

File Name for noise measurement: SU5013.78V
 Channel Number for saved file: 1

3.5.3 Output Voltage and Current Monitor Tests

V_{in} numbers would be useful. Move GND TVs.

The monitor board connected to the UIM Driver board inside the chassis provides continuous monitors of the output voltage and current (FC) and rms current (SC) for each channel. These monitors are tested in this section. These tests can be conducted in conjunction with the dynamic range tests described in section 3.1.3 of this document. In the tables below, record the current and voltage monitor output for each input voltage.

Table 17: Channel 1 Monitor Output Tests

Input Voltage	Nominal Voltage Monitor	Nominal Current Monitor (FC)	Nominal rms Current Mon (SC)	Actual Voltage Monitor (Volts)	Actual Current Monitor (Volts)	Actual Current rms Monitor (Volts)
+1V	0.443	0.217	0.217	0.403	0.202	0.020
-1V	-0.443	-0.217	±0.217	-0.444	-0.220	0.021
+5V	2.22	1.09	1.09	2.194	1.094	0.1108
-5V	-2.22	-1.09	±1.09	-2.185	-1.087	0.1076
+10V	4.43	2.17	2.17	4.354	2.168	0.217
-10V	-4.43	-2.17	±2.17	-4.355	-2.170	0.219
+20V	8.87	4.34	4.34	8.166	4.068	0.406
-20V	-8.87	-4.34	±4.34	-8.173	-4.073	0.398

Table 18: Channel 2 Monitor Output Tests

Input Voltage	Nominal Voltage Monitor	Nominal Current Monitor (FC)	Nominal rms Current Mon (SC)	Actual Voltage Monitor (Volts)	Actual Current Monitor (Volts)	Actual Current rms Monitor (Volts)
+1V	0.443	0.217	0.217	0.419	0.207	0.020
-1V	-0.443	-0.217	±0.217	-0.444	-0.221	0.021
+5V	2.22	1.09	1.09	2.208	1.101	0.1114
-5V	-2.22	-1.09	±1.09	-2.183	-1.088	0.1076
+10V	4.43	2.17	2.17	4.397	2.172	0.217
-10V	-4.43	-2.17	±2.17	-4.367	-2.172	0.213
+20V	8.87	4.34	4.34	8.167	4.072	0.406
-20V	-8.87	-4.34	±4.34	-8.174	-4.074	0.399

Serial Number: _____

Date: _____

Tech: _____

Table 19: Channel 3 Monitor Output Tests

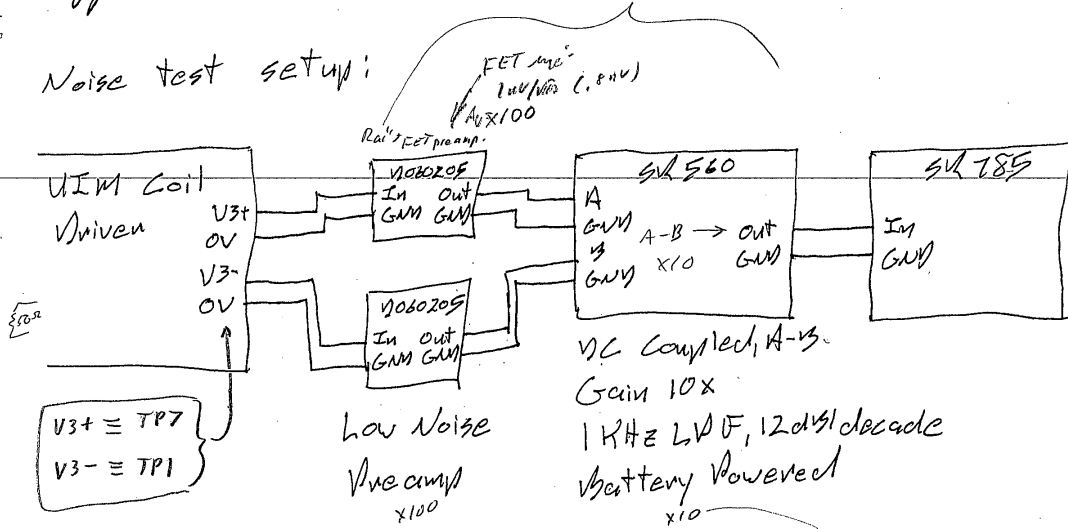
Input Voltage	Nominal Voltage Monitor	Nominal Current Monitor (FC)	Nominal rms Current Mon (SC)	Actual Voltage Monitor (Volts)	Actual Current Monitor (Volts)	Actual Current rms Monitor (Volts)
+1V	0.443	0.217	0.217	0.405	0.204	0.020
-1V	-0.443	-0.217	0.217	-0.446	-0.221	0.022
+5V	2.22	1.09	1.09	2.207	1.103	0.1115
-5V	-2.22	-1.09	1.09	-2.197	-1.094	0.1088
+10V	4.43	2.17	2.17	4.352	2.171	0.2170
-10V	-4.43	-2.17	2.17	-4.361	-2.174	0.2137
+20V	8.87	4.34	4.34	8.157	4.072	0.406
-20V	-8.87	-4.34	4.34	-8.176	-4.078	0.399

Table 20: Channel 4 Monitor Output Tests

Input Voltage	Nominal Voltage Monitor	Nominal Current Monitor (FC)	Nominal rms Current Mon (SC)	Actual Voltage Monitor (Volts)	Actual Current Monitor (Volts)	Actual Current rms Monitor (Volts)
+1V	0.443	0.217	0.217	0.421	0.205	0.208 0.02
-1V	-0.443	-0.217	0.217	-0.444	-0.222	0.021
+5V	2.22	1.09	1.09	2.202	1.097	0.1116
-5V	-2.22	-1.09	1.09	-2.164	-1.079	0.1068
+10V	4.43	2.17	2.17	4.352	2.167	0.2175
-10V	-4.43	-2.17	2.17	-4.355	-2.171	0.2135
+20V	8.87	4.34	4.34	8.176	4.072	0.4076
-20V	-8.87	-4.34	4.34	-8.178	-4.075	0.399

Bigger boxes to write in.

Noise test setup:



Noise @ 10 Hz w/ 6.6VDC offset on output

Ch. 1	2.949 $\mu\text{V}/\sqrt{\text{Hz}}$	$\div 10^3 = 2.95 \text{ nV}/\sqrt{\text{Hz}}$ for ch. 1
2	2.726	
3	2.771	
4	2.908	

Filename: SR5014.78V Channel: 1

looking at this file: (10Hz, $2.94 \times 10^{-6} \text{ V}_{\text{rms}}/\sqrt{\text{Hz}}$)

This is the baseline ref. for the test set up noise

preamp + SR560 + SR785
x100 x10

The file SR5004 is the measurement of the UIM driver in LN-mode.

Comparison:

$$\begin{aligned} \text{SR5004: } & \text{V}_{\text{rms}}/\sqrt{\text{Hz}} \\ \text{at 10Hz: } & \frac{4.825 \times 10^{-5}}{10} = \\ & = 4.825 \times 10^{-6} \end{aligned}$$