LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
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Timing System Document Map
Advanced LIGO

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Timing System Document Map
Advanced LIGO

This document provides a broad overview of the documentation structure of the Timing System associated with the Advanced LIGO. Its intended purpose is to enable fast access to the available information and to facilitate understanding.

Rationale:

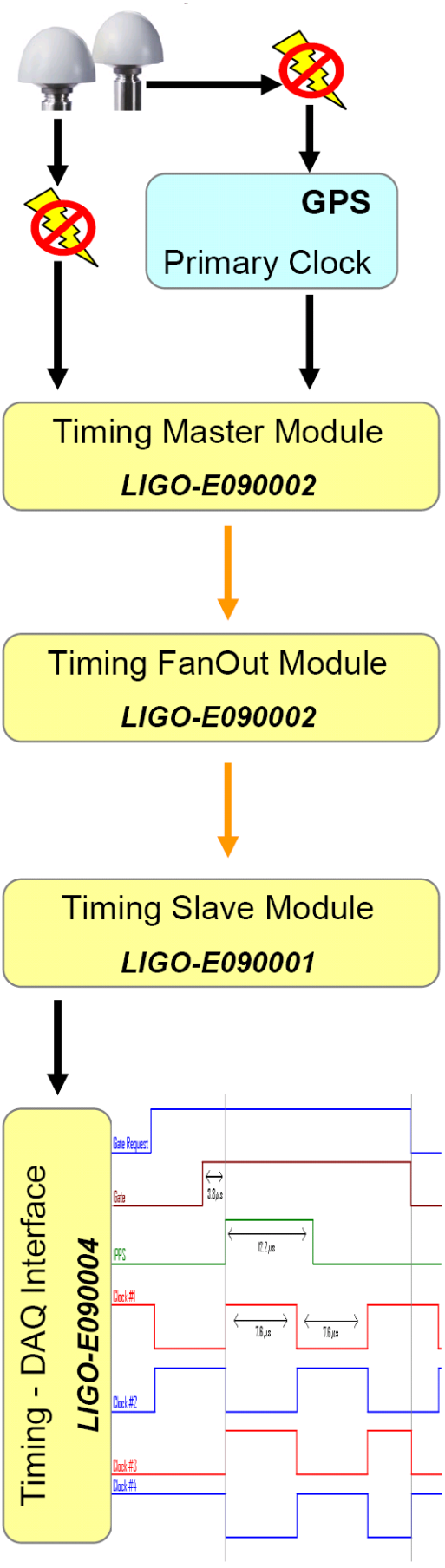
The Advanced LIGO Time-Stamping System (*thereafter ATS*) directly provides the 2^N clock to the Analog-to-Digital/Digital-to-Analog Converter (*ADC/DAC* thereafter) boards of the Advanced LIGO Data Acquisition System (*DAQ* thereafter). The ATS relies on redundant GPS based primary time sources (*GPS* thereafter) and an optical fiber based timing distribution system (*TDS* thereafter).

The Advanced LIGO Timing Diagnostic System (*thereafter ATD*) provides diagnostic signals that allow traceable Timing and Phase Calibration (*TPC* thereafter) of the archived LIGO data stream for the useful lifetime of the project. The ATD relies on *'flywheeling'* Caesium Atomic Clocks (*CAC* thereafter) as its primary time source and a commercial optical fiber based timing distribution system (*TSC* thereafter).

The relative, site-to-site TPC of gravitational wave observatory sites is ensured through the usage of the common global UTC time reference via the GPS system. Transient errors of the GPS system can be diagnosed by the redundant and independent GPS and CAC systems continually verifying each other.

Requirements in perspective

ATS ensures that that the UTC time stamp of each ADC/DAC sample is known for better than the required 1μs. The GPS-to-UTC accuracy is specified by the government to 100ns, albeit better is achievable with carefully tuned equipment. Our comparison of precision commercial GPS based primary time sources to each other in the laboratory (exposed to their environment) indicated that their relative time can deviate by <300ns between devices, however a carefully controlled environment and matched calibration can reduce this discrepancy. The TDS automatically corrects for the delays in the optical fibers connecting its modules. The step size for this correction is 15ns, however it can be refined if need arises. During the tests in our laboratory we simulated extreme environmental conditions. Abrupt and direct exposure of the Oven-stabilized Crystal Oscillator (*OCXO* thereafter) of the TDS resulted in <200ns transient discrepancies, however these could be mitigated through careful control of the OCXO's environment. These a-priory and observed systematics leave ~385ns safety margin for the end-to-end system. Tests in our laboratories indicated that even in uncontrolled environments and using 4km long optical fibers, the ATS reliably provides better performance than this conservative safety margin.



- Commercial GPS Antennae for the primary GPS clock and the redundant *'failover'* (internal) GPS clock are connected through lightning protection and in-line amplifier using LMR-400 Plenum cable.

- High quality commercial GPS receiver serves as the primary GPS clock.

- The 1 pulse per second (1PPS) signal output of the GPS serves as an input to the Advanced LIGO timing distribution system

- The Master Module of the Timing Distribution System takes the 1PPS from the primary GPS clock and the failover GPS antenna signals as inputs. It outputs maximum 16 optical signals through fibers that are capable of transmitting precise time to FanOut and Slave Modules. Full technical description and manufacturing details are given in LIGO-E090002.

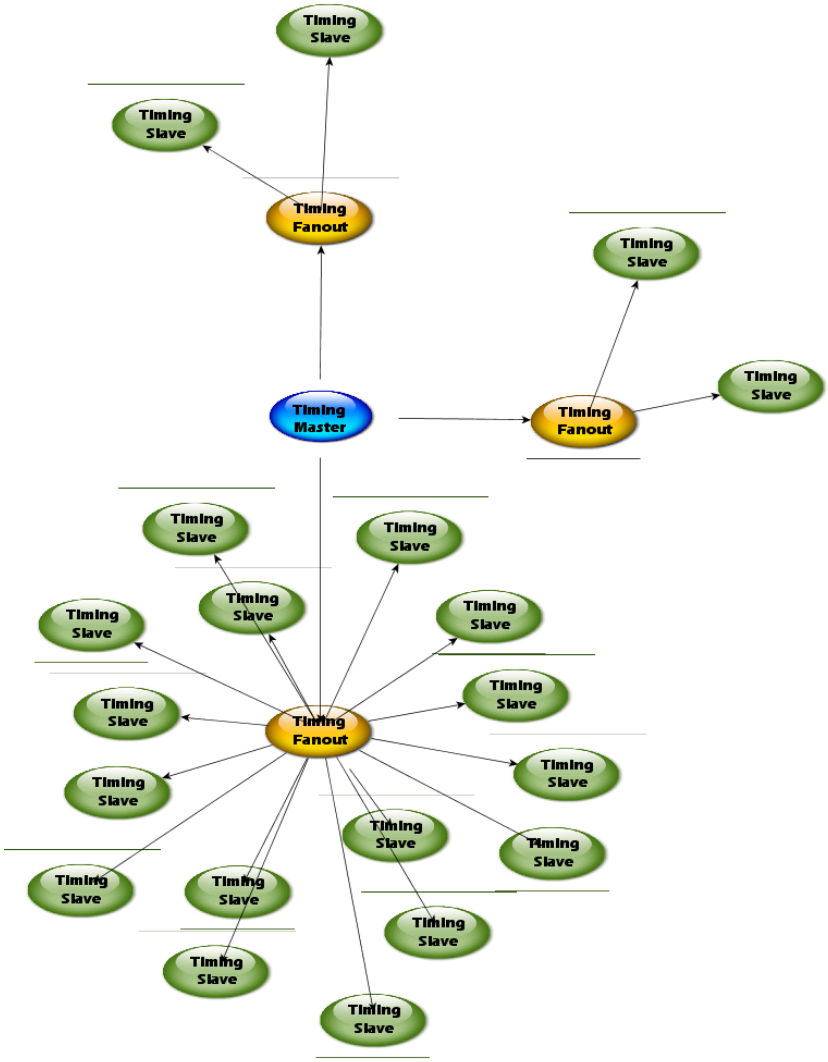
- The FanOut Module of the Timing Distribution System takes the encoded timing signal from the Master Module through optical fiber. It outputs maximum 16 optical signals through fibers that are capable of transmitting precise time to other FanOut and Slave Modules. Full technical description and manufacturing details are given in LIGO-E090002.

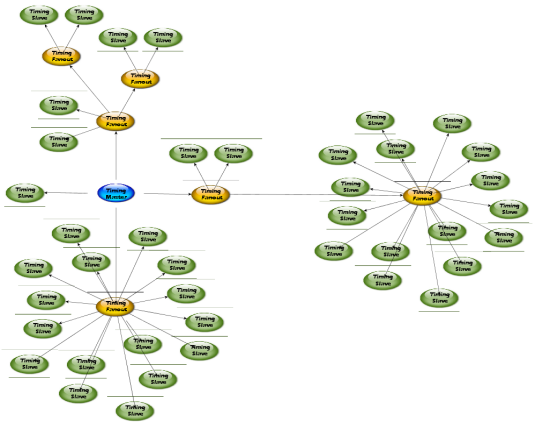
- The Slave Module of the Timing Distribution System takes the encoded timing signal from the Master or a FanOut Module through optical fiber. It outputs TTL compatible logic signals to drive the clock input of the ADC/DAC boards. Full technical description and manufacturing details are given in LIGO-E090001.

- The passive Timing-DAQ interface board provides conversion from header type connectors on the Slave Module to connectors of the ADC/DAC/Logic boards. Full technical description and manufacturing details are given in LIGO-E090004.

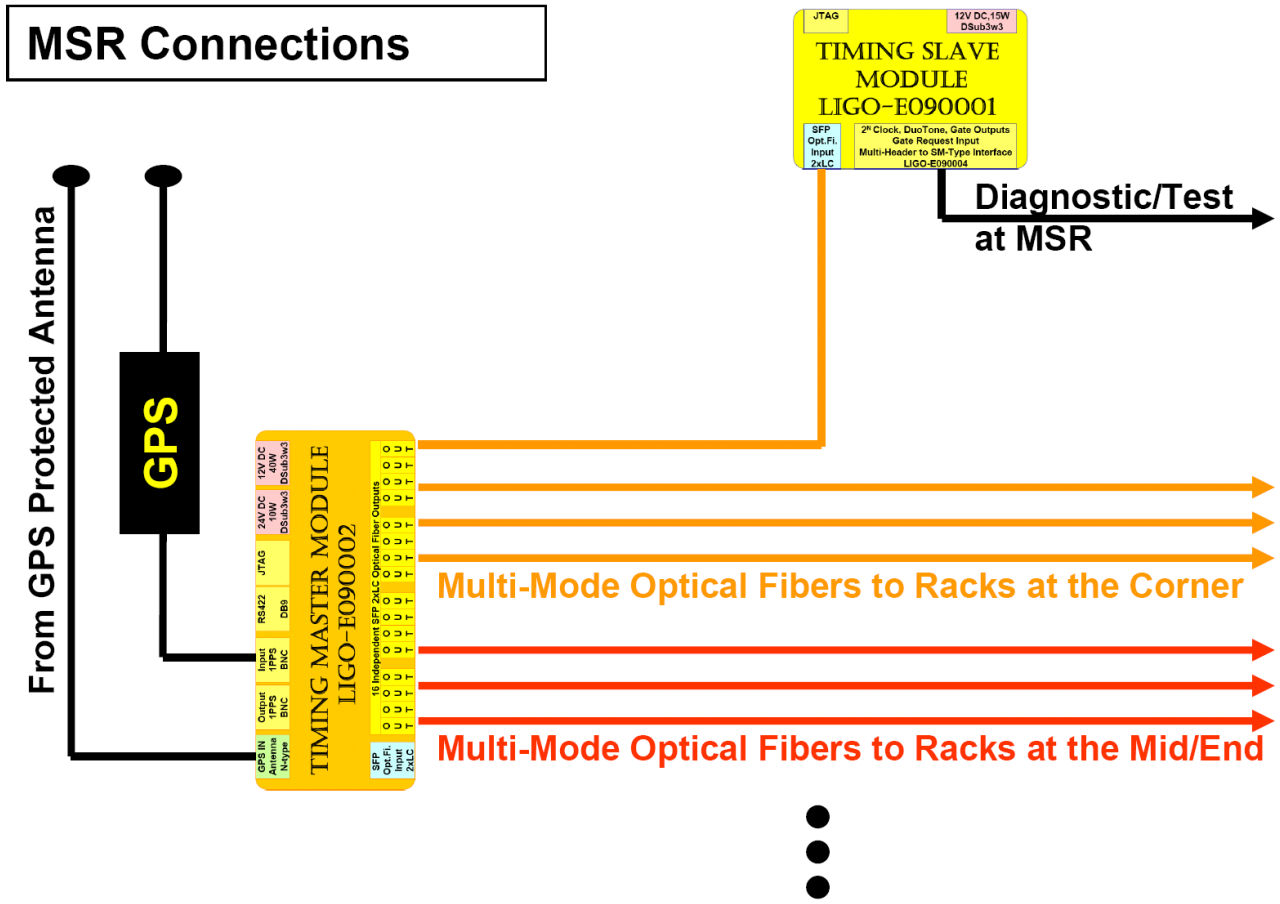
The deployment ready and tested modules and boards, as described in LIGO-E090001 - LIGO-E090004, can be readily integrated to serve the desired configuration. The detailed instructions for field deployment are provided in LIGO-E080542.

Possible arbitrary configurations in the block diagrams below emphasize the flexibility of the Timing Distribution System:

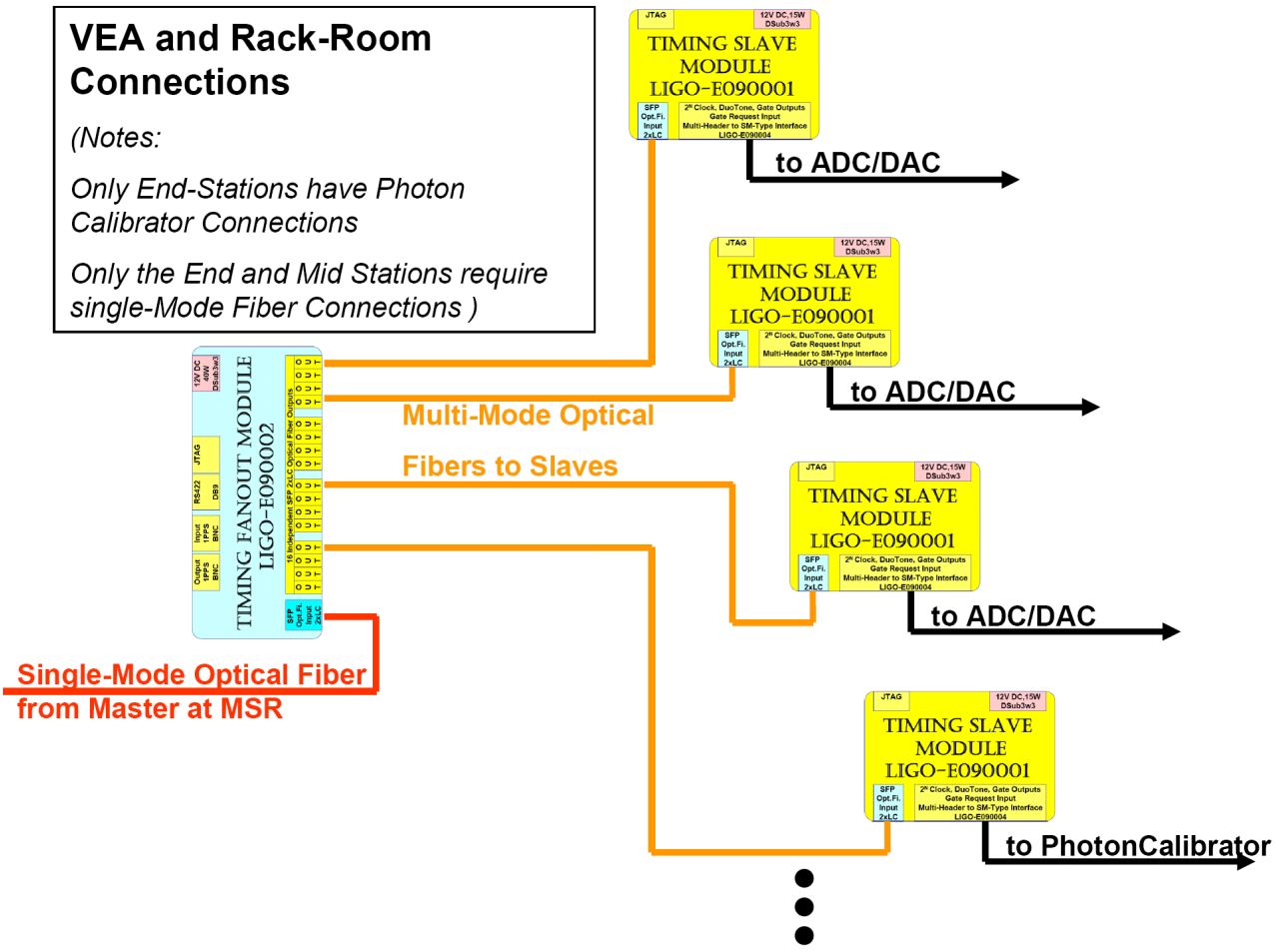




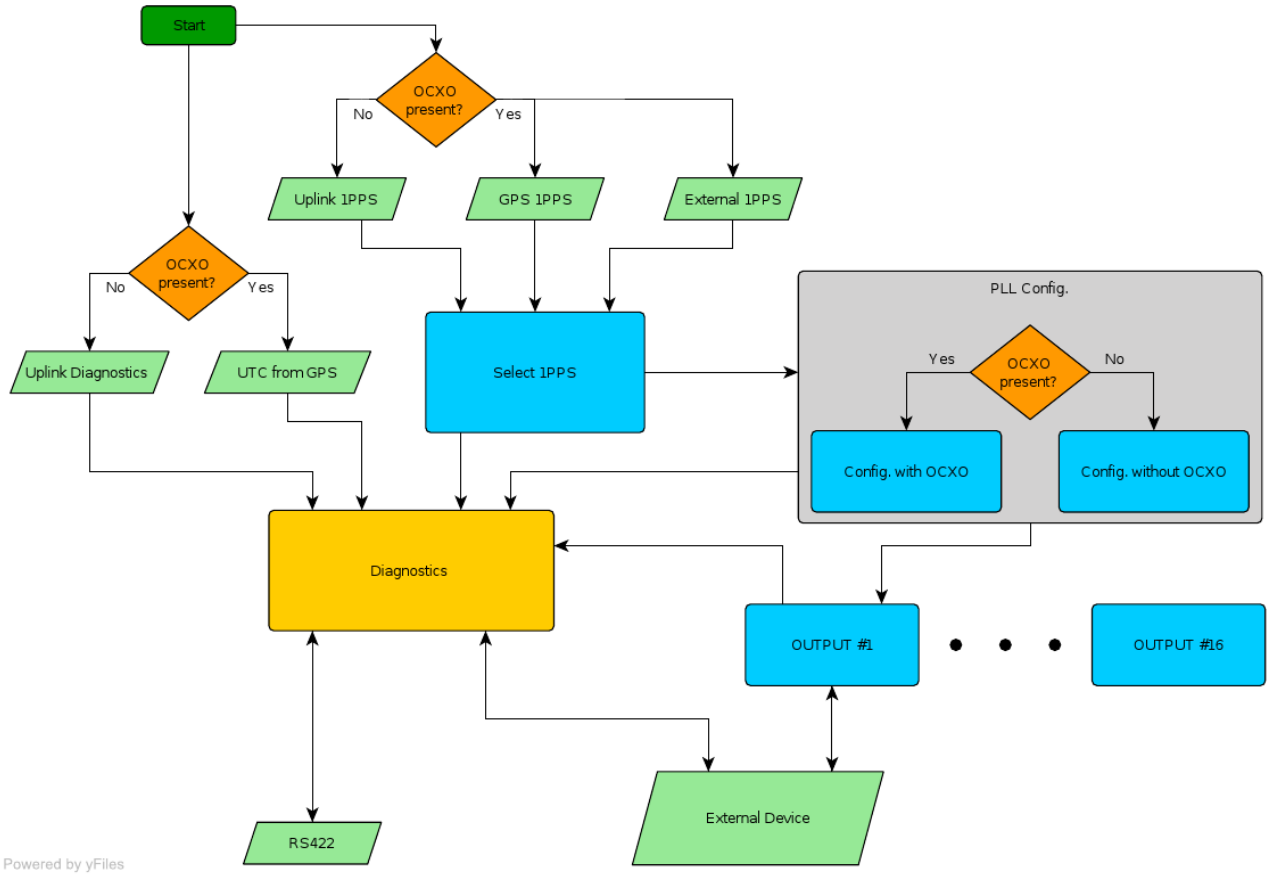
Generic MSR layout:



Generic layout for VEAs and rack rooms:



Master and FanOut Main Diagram

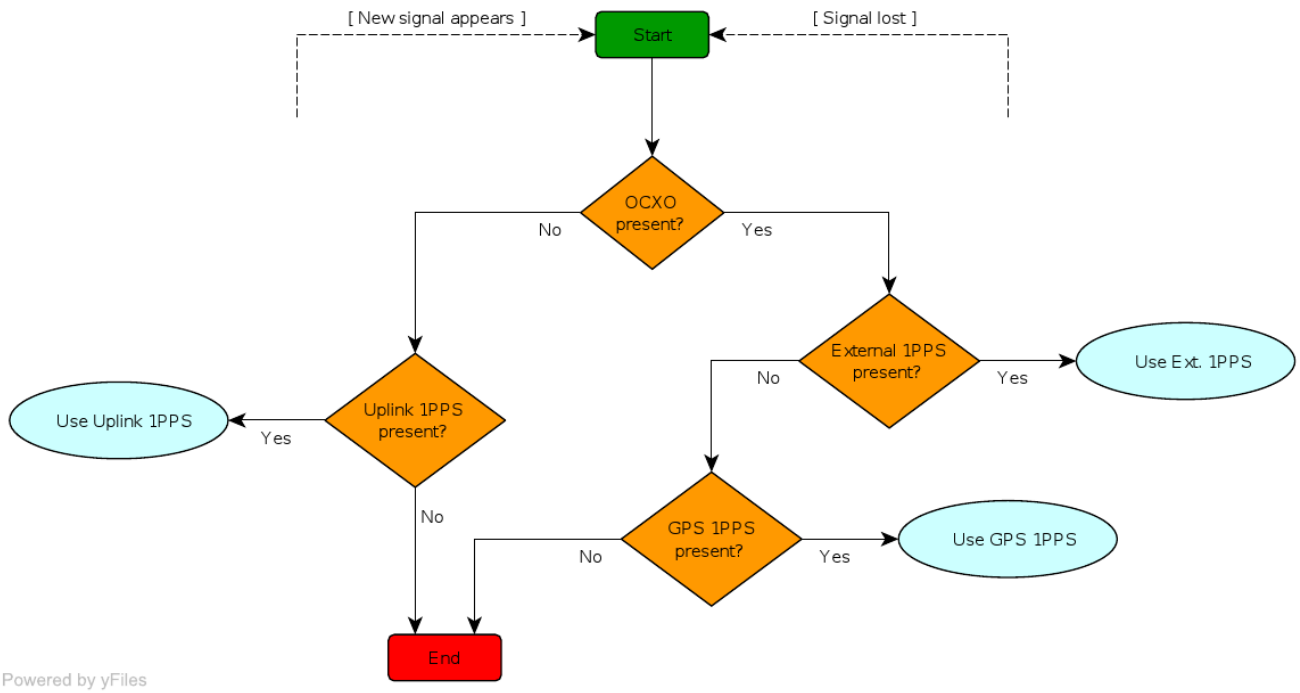


The Master and FanOut Main Diagram (Main Diagram) summarizes the operation of the Master and FanOut Modules, representing the main, distinct parts of operation with separate *'black-boxes'*. The detailed operation of these parts are shown in separate diagrams below.

There is an order in which the system sets itself up in the case of startup or change/error in the input signals. This order is shown on the Main Diagram. First, the system checks whether it has a built in OCXO. This determines whether it will operate as a Master (has OCXO) or as a FanOut (has no OXCO), and thus which inputs it will use for communication with other boards and to which inputs it locks its internal clock to.

Next, the system uses a phase locked loop (PLL) to lock its internal clock to the proper external signal. Finally, the system sends out timing information to external devices based on its locked internal clock. The whole process is being diagnosed and diagnostics information is sent upstream and downstream. Diagnostics information is eventually collected from connected boards and can be sent to an external computer.

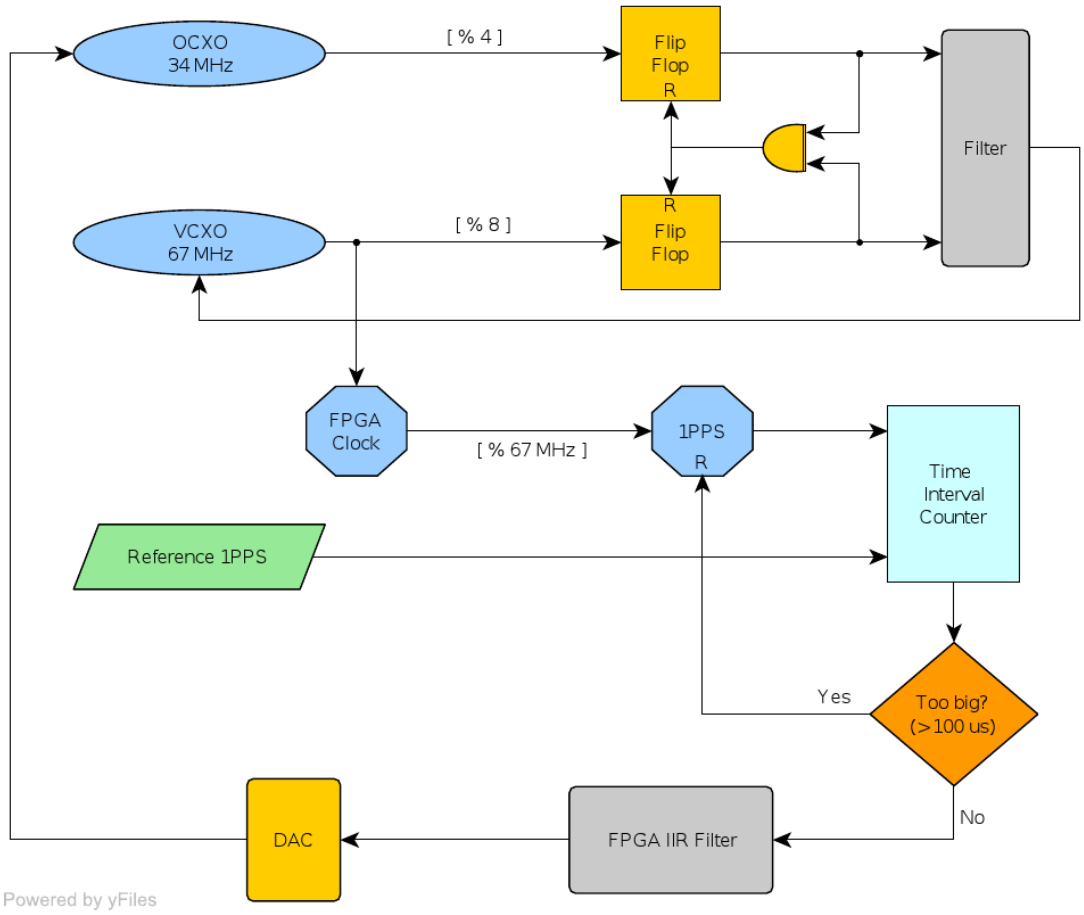
Select 1PPS Diagram



The procedure depicted on the Select 1PPS Diagram shows the detailed operation of the Select 1PPS box on the Main Diagram. It describes the procedure of how a Master or FanOut Module selects the external 1PPS source that it uses to lock its internal clock.

There is an order of preference in which the Module selects the 1PPS source, if they are present. The selection process is different for Master (has OCXO) and FanOut (has no OCXO) Modules. After a selection is made, the Module will use the selected 1PPS source until the signal from the source is lost or a new signal source becomes active. In this case the selection process is restarted. The selection process as a whole is executed in a tiny portion of a second therefore it does not interfere with other processes. Changing the time source always generates a diagnostic flag.

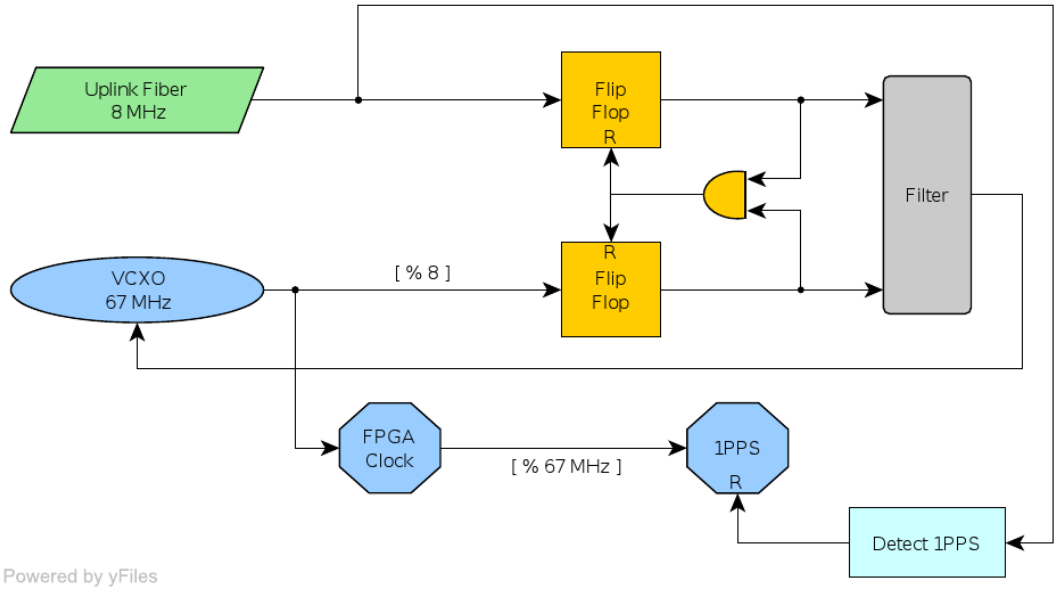
Master PLL Configuration Diagram



The Master PLL Configuration Diagram shows the process how the Master Module locks its OCXO to an external reference 1PPS chosen previously by the Select 1PPS process, and its internal clock to the OCXO.

The Master PLL uses two internal clocks, an OCXO and a VCXO. The clock signal used in FPGA (FPGA clock) is taken from the VCXO. The signals of these two clocks, after being transformed to ~8MHz, go to a phase detector that consists of positive-edge-triggered flip-flops with asynchronous resets and an AND gate. After the phase detector, the signal reaches a filter that operates as the servo compensation, providing feedback to the VCXO to synchronize it to the OCXO. A 1PPS signal, obtained from the VCXO clock signal, is then compared to the reference 1PPS from the source previously chosen by Select 1PPS. If the difference is above threshold, the 1PPS is reset, otherwise it goes through a low pass filter and is used to lock the OCXO to the external reference by changing the applied control voltage on it.

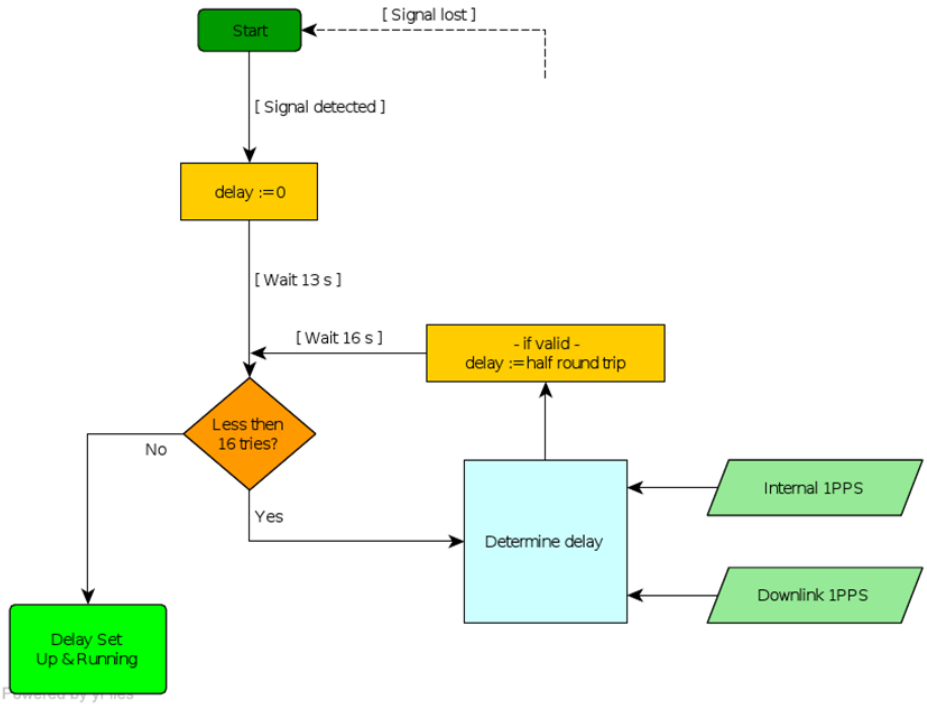
FanOut PLL Configuration Diagram



The FanOut/Slave PLL Configuration Diagram shows the process of how the FanOut or Slave Module locks its internal clock (VCXO) to an external reference 1PPS coming from an upstream Master or FanOut Module (the upstream source was chosen by Select 1PPS using the fact that OCXO is not present).

The VCXO receives a similar feedback from a filter from the comparison of its clock signal to the uplink source than for the case of the Master PLL Configuration. The VCXO clock signal is then used to provide the FPGA clock. The 1PPS is based upon direct comparison to the 1PPS from the uplink source.

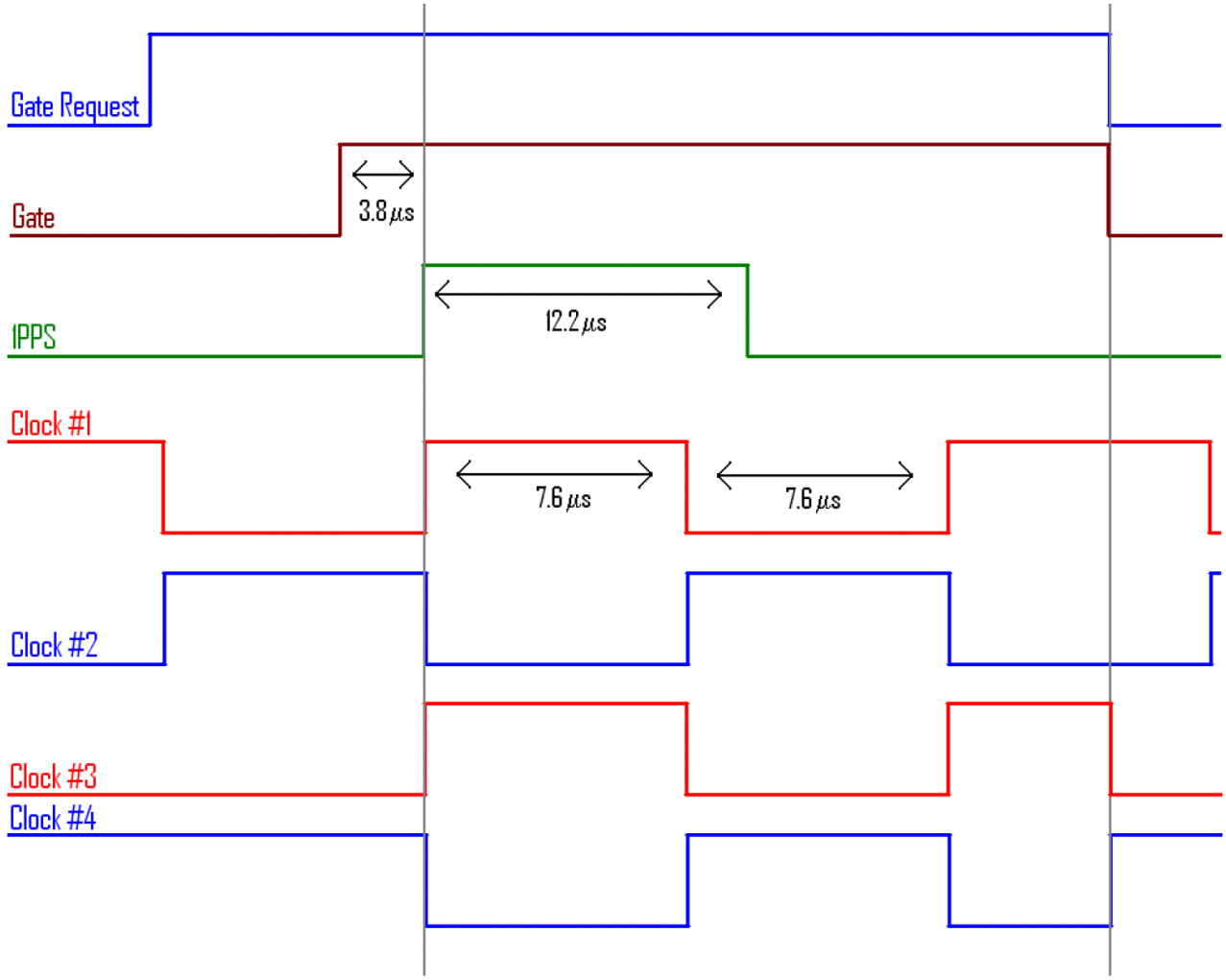
Fiber Delay Determination Diagram



The Fiber Delay Determination Diagram (Output module of the main diagram) shows how the correct time shift of an output to an external device is determined. The output consists of an 8 MHz clock signal, 1PPS and diagnostics information.

After a signal is detected from the external device connected to the Output, the Master or FanOut Module starts the transmission of the output signal (clock signal, 1PPS and diagnostics). The external device (a FanOut or Slave board) automatically synchronizes its internal 1PPS to the received 1PPS, and sends this 1PPS back. The Master or FanOut Module measures the delay of the received 1PPS from which it can determine the delay due to signal transmission time. This delay is then compensated for by sending out the 1PPS signal in advance to the internal 1PPS of the Master or FanOut Modules. Delay is determined 16 times, using 16 seconds for each determination (except the first that takes 13 seconds). The determined value of the delay is then stored, therefore it is a fixed value after system startup, this way preventing fluctuations due to noise. In case of loss of signal, the determination of the delay restarts. This enables the change of external devices or cables without restarting the whole system.

ADC/DAC Clock and Gating Signals

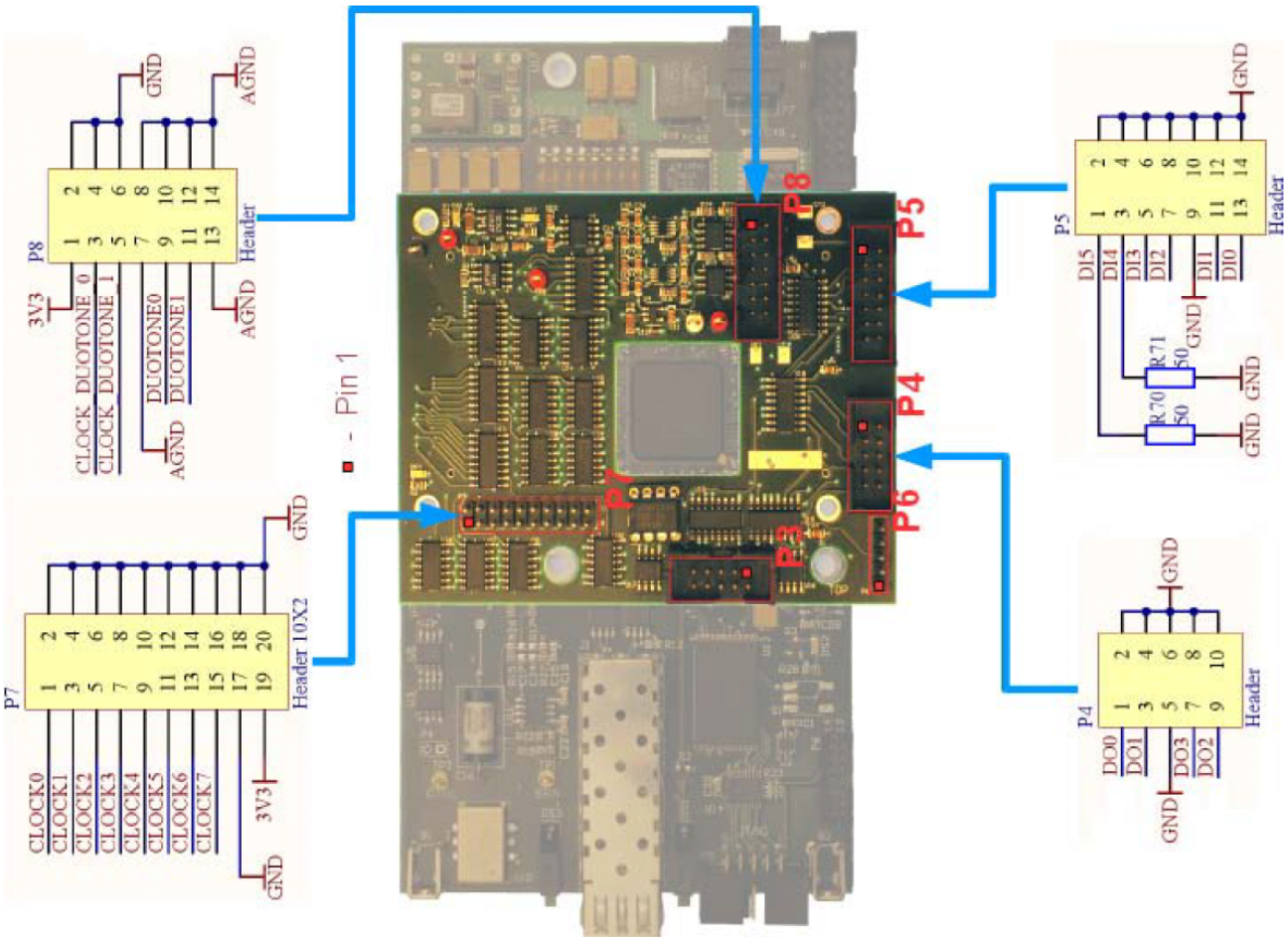


The purpose of the Slave Module is to provide synchronized Clock, Gate and DuoTone signals to the ADC/DAC boards. Besides a constant and synchronized clock signal, the Slave Module also defines when to start the conversion process.

Gate and Gate Request: Some ADC/DAC boards need a separate 2^{16}Hz Clock signal and a Gate signal. A conversion happens at the rising edge of each clock signal. The ADC/DAC board does not send the acquired data upstream until the Gate signal goes high. Consequently a properly timed Clock/Gate signal pair ensures that the first communicated conversion happens exactly at the rising edge of the 1PPS/UTC second tic. The Slave ensures that the Clock is synchronized to 1PPS/UTC and that the Gate rising edge is placed just right preceding the 1PPS/UTC rising edge. In practice, this is determined based on the user input that sends a Gate Request signal to the Slave Module. Gate Request informs the Slave that conversion should start at the next available 1PPS signal rising edge. In response, the Slave issues a Gate signal to the ADC/DAC boards ~4 μs before the consecutive 1PPS signal rising edge (after the arrival to the Gate Request signal). A 180° phase shifted Clock signal is also provided if needed. See Gate Request, Gate, 1PPS, Clock#1 and Clock#2 signal timing in the figure above.

Gated Clock: Some DAC/ADC boards do not have separate Clock and Gate inputs, only a Clock input. These converter boards are able to do the conversion at the first incoming Clock rising edge. Therefore, the Slave Module also provides gated clock signals. After the Gate Request signal turns on, the Gated Clocks will turn on at the next consecutive rising edge of the 1PPS/UTC signal. A 180° phase shifted Clock signal is also provided if needed. See Gate Request, Gate, 1PPS, Clock#3 and Clock#4 signals. The Gate and Gated Clock signals turn off immediately when Gate Request turns off.

The physical interface towards the ADC/DAC boards is provided through header type connectors:



The passive header to ADC/DAC connector converter boards will be provided as part of the DAQ chassis infrastructure.

Further Information

Further and more detailed information on the system is available in the following documents, and in other documents referenced within them: LIGO-E080542, LIGO-E090001, LIGO-E090002, and LIGO-E090004.

Glossary of Timing System Related Terms:

ADC	Analog-to-Digital Converter
ATD	Advanced LIGO Timing Diagnostic System
ATS	Advanced LIGO Time-Stamping System
BCD	Binary Coded Decimal
CAC	Caesium Atomic Clock
DAC	Digital-to-Analog Converter
DAQ	Advanced LIGO Data Acquisition System
DCLS	Direct Current Level Shift, or digital IRIG
Flywheel	Maintaining time (frequency) when the primary reference source has been lost
GPS	Global Positioning System
HW	Hardware
IRIG	Serial time format standard maintained by the Inter Range Instrumentation Group
NIST	National Institute of Standards and Technology
OCXO	Oven-Controlled Crystal Oscillator
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
1PPS	pulse per second
RAC	Rubidium Atomic Clock
SW	Software
TCXO	Temperature Compensated Crystal Oscillator
TDS	Optical fiber based timing distribution system
TPC	Timing and Phase Calibration
TSA	Timing System for Advanced LIGO
TSC	Commercial optical fiber based timing distribution system
USNO	U.S. Naval Observatory
UTC	Universal Coordinated Time (UTC), ITU standard since 1972.
XO	Crystal Oscillator
VCXO	Voltage-controlled Crystal Oscillator.