LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Technical Note	LIGO-E090001-00-D	01/04/09

Chassis Integration Plan
Clock, Gate, and DuoTone Signal Interface
Advanced LIGO

Imre Bartos, Rolf Bork, Maxim Factourovich Jay Heefner, Szabolcs Márka,
Zoltán Raics, Paul Schwinberg and Daniel Sigg

This is an internal working note
of the LIGO Project.

California Institute of Technology
LIGO Project – MS 51-33
Pasadena CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project, MIT NW22-295,
185 Albany St.,Cambridge, MA 02139 USA
Phone (617) 253 4824
Fax (617) 253 7014
E-mail: info@ligo.mit.edu

Columbia University
Columbia Astrophysics Laboratory
Pupin Hall - MS 5247
New York NY 10027
Phone (212) 854-8209
Fax (212) 854-8121
E-mail: geco.cu@gmail.com

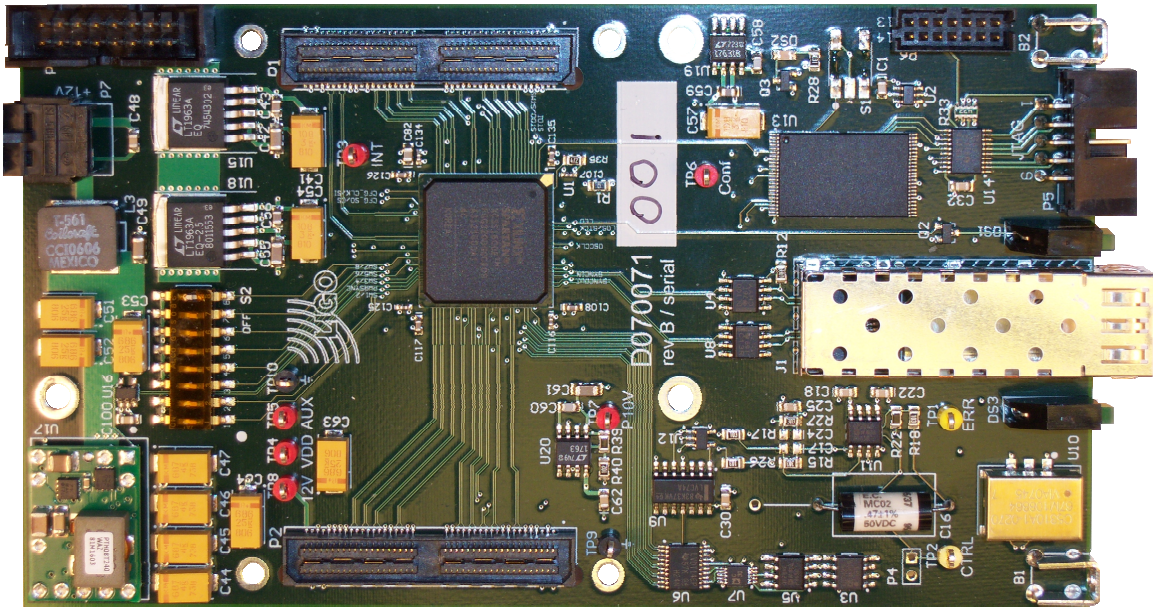
WWW: http://www.ligo.caltech.edu

Chassis Integration Plan: Clock, Gate, and DuoTone Signal Interface for Advanced LIGO

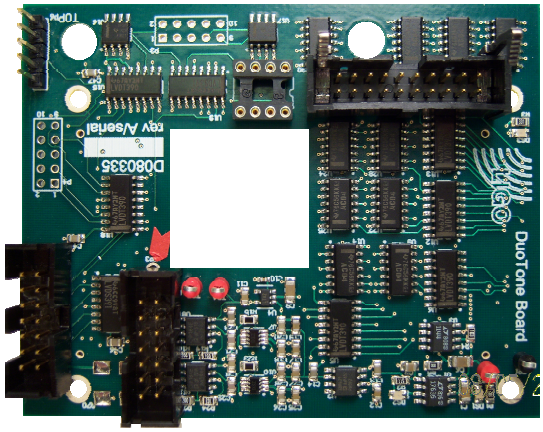
This document provides an overview of the documentation covering the production, programming, and testing of the Clock, Gate, and DuoTone Signal Interface (Slave) node assemblies. Its intended purpose is to enable the manufacturing of deployment ready modules.

Visual identification of circuit boards

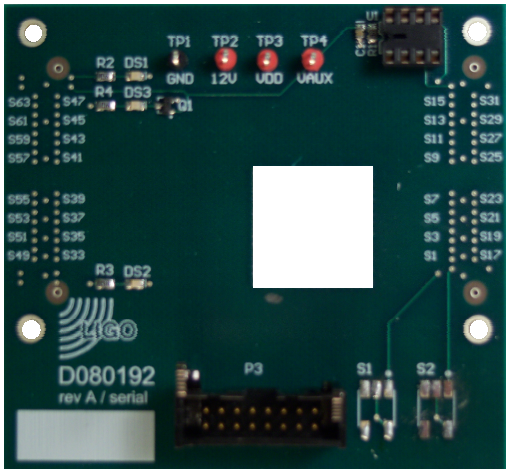
Slave board:



Clock, Gate and DuoTone interface daughter circuit board



Hardware and FPGA test daughter circuit board



Board Designs

- **Slave board (LIGO-D070071) design:**
  - Schematics is described in:
    - Overview of the schematics: D070071-B.pdf
    - Detailed Altium files: D070071-B.zip
  - PCB Design is described in:
    - Detailed Altium files: D070071-B.zip
  - Order/Manufacturing package is provided in:
    - Detailed files: D070071-B.zip

- **Clock, Gate and DuoTone interface daughter board (LIGO-D080335) design:**
  - Schematics is described in:
    - Overview of the schematics: D080335-B.pdf
    - Detailed Altium files: D080335-B.zip
  - PCB Design is described in:
    - Detailed Altium files: D080335-B.zip
  - Order/Manufacturing package is provided in:
    - Detailed files: D080335-B.zip

- **Hardware and FPGA test daughter board (LIGO-D080192) design:**
  - Schematics is described in:
    - Overview of the schematics: D080192-B.pdf
    - Detailed Altium files: D080192-B.zip
  - PCB Design is described in:
    - Detailed Altium files: D080192-B.zip
  - Order/Manufacturing package is provided in:
    - Detailed files: D080192-B.zip

Board Test

- Test Documents:
  - Slave board test:
    - Procedure: LIGO-E050262.pdf
    - FPGA: Code
  - Clock, Gate and DuoTone interface assembly test:
    - Procedure: LIGO-E0900019.pdf
    - FPGA: Code

Chassis Assembly

- Front Panel Design:
  - D080703-A.fpd
- Quick Start Guide / Specifications:
  - LIGO-E080541.pdf
- Product FPGA Code:
  - Code